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To cite this version:

Francois Rivet, Yann Deval, Jean-Baptiste Begueret, Dominique Dallet, Philippe Cathelin, et al.. The first experimental demonstration of a SASP-based full Software Radio Receiver. IEEE Radio Frequency Integrated Circuits Symposium (RFIC 2009), Jun 2009, Boston, United States. pp.25-28, 10.1109/RFIC.2009.5135482 . hal-00359769

HAL Id: hal-00359769

https://hal.science/hal-00359769v1

Submitted on 6 Aug 2013

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The first experimental demonstration of a SASP-based full Software Radio Receiver

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***Abstract*— This paper presents the principles of a Sampled Analog Signal Processor (SASP) dedicated to Software Radio mobile device. Many technological bottlenecks are to be overcome. The idea is to design a discrete analog signal processor to challenge theses bottlenecks. The main issue associated with the A/D conversion is thus avoided. The SASP aims to select a spectral envelope of a RF signal among all RF signals. To reach that target, the SASP processed analogically the RF input signal spectrum thanks to an analog Discrete Fourier Transform (DFT). Once the spectrum processed, only the voltage samples representing the signal envelope to be treated are converted into digital. The selection of few voltage samples among thousands others replaces the classical mixing and filtering operations. It dramatically reduces the A/D conversion frequency from GHz to MHz frequencies. Design strategy, applications and for the very first time, measurements are presented.**

***Index Terms*— analog signal processing, software radio, cognitive radio, sampled analog signal processor.**

I. Introduction

SOFTWARE Radio (SR) concept is to replace most of the analog signal processing with digital signal processing to provide flexibility through reconfiguration in future transceivers [1]. Consequently, a SR receiver is composed by an antenna, an Analog to Digital Converter (ADC) and a DSP. But, a critical technological bottleneck prevents from realizing such architecture in the case of mobile terminals: the ADC requires a 17-bit resolution at RF frequencies [2] and the DSP must handle the digital flow at the same rate. It leads to a power consumption of hundreds of Watts which is not compatible with mobile device constraints.

A disruptive approach is to shift a part of the digital signal processing into the analog domain. A Sampled Analog Signal Processor (SASP) is designed to carry out analog operations on discrete voltage samples at RF frequencies with low power consumption [3]. It aims to relax ADC constraints and coherently the DSP constraints by decreasing its working frequency. It is located between the antenna and ADC in a SR receiver (Fig. 1). However, to reduce the constraints on the SASP front-end, a LNA can be added as well.

The SASP principle is based on the frequency translation (Fig. 2). Instead of working into time domain, the idea is to work into frequency one. The observation is that a RF signal envelope varies slowly compared to its carrier frequency.

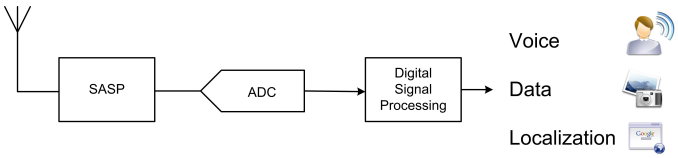

Fig. 1. Proposed SR architecture

Signal processing on the RF signal envelope is thus focused. Given the criteria of reconfigurability constrained by SR, the SASP intent to process any RF signal envelope in a 0 to 5GHz frequency range.

The SASP processes analogically a Fast Fourier Transform. The purpose is to extract the desired input signal envelope by recovering its spectrum. Among thousands of voltage samples, only the ones representing the wanted RF signal envelope are sent out towards an A/D conversion (Fig. 2). The converted samples are translated to baseband. An Inverse Fast Fourier Transform or an optimized signal processing is done to demodulate the RF signal. The goals of SR are fulfilled thanks to two major characteristics:

- The Fast Fourier Transform enables to switch from time to frequency domain. The entire RF spectrum is considered and any RF signal can be thus processed. The system is wideband.
- Discrete voltage samples guarantee the signal resolution.

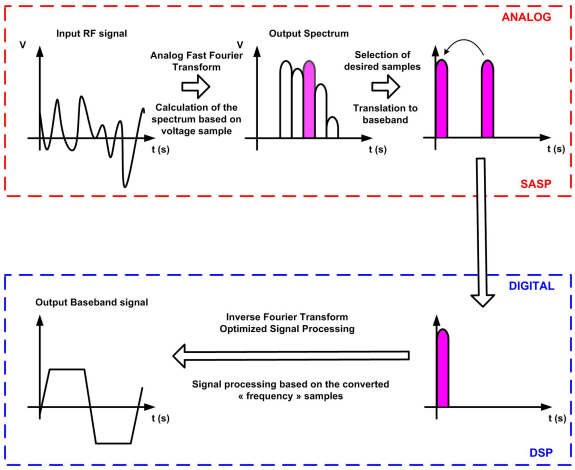

Fig. 2. Principle of Frequency Translation

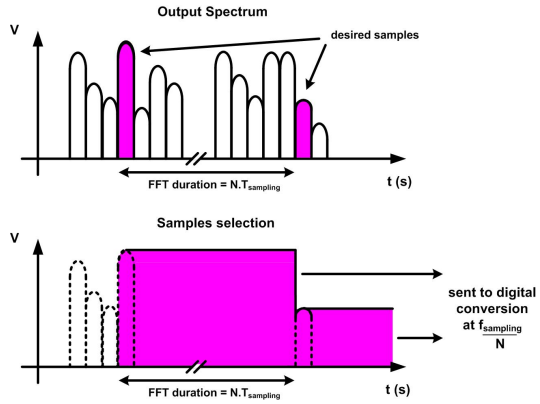

Fig. 3. Samples Selection

Their selection before the A/D conversion dramatically reduces the data rate and gives a low frequency conversion and a low working frequency of the DSP.

The samples selection (Fig. 3) at the output of the SASP can emphasize two applications:

- The frequency demodulation: as only the sample containing the modulated signal is selected, phase and amplitude information are extracted by removing the carrier. Some modulation can be directly processed such as phase modulation (PSK) by a reading of their phase shifting in their spectrum, amplitude modulation (QAM) or frequency modulation (FSK) [4], [5].
- The concurrent reception: the samples selection is not limited to a lonely RF envelope. Several envelopes can be processed at the same time by using common parameters. A direct application is to recover all the subcarriers of an OFDM modulation [6].

II. Circuit Design

An architecture was thus proposed to implement the DFT algorithm in order to process the frequency translation principle. A full SR system is given. [6] presents the study which is focused on the DFT part. Technical perspectives are also given on the RF-surrounding building blocks. A demonstrator of the SASP was designed with 65nm CMOS technology from STMicroelectronics and the prototype is here presented for the first time. 64 voltage samples are handled by this circuit. Future versions will process 65536 voltage samples [5].

A Track and Hold (T/H) sampler pre-discretizes the signal and displays the voltage samples to the FFT circuit. Sampling is the most important part of the system because the resolution of the calculation depends on its accuracy. The sampling frequency $f_{sampling}$ determines the FFT timing ($64.f_{sampling}$), the spectrum range (from 0 Hz to $\frac{f_{sampling}}{2}$) and the spectrum resolution ($\frac{f_{sampling}}{64}$).

Once sampled, the signal is windowed. In fact, the range of the data processing is limited to the number of stored samples N. The boundaries of the processed signal are abrupt. Turning data abruptly "on" and "off" has an undesired effect on the spectrum. This effect is reduced thanks to a weighting function called window. In our case, the window period considered is equal to $64.T_{sampling}$ and is synchronized on the FFT processing period. Different kinds of windows can be applied on the sampled signal [7], [8]. A choice is made to maximize the FFT accuracy as the window is hard-implemented in the circuit and cannot be modified. The Hamming window (Eq. 1) is the best compromise in term of bandwidth and loss as it provides a moderate frequency resolution and a moderate scallop loss. It is hard-implemented to window received RF signal in the SASP.

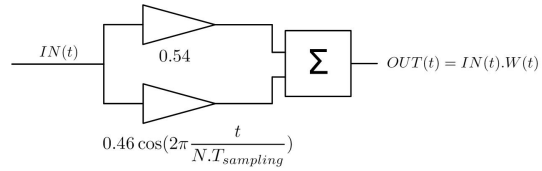

Fig. 4. Window function

$$W(t) = 0.54 + 0.46\cos(2\pi\frac{t}{64.T_{sampling}}) \quad (1)$$

The windowed signal is processed by the analog DFT [6]. Basic analog operations are carried out on voltage samples to display the spectrum. Three operations on voltage samples are done in series: delay, addition and weighting. Their combination gives the DFT calculation. These operations are also used to perform the windowing. A block is designed to window the input signal (Fig. 4). It uses weighting and addition.

Weighting operation is performed by applying a factor within the interval $[0, 1]$ which corresponds to $0.46.\cos(2\pi\frac{t}{64.T_{sampling}})$. The principle of the voltage/current/voltage conversion presented in [6] is used to carry out this analog operation. An extended switch network (S_x) connected to 16 transistors is proposed. It selects the input voltage of each transistor (M_x) gate which has a different ratio (W_x/L) (Fig. 5). The input voltage can be either a voltage sample to be weighted or the DC reference voltage (800mV). Consequently, the current crossing each transistor is proportional to the width of the selected transistors. Table I shows the configuration to carry out any 16 coefficients. Behavioural simulation is exhibited in figure 6 to illustrate this signal processing. The input signal is a constant voltage of 100mV. The output is the expected Hamming window itself.

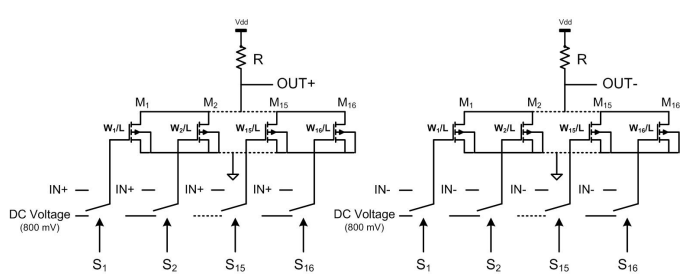

Fig. 5. Coefficients generation (simplified schematic)

TABLE I

WINDOW COEFFICIENTS APPLICATION

Switch Network Configuration					Coefficients			
S_1	S_2	$\cdots$	S_{15}	S_{16}				
Transistor Characteristics					For a 100mV input voltage sample (simulation)			
M_1 $\frac{W_1}{L} = 2.1$	M_2 $\frac{W_2}{L} = 6.5$	$\cdots$ $\cdots$	M_{15} $\frac{W_{15}}{L} = 43.4$	M_{16} $\frac{W_{16}}{L} = 43.8$	0.46. $cos(2\pi.nk)$	Output Output	Effective Coefficient	Error Error
DC	DC	$\cdots$	DC	DC	0	0	0	0%
DC	DC	$\cdots$	DC	IN	0.045	11.65mV	0.0452	0.33%
DC	IN	$\cdots$	IN	IN	0.458	117mV	0.453	1%
IN	IN	$\cdots$	IN	IN	0.46	118.7mV	0.46	0%

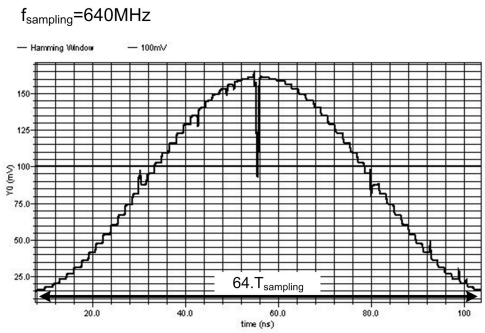

Fig. 6. Behavioural simulation of a Hamming Window

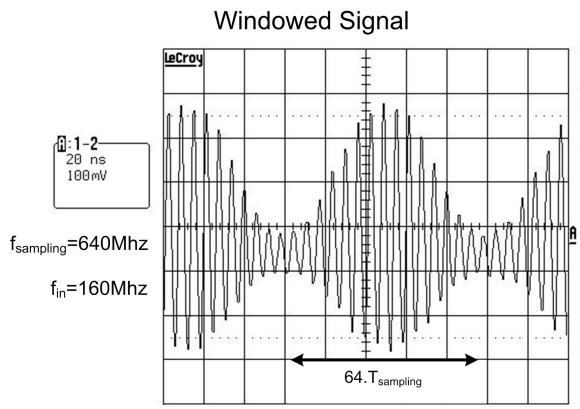

Fig. 8. Measured hamming window

III. MEASURES

A circuit was sent to foundry (Fig. 7). Its die area is $1.44mm^2$ with an active area of $0.13mm^2$. Measures were performed on the windowing unit to validate weighting and addition of voltage samples. A sinewave at the frequency of $f_{in} = 160MHz$ was windowed with a sampling frequency of $f_{sampling} = 640MHz$ (Integer numbers were chosen for a matter of simplicity). Figure 8 exhibits the windowed input signal and confirms the feasibility of discrete analog operations at high frequencies.

Measures of the whole circuit were performed on a sinewave. The sampling frequency is $f_{sampling} = 320MHz$. The input signal is given by $f_{in} = 150.01MHz$. Figure 9 exposes how the SASP shifts any RF signal into baseband. The only voltage sample containing the desired band is selected. As the signal frequency is not an entire number of the sampling frequency, the output of the SASP displays a signal with a frequency of $f_{out} = f_{in} - \frac{n.f_{sampling}}{64} = 10kHz$ where $n = 30$. It is just a matter of selecting the correct voltage sample to switch from one RF band to others. Figure 10 depicts the shifted signal with a measured $f_{out} = 10kHz$. If the number of samples and the sampling frequency are high enough, the spectrum accuracy can be guaranteed to process any RF signals. Consequently, the output frequency of the SASP is dramatically lowered and all the constraints of ADC and DSP are fully relaxed. The SR becomes feasible which is much more efficient than usual Software-Defined Radio (SDR). The principle of concurrent reception is also proven.

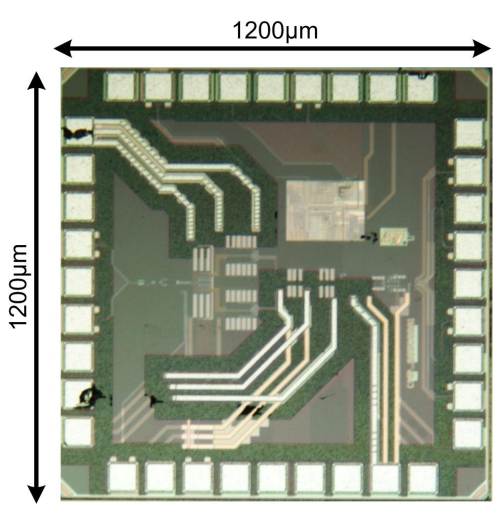

Fig. 7. Die Photography

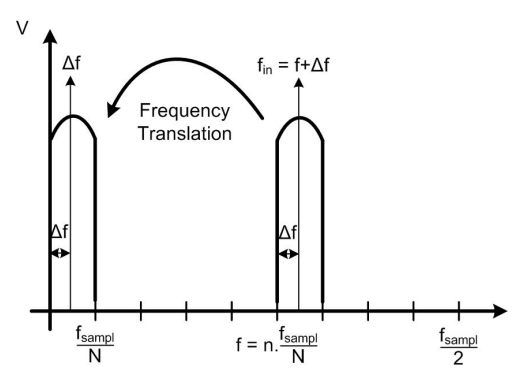

Fig. 9. Frequency Shifting

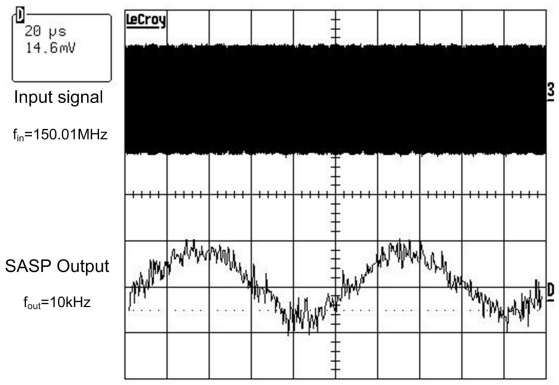

Fig. 10. Measure of frequency Shifting

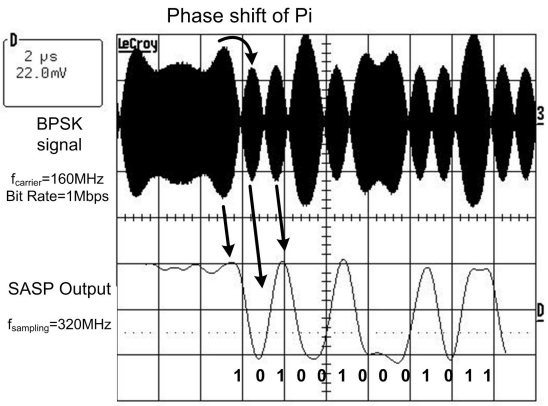

Fig. 11. BPSK modulation

Measures went on digital modulations. They are the best example of the possibilities offered by the SASP. [4] presents the case of a BPSK modulation. Figure 11 presents a BPSK modulated signal processed by the SASP. The sampling frequency is $f_{sampling} = 320MHz$. The input signal is given by $f_{in} = 160MHz$ and a bit rate of $1Mbps$. FFT timing is scaled exactly on the bit rate, i.e. $10MHz$ which is an entire number of the bit rate. 10 successive FFT are able to process one bit. As the spectrum is directly an image of the phase, it is easy to consider that the SASP process a direct demodulation. It removes the carrier of any RF signal. The principle of frequency demodulation is proven.

IV. Conclusion

For the very first time in this paper, a demonstrator of the SASP has been designed and measured. It handles 64 voltage samples to perform a FFT on RF signal to fulfill the Software Radio concept for mobile terminals. The power consumption is 389mW with a power supply of 1.2V. The maximal frequency of operation is 1.2GHz. This characteristic should be dramatically lowered thanks to an overall circuit optimization, which was not brought into play in this demonstrator. The SASP has demonstrated the feasibility of analog signal processing for RF applications and how the technical bottleneck of the ADC and DSP is solved. It paves the way to an industrial implementation which is expected to process 65536 samples at 10GHz at low power consumption.

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