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# A Baseband Ultra-Low Noise SiGe:C BiCMOS 0.25 $\mu\text{m}$ Amplifier And Its Application For An On-Chip Phase-Noise Measurement Circuit

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**Abstract**—The design and realization of an ultra-low noise operational amplifier is presented. Its applications are integrated low-frequency noise measurements in electronic devices and on-chip phase-noise measurement circuit. This paper discusses the SiGe:C BiCMOS 0.25  $\mu\text{m}$  design improvements used for low noise applications. The proposed three-stage operational amplifier uses parallel bipolar transistor connection as input differential pair for low noise behavior. This operational amplifier provides both low noise and high gain performances. This operational amplifier has an area of only  $660 \times 250 \mu\text{m}^2$  with an equivalent input noise floor of only  $1.1 \text{ nV}/\sqrt{\text{Hz}}$  square root at 10 kHz. The measured noise characteristics (versus total power consumption) are better than those of most operational amplifiers commonly adopted in low-frequency noise measurements. The AC gain is 83 dB and the unity gain bandwidth is 210 MHz, with a total current consumption of 18 mA at 2.5 V supply voltage.

## I. INTRODUCTION

The operational amplifier is the most widely used of all linear circuits in production today, in various areas such as consumer, industrial, and scientific. The presented low noise amplifier has been designed especially for noise measurements [1], and has been integrated in an on-chip phase-noise measurement circuit as shown in Fig. 1. In fact, many high

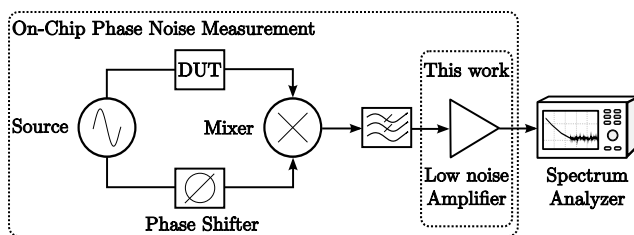


Fig. 1. Integrated phase-noise measurement system

precision instruments such as instrument amplifier require a very high open loop gain and ultra low input noise to achieve the required signal to noise ratio. In these instrumentation applications, the amplifier input noise voltage is the most important parameter. Several operational amplifiers are available with noise voltages below  $3 \text{ nV}/\sqrt{\text{Hz}}$  [2] and a few are available with noise voltage in the range of  $2 \text{ nV}/\sqrt{\text{Hz}}$  [3].

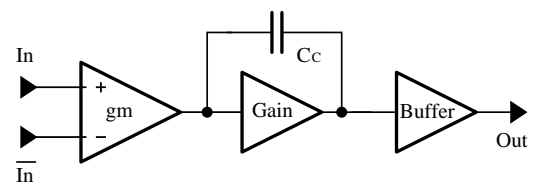


Fig. 2. Three-stage amplifier

A high gain operational amplifier usually consists of the basic stages shown in Fig. 2, in which the input differential voltage is  $V_{\text{In}} - \overline{V}_{\text{In}}$  and the single-ended output voltage is  $V_{\text{Out}}$ . The input stage must have low noise behaviour with both high voltage gain and a high common-mode rejection ratio. As a result, external parasitic signals are rejected since they are seen common mode. The second stage exhibits a high gain  $G_1$  and includes a local compensation capacitor  $C_c$  [4].

The motivation of this paper is to minimize noise in operational amplifier by appropriately choosing a topology together with components parameters. In section II of this paper, noise considerations are discussed and the operational amplifier design is proposed. Finally, section III is dedicated to the measurements performed on the realized circuit.

## II. NOISE ANALYSIS AND LOW NOISE OPAMP DESIGN

In the design of low noise operational amplifiers, the inherent limitations of monolithic devices impose severe restrictions on possible design approaches: the most significant design restriction is the input referred voltage noise floor. This noise can be calculated using the following expression (1), where  $k$  is the Boltzmann constant,  $r_b$  the base resistor,  $r_e$  the emitter resistor,  $I_b$  the base current and  $T$  the temperature [5], [6]. This expression is valid to describe the voltage noise floor at the bipolar transistor input:

$$S_v \approx 4kT(r_b + r_e) + 2qI_b(r_b + r_e)^2 \quad (1)$$

Operational amplifier design for baseband analog circuits has achieved higher voltage gain, better input noise and input offset performances with bipolar transistors than with CMOS

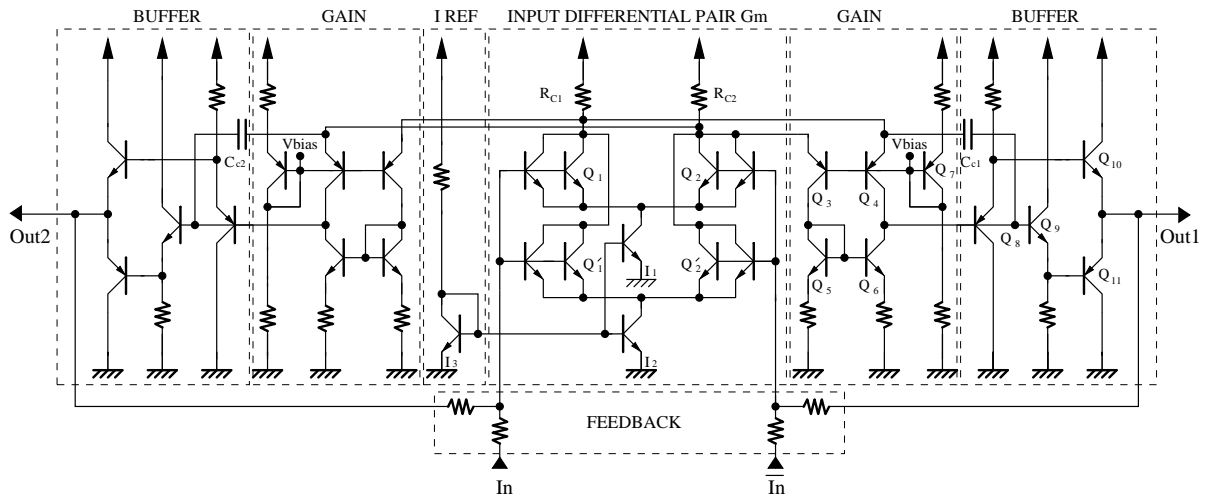


Fig. 3. Simplified low noise operational amplifier design

transistors at identical bias current. Indeed, bipolar transistors have a much larger transconductance and a smaller flicker noise than MOSFET. This operational amplifier has been fabricated in a BiCMOS SiGe:C 0.25  $\mu\text{m}$  process with a specific careful design on the input stage as it is the main contributor for the total noise.

Bipolar transistor noise at low frequency (approximately from 10 Hz to 10 kHz) is mainly due to Flicker noise, also called  $1/f$  noise. It is caused mainly by traps (contamination or crystal defects) at the emitter silicon interface. These traps capture and release carriers in a random fashion and give rise to a noise signal with a  $1/f$  dependence [7]. This noise is detected on the base current  $I_b$  and can be measured through a power spectral density  $S_{iB}$  [6].

A simplified schematic of our operational amplifier is shown on fig. 3 with the stages previously mentioned.

has been chosen to conciliate both low noise behaviour and sufficient gain. To further reduce the noise behaviour, each transistor of the differential pair is duplicated four times, as shown in Fig. 5. Transistor noise fluctuations reduce with

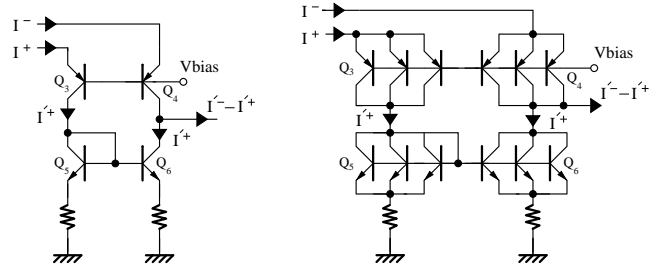


Fig. 6. Simplified current mirror Fig. 7. Low noise purpose implementation from fig. 6

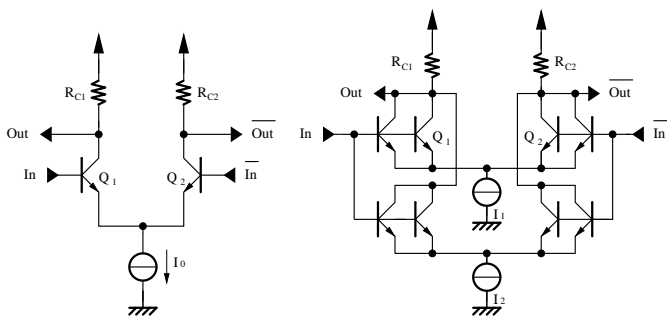


Fig. 4. Differential input stage Fig. 5. Low noise purpose implementation from fig. 4

Fig. 4 and Fig. 5 show more precisely the input differential stage of the operational amplifier. It consists of two differential transistors  $Q_1$  and  $Q_2$  which convert the input differential voltage  $V_{in} - \overline{V}_{in}$  to a differential output voltage  $V_{Out} - \overline{V}_{Out}$ . The loads in the transistor collectors have been chosen as resistors instead of a NPN current mirror because of the noise behaviour, crucial in this first stage. The value of the resistors

increasing area, and thus, the bipolar parallel connection reduces the total base resistance ( $r_b$ ), which improves the noise performances, as shown in equation (1). An increase of emitter area involves an increase of current consumption (to work at same current density) by enlarging the current source.

A second stage, a gain stage, is realized with a NPN current mirror  $Q_5, Q_6$ . This current mirror could have been a PNP mirror as the load of the differential pairs in the first stage, but as we replace it with the less noisy resistors  $R_{C1}$  and  $R_{C2}$ , it is now used in the second stage. Also, a cascode-like structure is used with further common base  $Q_3$  and  $Q_4$  PNP transistors, which improves gain of this second stage as well as reverse isolation with previous stage. As in the first stage, the transistors have been duplicated as shown in Fig. 7, to minimise the noise behaviour.

Fig. 3 also shows a capacitor  $C_c$  that ensures sufficient phase and gain margins for the close-looped stability by splitting dominant pole locations. The output and third stage of this operational amplifier provides impedance matching by presenting high input impedance to the previous stage and low output impedance to the load, and uses two common

collectors to avoid crossover distortion. To avoid degrading high frequency performance, the output stage is designed to have low input capacitance and wide bandwidth.

### III. CIRCUIT IMPLEMENTATION AND MEASUREMENTS

The proposed ultra-low noise operational amplifier has been implemented in STMicroelectronics 0.25  $\mu\text{m}$  BiCMOS SiGe:C process that provides HBT with a transition frequency of about 70 GHz.

The amplifier has been integrated in the closed-loop configuration presented in Fig. 3, thus no open-loop measurement results are available. We will show measured closed-loop and simulated open-loop characteristics.

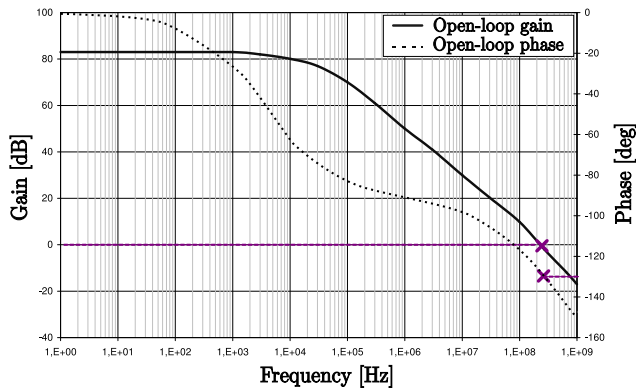


Fig. 8. Simulated open-loop frequency performances of this operational amplifier

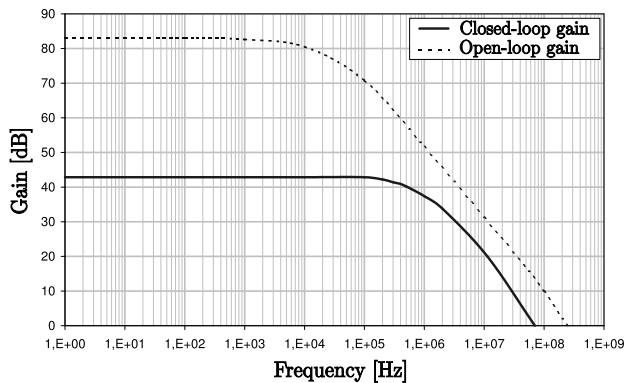


Fig. 9. Measured closed-loop frequency performances of this operational amplifier

As shown in Fig. 8, the unity gain bandwidth (UGB) of this operational amplifier is 210 MHz with 51 degrees phase margin. The AC open-loop gain is 83 dB. The closed-loop performances are given in Fig. 9. The Fig. 10 shows the measured input voltage noise performances:  $e_n = 1.7 \text{ nV}/\sqrt{\text{Hz}}$  @ 1 kHz, a very low input voltage noise floor of  $1.1 \text{ nV}/\sqrt{\text{Hz}}$  @ 10 kHz, and the  $1/f$  corner frequency of about 7 kHz. These measurements have been performed on a noise measurement setup with a detection noise floor of  $0.6 \text{ nV}/\sqrt{\text{Hz}}$  @ 1 kHz, available at LAAS facilities. Fig. 11 is taken from [3] and

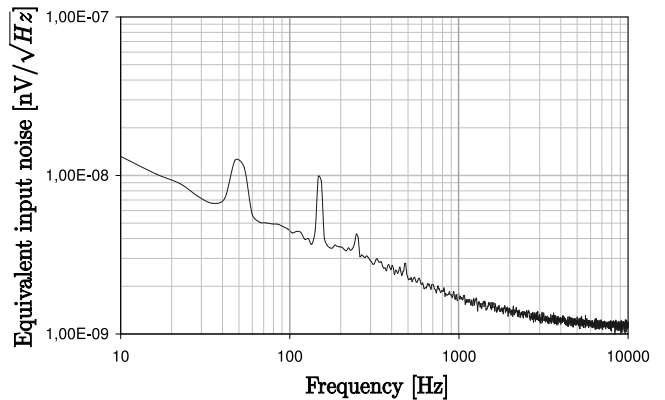


Fig. 10. Measured input referred voltage noise

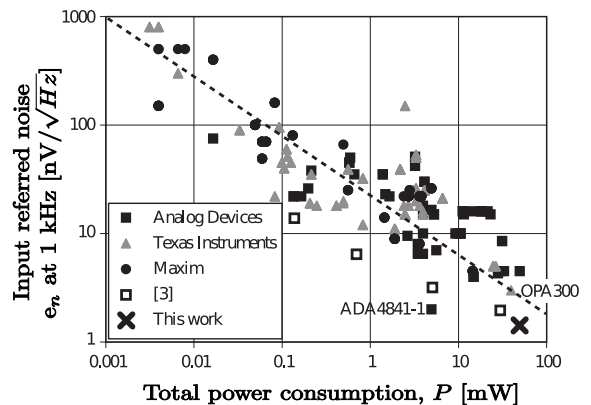


Fig. 11. Comparison of this work with state-of-the-art operational amplifiers versus total power consumption

makes a comparison with state-of-the-art low noise voltage operational amplifiers. The presented work is following the general trend high lighted by this graph, while reporting the lowest equivalent input noise versus power consumption presented so far by integrated amplifiers. To evaluate the linearity, the second order harmonic amplitude is simulated to be at about  $-56 \text{ dBc}$  with 100 kHz input frequency, and measured to be at  $-50 \text{ dBc}$  (Fig. 12). The 3<sup>rd</sup> order harmonic is situated in the measurement set-up noise floor.

The die microphotograph is shown in Fig. 13. The chip size (without probe PADs) is  $660 \times 250 \mu\text{m}^2$ . Its DC consumption is 45 mW and operates from a 2.5 V supply. Table I compares the presented work with best-in-class instrumentation amplifiers recently published.

### IV. CONCLUSION

An ultra-low noise operational amplifier using a optimized design in a 0.25  $\mu\text{m}$  BiCMOS SiGe:C process has been presented in this study. The fabricated compact operational amplifier has a area of only  $660 \times 250 \mu\text{m}^2$  with a equivalent input noise floor near to only  $1.1 \text{ nV}/\sqrt{\text{Hz}}$  @ 10 kHz. The measured noise characteristics are better than most of state-of-the-art baseband amplifier commonly adopted in low-frequency noise measurements. The input referred voltage noise versus

TABLE I  
COMPARAISON OF THIS WORK WITH STATE-OF-THE-ART OPERATIONAL AMPLIFIERS

Performances	Process	DC Gain	Phase Margin	Gain-Bandwidth	Consumption	THD	$E_n$
[3]	0.35 $\mu\text{m}$ CMOS	—	20	39 MHz	30 mW	—	2 nV/ $\sqrt{\text{Hz}}$
[8]	1.5 $\mu\text{m}$ CMOS	39.5 dB	55	7.2 kHz	80 $\mu\text{W}$	69 dB	2.2 $\mu\text{V}/\sqrt{\text{Hz}}$
[9]	1.6 $\mu\text{m}$ CMOS	150 dB	—	400 kHz (UGB)	1mW	—	27 nV/ $\sqrt{\text{Hz}}$
[10]	0.18 $\mu\text{m}$ CMOS	58 dB	—	—	—	—	2.9 nV/ $\sqrt{\text{Hz}}$
<b>This Work</b>	<b>0.25 <math>\mu\text{m}</math> BiCMOS</b>	<b>80 dB</b>	<b>50</b>	<b>210 MHz (UGB)</b>	<b>45 mW</b>	<b>50 dB</b>	<b>1.1 nV/<math>\sqrt{\text{Hz}}</math></b>

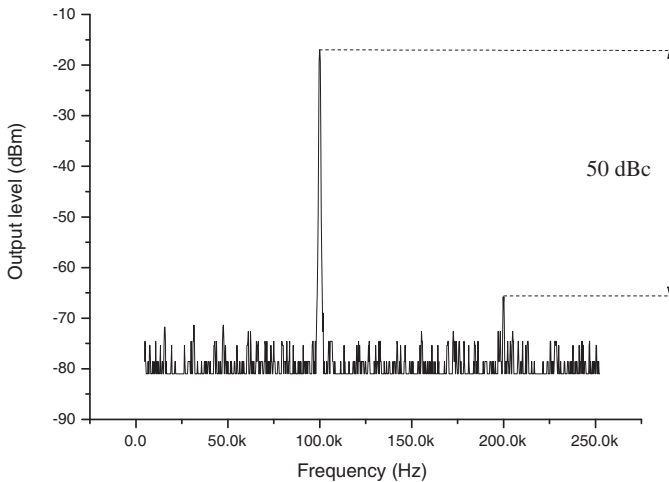


Fig. 12. Measured second harmonic value

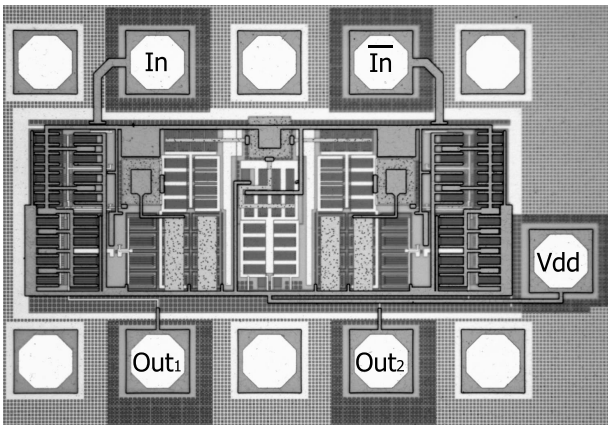


Fig. 13. Chip microphotograph

power consumption performance has been optimized through a careful choice of the topology and the active devices.

The circuit shows a 83 dB open-loop gain. This amplifier is well suited for low noise applications involving high speed circuits which can be integrated on the same wafer, such as an on-chip phase-noise measurement circuit or an microwave power sensor.

#### V. ACKNOWLEDGEMENTS

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#### REFERENCES

- [1] L. Carloni, F. De Bernardinis, A. Sangiovanni Vincencentelli, and M. Sgroi, “The art and science of integrated system design,” in *Proc. Proceeding of the 32nd European Solid-State Device Research Conference*, 24–26 September 2002, pp. 19–30.
- [2] Z. Li, J. Ma, M. Yu, and Y. Ye, “Low noise operational amplifier design with current driving bulk in 0.25/ $\mu\text{m}$  cmos technology,” in *Proc. 6th International Conference On ASIC ASICON 2005*, vol. 2, 24–27 Oct. 2005, pp. 630–634.
- [3] C. Bronskowski and D. Schroeder, “An ultra low-noise cmos operational amplifier with programmable noise-power trade-off,” in *Proc. 32nd European Solid-State Circuits Conference ESSCIRC 2006*, Sept. 2006, pp. 368–371.
- [4] A. B. Grebene, *Bipolar and MOS analog integrated circuit design*, J. Wiley and Sons, Eds. Micro-linear corporation, 1983.
- [5] T. G. M. Kleinpenning, “Location of low frequency noise sources in submicrometer bipolar transistors,” in *IEEE Trans. On Elec. Dev.*, vol. 39, June. 1992, pp. 1501–1506.
- [6] J. Brini, “Low frequency noise spectroscopy in mos and bipolar devices,” *Microelectron. Eng.*, vol. 40, no. 3-4, pp. 167–179, 1998.
- [7] A. Mounib, G. Ghibaudo, F. Balestra, D. Pogany, A. Chantre, and J. Chroboczek, “Low frequency ( $1/f$ ) noise model for the base current in polysilicon emitter bipolar junction transistors,” *Journal of Applied Physics*, vol. 79, no. 6, pp. 3330–3336, 1996. [Online]. Available: <http://link.aip.org/link/?JAP/79/3330/1>
- [8] R. Harrison and C. Charles, “A low-power low-noise cmos amplifier for neural recording applications,” *IEEE Journal of Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, 2003.
- [9] A. Bakker, K. Thiele, and J. Huijsing, “A cmos nested-chopper instrumentation amplifier with 100-nv offset,” *IEEE Journal of Solid-State Circuits*, vol. 35, no. 12, pp. 1877–1883, Dec. 2000.
- [10] I. Nam and K. Lee, “High-performance rf mixer and operational amplifier bicmos circuits using parasitic vertical bipolar transistor in cmos technology,” *Journal of Solid-State Circuits*, vol. 40, no. 2, pp. 392–402, 2005.