A Low Phase Noise and Wide-Bandwidth BiCMOS SiGe:C 0.25μm Digital Frequency Divider For An On-Chip Phase-Noise Measurement Circuit

Sylvain Godet, Éric Tournier, Olivier Llopis, Andreia Cathelin, Julien Juyon

A Low Phase Noise and Wide-Bandwidth BiCMOS SiGe:C 0.25µm Digital Frequency Divider For An On-Chip Phase-Noise Measurement Circuit

S. Godet[1,2], É. Tournier[1,2], O. Llopis[1], A. Cathelin[3], J. Juyon[1,2]
[1] LAAS-CNRS; Université de Toulouse; 7, avenue du Colonel Roche, F-31077 Toulouse, France
[2] Université de Toulouse; UPS
[3] STMicroelectronics, Crolles, France
Email: sgodet@laas.fr

***Paper* — It is a student paper**

***Abstract* — A low phase noise and wide-bandwidth frequency divider has been developed in a 0.25 µm SiGe:C process. This paper discusses the BiCMOS design improvements used for ultra low phase noise applications like on-chip phase-noise measurement circuit. From a single-ended signal provided by a local oscillator LO, the wide-bandwidth frequency divider circuit generates accurate quadrature signals. For the full 1kHz-5.5 GHz input frequency range, the frequency divider achieves an output quadrature error less than ±1°. This paper presents a novel architecture designed for improving phase noise and exhibits a measured residual phase noise of –164 dBc/Hz @ 100 kHz with a 3.5 GHz input frequency.**

***Index Terms* — On-chip phase-noise measurement circuit, Silicon bipolar/BiCMOS process technology, RF analog circuits, low phase noise, frequency divider.**

I. Introduction

The frequency divider (FD) is an important building block in today's RFIC and microwave circuits mostly because it is an integral part of the phase-locked loop (PLL) circuit [1-3]. Quadrature generation techniques can be classified into either active or passive techniques. Active quadrature splitters, such as digital dividers, are popular [4]. Deviation from that frequency results in quadrature degradation, which can dramatically reduce system performance until it is unusable [5]. It is thus interesting to combine these two important functions, frequency divider and quadrature generator, in a single device. Compared to the traditional resistor and capacitor (RC) quadrature generation, this frequency divider approach is easier to implement, and offers smaller phase imbalance [6, 7]. Another important feature of such a device is in the phase noise it may add to the signal. It is thus mandatory to investigate on a circuit topology for which the noise conversions can be minimized.

The frequency divider is implemented in silicon bipolar technology and quadrature outputs are low phase noise. Its application scheme as phase shifter to an on-chip phase-noise measurement circuit is proposed. The circuit block diagram is shown in Fig. 1. This test bench is composed of an oscillator based on a resonator with a strong Q-factor and exhibits an ultra low phase noise and an accurate stability. The typical method used to measure phase noise involves a single mixer that is driven by sources on its RF and LO ports. The IF port is then low pass filtered and amplified before it is connected to a spectrum analyzer or FFT. The noise floor of this technique is highly dependent upon the performances of the quadrature generation circuit, the mixer and amplifier. The phase detector (typically a double balanced mixer) is used to convert phase fluctuations which are then displayed on a spectrum analyzer. This test bench worked with fully differential circuits, the mixer operating mode has to be set up with a quadrature between its ports. The phase difference between the four mixers ports has to be 0°, 180° and 90°, 270° respectively.

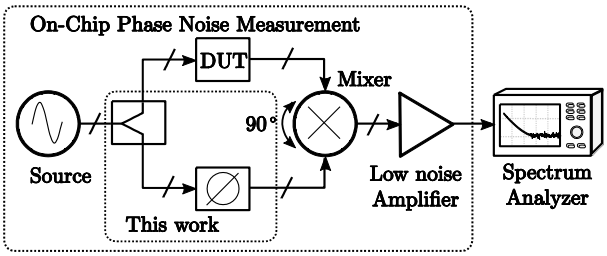

Figure 1. Integrated phase-noise measurement system

The emphasis is put on the phase noise reduction techniques.

II. Devices and technology

In the design of wide-bandwidth high-frequency dividers, more especially for low phase noise applications, the inherent limitations of monolithic devices impose severe restrictions on possible design approaches: the most

significant design restriction is the transistor phase noise. Typically, for the same area, the bipolar transistors exhibit better phase noise than MOS transistors. The circuit has been fabricated in a 70 GHz STMicroelectronics BiCMOS SiGe:C 0.25 µm. Proper sizing of the transistors in this configuration results in a reasonable speed and phase noise trade-off at gigahertz rate.

III. Frequency divider architecture

The block diagram of the traditional frequency divider is shown in Fig. 2. It consists of two latches in a negative feedback loop [1].

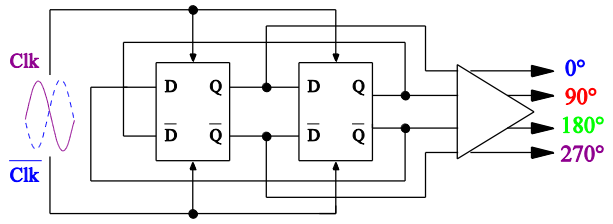

Figure 2. Frequency divider-by-two based on D-latches

The frequency divider is composed of two basic D-latches cascaded. The implementation of the latches depends on the available type of transistors, but a current-steering topology consisting of a differential pair and a regenerative pair achieves high speed in both bipolar and CMOS technologies [3]. The divider configuration generates accurate quadrature phases at 0, 90, 180 and 270° terminals, as shown in Fig. 2. This frequency divider operates both with differential signal input or single-ended input thanks to a differential stage before the divided-by-two circuit.

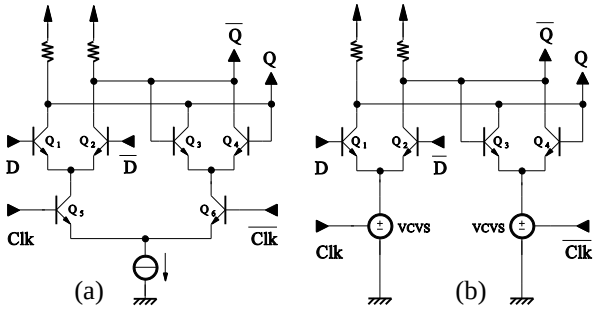

Figure 3. Basic implementation (a) and optimized D-latch implementation (b)

In order to get a divided-by-two circuit the Q and terminals are respectively connected to the D and terminals of the second D-latch. The basic configuration is composed of a double differential current-divider circuit shown in Fig. 3a. In this case the lower differential pair is driven by the differential input signal, and the differential D signal is applied to the bases of the upper differential pairs. The differential voltage (Clk, $\overline{\text{Clk}}$) controls which differential pair will be activated. D-latch is duplicated once to obtain a divider-by-two circuit as shown in Fig. 4. Data-input are driven by the negative output of the flip-flop which changes its state on each rising-edge of the flip-flop clock input. The output signal of the first stage generates the signal input for the next one.

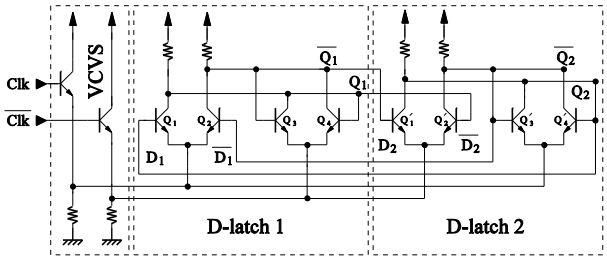

Figure 4. Optimized frequency divider with simplified D-latch implementation

Our main effort has thus been focused on developing a new topology for low phase noise latch. High-speed latches in wireless communications are usually designed using current-mode logic. To improve the phase noise performances, it was necessary to investigate on a special D-latch topology, as shown in Fig. 3b. In fact the circuit phase noise is mainly related to the D-latch design. Thus the current source of the bottom differential pair (Q5 and Q6), typically designed with a MOS current source, has been substituted by a bipolar transistor (Fig. 3a) in a first approach, and then by a voltage controlled voltage source (VCVS) in a second approach. This VCVS controls the D-latch upper differential pair emitters with a low impedance, which reduces the noise contribution at the emitters of the differential pairs. As shown in Fig. 4, a common collector is used as VCVS for each input signal. Output signals of the quadrature generator is represented by $Q_1, \overline{Q_1}$ and $Q_2, \overline{Q_2}$ respectively.

IV. Device realization and measurements

A. Measurements and simulations

The outputs signals of the active quadrature splitter are then equalized in magnitude. As shown in Fig. 5, the Fig. 4 produces an accurate quadrature relationship for the whole bandwidth, thanks to the perfect symmetry of the circuit. Because the input frequency is twice the output frequency this circuit cannot be used as a simple quadrature generator. Concerning the frequency performance of the circuit, it is directly related to the circuit main block which is the D-latch. Consequently, a high-speed latch automatically results in a high-speed divided-by-two circuit.

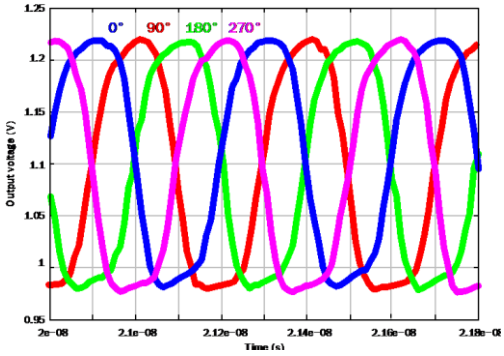

Figure 5. Measured output time responses @ 5 GHz input frequency

This particular structure allows low phase noise high-performance divider circuits, as shown in Fig. 6, with a phase noise level of –164 dBc/Hz at 100 kHz offset with a 3.5 GHz input signal frequency. In fact, this represents an improvement of phase noise of about 15 dB compared to the classical topology. The level of the phase noise floor is also dependent on the input signal frequency. In fact, as shown in Fig. 7, the noise floor increases lightly with the input frequency. To get these phase noise characteristics, transistors sizing was very important. Indeed the emitter area affects directly the minimum phase noise level. We have demonstrated that the phase noise floor decreases if the emitter area increases, as shown in Fig. 8, with a current density Jc/Area constant. Our optimized D-latch is composed of bipolar transistors with 12 µm² emitter area with 3 fingers, 2 collectors and 4 bases.

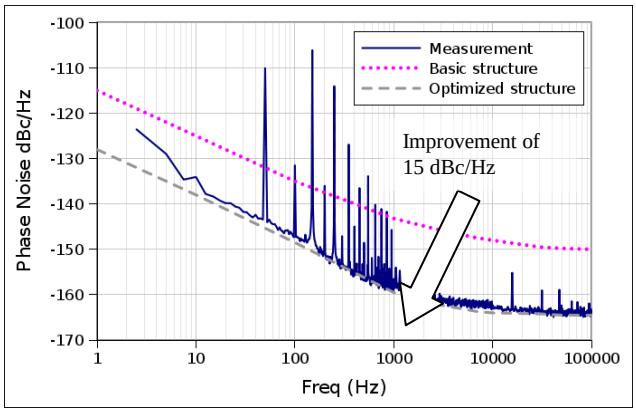

Figure 6. Residual phase noise measurement @ 3.5 GHz input frequency versus simulated results of basic and optimized FD

In preliminary on-wafer measurements with external clock inputs, successful operation of these circuits has been demonstrated for the full 1 kHz-5.5 GHz frequency range, with a supply of 2.5 V and with a power consumption of 53 mW.

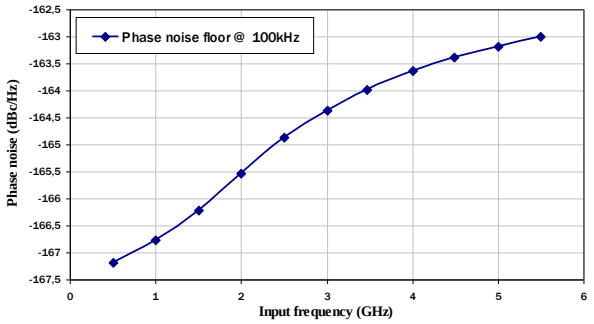

Figure 7. Predicted phase noise floor versus input frequency

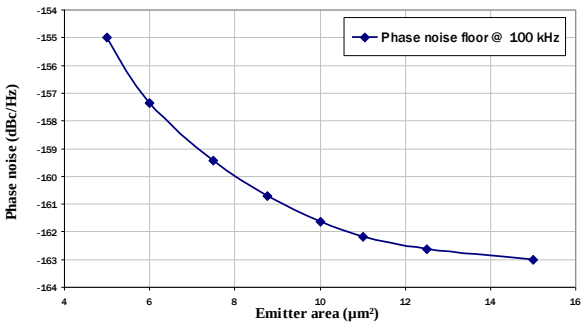

Figure 8. Predicted phase noise floor versus emitter area at 5.5 GHz input frequency

The consumption can be decreased with a diminution of the emitter area (with the same current density versus emitter area), with an increase of the level of the residual phase noise floor.

B. Layout considerations

In a monolithic low phase noise circuit, the input differential transistor pair is the key of the circuit performance. Therefore, the design and layout of the low phase noise transistors require additional care and attention. To obtain a very low phase noise level, it is necessary to increase the bipolar transistor areas, and increase current biasing respectively. It is necessary to make a compromise between the residual phase noise floor and the maximum operating frequency. The study presented here has been designed to obtain the minimum residual phase noise. The current injection occurs along the edge or periphery of the emitter. To increase the emitter periphery and to minimize the biasing effects due to base-spreading resistance, one normally uses an interdigitated structure for the emitter and base regions. The presence of bipolar transistor with a large area in a close proximity to the low-level signal-processing and control circuitry can require additional layout precautions.

The device serves as a concentrated heat source and can cause thermal gradients within the chip [8, 9].

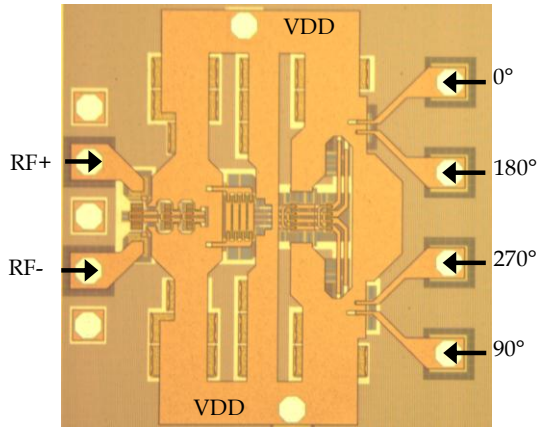

Figure 9. Chip photograph of low phase noise frequency divider 1150 x 1150 µm²

TABLE I. EXEMPLES OF SYSTEMS USING FREQUENCY DIVIDERS

Ref	Ciruit Type	Device Process	Operation Frequency	Phase Noise	Power Dissipation
[10]	BiCMOS	0.25µm	10 GHz	–115 dBc/Hz @ 1 MHz	16.25 mW
[11]	BiCMOS	65nm	11.8 GHz	–157.7 dBc/Hz @ 20 MHz (simulated)	14.5 mW
[12]	BiCMOS	0.25µm	5 GHz	–112 dBC/Hz @ 1MHz	142 mW
This Work	**BiCMOS**	**0.25µm**	**1kHz - 5.5 GHz**	**–163 dBc/Hz @ 100 kHz**	**53 mW**

IV. Conclusion

In this paper, a wide-bandwidth and low noise frequency divider with quadrature outputs is described. The phase noise performance has been optimized through a careful choice of the topology and of the active devices. This device is used in an on-chip phase noise measurement circuit .The circuit operation has been verified on the 1 kHz-5.5 GHz frequency range. The residual phase noise performances have been measured, –164 dBc/Hz @ 100 kHz with a 3.5 GHz input frequency.

Acknowledgement

This work has been performed in the frame of the European contract IST n. 0270003 “MOBILIS”. We would like to thank our partners of this consortium for fruitful discussions.

References

[1] B. Razavi, “RF Microelectronics” Upper Saddle River, NJ: Prentice-Hall, 1998, pp. 290-295

[2] R. Dehgahani and S. M. Atarodi, “A low power wideband 2.6 GHz CMOS injection-locked ring oscillator prescaler,” in *Proc. RFIC Symp.*, Philadelphia, PA, Jun. 8–10, 2003, pp. 659–662.

[3] A. Bonfanti, A. Tedesco, C. Samori and A. L. Lacaita, “A 15-GHz Broad-Band ÷2 Frequency Divider in 0.13 µm CMOS for Quadrature Generation”, *IEEE Microwave and wireless components letters*, vol. 15, no. 11, pp. 724-726, Nov. 2005.

[4] Y. H. Chun, J. R. Lee, S. W.Yun, and J. K. Rhee, “Design of an RF low-noise bandpass filter using active capacitance,” *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 2, pp. 687–695, Feb. 2005.

[5] S. Verma, H. R. Rategh, and T. H. Lee, “A unified model for injection-locked frequency dividers,” *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 1015–1027, Jun. 2003.

[6] R. Mohanavelu and P. Heydari, “Novel ultra high-speed flip-flop-based frequency divider,” in *Proc. Int. Symp. Circuits Syst. (ISCAS’04)*, May 2004, vol. 4, pp. 169–172.

[7] H. M.Wong, “A 1.8-V 3-mW 16.8-GHz frequency divider in 0.25-_m CMOS,” in *Tech. Dig. IEEE Int. Solid-State Circuits Conf. (ISSCC’00)*, Feb. 2000, pp. 196–197.

[8] Gray P. R., and Hamilton D.J., “Analaysis of electrothermal integrated circuits”, *IEEE J. Solid State Circuits*, vol. SC-6, pp. 8-14, 1971

[9] Sato T., Ichimiya J. Ono N., Hachiya K., Hashimoto M., “On-chip thermal gradient analysis and temperature flattening for SoC design”, *Design Automation Conference 2005, proceedings of the ASP-DAC 2005. Asia and South Pacific*, vol. 2, pp. 1074-1077, Jan. 2005.

[10] F. Herzel, W. Winkler and J. Borngräber,“An Integrated 10 GHz Quadrature LC-VCO in SiGe:C BiCMOS Technology for Low-Jitter Applications”, *IEEE Custom Integrated Circuits Conference*, 2003, pp. 293-296.

[11] R. Prakash, S. Akhtar, P.T. Balsara, ”Phase noise reduction in high speed frequency divider”,*IEEE Design, Applications, Integration and Software*, Oct. 2006, pp.83-86.

[12] K. Schmalz, F. Herzel and M. Piz, “An Integrated 5 GHz Wideband Quadrature Modem in SiGe:C BiCMOS Technology”, *Proceedings of the 36th European Microwave Conference*, Sept. 06, pp.1656-1659.