Integration of PtSi in p-type MOSFETs using a sacrificial low-temperature germanidation process

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Integration of PtSi in p-Type MOSFETs Using a Sacrificial Low-Temperature Germanidation Process

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***Abstract*—In this letter, an original selective etching method of Pt with respect to PtSi using a sacrificial low-temperature germanidation process is used for the integration of valence band edge contacts in p-type MOSFET devices. After silicidation annealing, the excess of Pt due to incomplete reaction with silicon or standing on insulating layers can be transformed into the $PtGe_2$ phase. The solubility of this phase in a sulfuric peroxide mixture (SPM) without altering PtSi is demonstrated. The suitability and scalability of the proposed integration scheme is shown through the successful integration and characterization of PtSi source/drain contacts in p-type MOSFETs.**

***Index Terms*—Etching, platinum, Schottky barriers, semiconductor-metal interfaces, silicon.**

I. Introduction

PLATINUM Silicide (PtSi) is very attractive for the future very-large-scale integration (VLSI) technologies as a contact silicide for submicrometer p-MOSFETs because of its low barrier height to p-type Si, low-silicon consumption, and low-temperature of formation [1]. The integration of a contact silicide requires a self-aligned selective etching process in order to remove the excess metal remaining after the silicidation annealing, without altering the silicide phase. For this purpose, aqua regia (AR) is commonly used to integrate PtSi in MOSFET devices. However, it was highlighted that AR is not a suitable solution unless a high-temperature (around 600 °C) oxidization step of PtSi is realized in order to form an ∼5-nm-thick SiO_2/PtSi protective overlayer [2]–[4].

As the oxidization reaction requires a silicon reservoir coming from the silicide phase, this process is hardly applicable to very thin PtSi layers integrated as source and drain contacts, because it can alter the PtSi/Si contact resistance, and severely increase the silicide sheet resistance (Rs).

Furthermore, the introduction of a high-*k*/metal gate stack at the 32 nm technology node brings tight constraints associated with the thermal budget and the chemical steps involved after the gate definition. In that context, AR cannot be envisioned as a viable solution due to its extreme reactivity with most metals and silicon alloys. In contrast, we report in this letter a new selective etching method of Pt with respect to PtSi using a sacrificial low-temperature germanidation process and a conventional chemistry based on sulfuric peroxide mixture (SPM). We demonstrate that this original process enables the safe integration of thin PtSi layers through the fabrication and characterization of p-type MOSFETs featuring promising electrical characteristics.

II. Sacrifical Germanidation

Self-aligned silicidation involves the removal of metal in excess either due to partial Pt consumption on silicon areas or due to unreacted Pt over an insulating film (e.g., SiO_2 or Si_3N_4 spacers). As an alternative to the AR-based chemistry, the proposed process is based on the transformation of a chemically stable Pt layer into a more reactive Pt_xGe_y phase that is easily etched in SPM. Starting from a Ge/Pt stack, the Pt_xGe_y phase formed after annealing depends both on the thickness ratio of these layers and on the annealing temperature. Considering the MOSFET device integration, uncertainties on the thickness ratio exist due to the device morphology and due to some degree of anisotropy associated with deposition processes. It is, therefore, desirable to implement a method for which the final phase depends only on the annealing temperature, regardless of the amount of Ge. According to the literature [5]–[8], $PtGe_2$ is the Ge richest phase of the Pt–Ge binary system. Because this stoichiometry is obtained with Ge in excess and for annealing temperatures around 400 °C, our study focuses on this phase. Considering an atomic density [9] of 6.64×10^{22} and 4.42×10^{22} atoms/cm^3 for Pt and Ge, respectively, the Pt:Ge thickness ratio is systematically set to 1:3 in the following experiments.

The p-type substrates featuring a 20-nm-thick SiO_2 full sheet layer were used to study the formation of Pt_xGe_y phases and their solubility in SPM. The samples were loaded in an e-gun evaporation system, and a 20-nm-thick Pt layer followed by a 60-nm-thick Ge overlayer were evaporated. They subsequently received a rapid thermal annealing (RTA) at temperatures ranging from 100 °C to 600 °C for 5 min in forming gas (N_2:H_2::95:5). Grazing angle X-ray diffraction (XRD) characterizations as well as four points probe Rs measurements were performed on full

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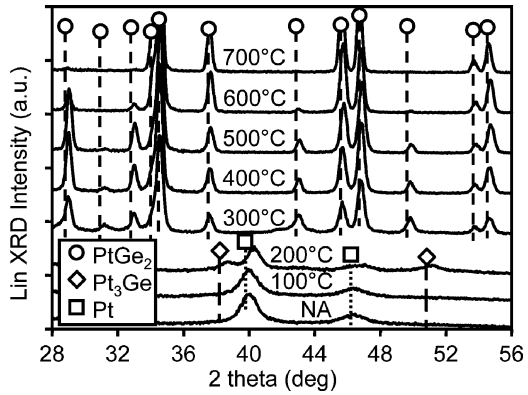

Fig. 1. XRD spectra of the Pt_xGe_y phases obtained from alloying of a Ge (60 nm)/Pt (20 nm) stack on a SiO_2 substrate showing changes in Pt_xGe_y stoichiometry with the temperature of germanidation. A part of the Pt layer reacts with Ge to form the Pt_3Ge phase at 200 °C. At 300 °C, the Pt layer is totally transform into the $PtGe_2$.

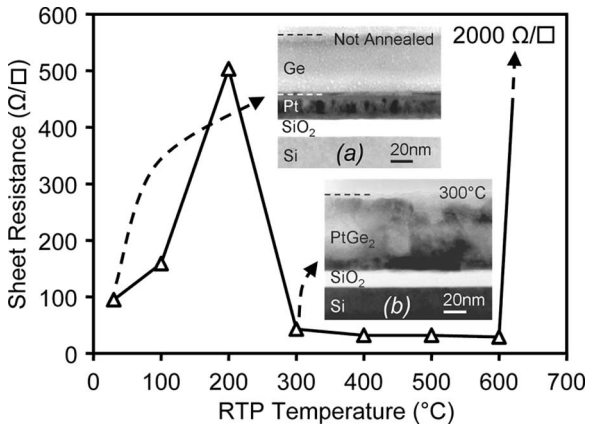

Fig. 2. Variations of the sheet resistance (Rs) with the temperature of germanidation of the Ge (60 nm)/Pt (20 nm) stack on a SiO_2 substrate. A stable $PtGe_2$ phase is formed between 300 and 600 °C. At 200 °C, the large increase of Rs is related to the formation of the Pt_3Ge phase. Above 600 °C, the layer starts to agglomerate resulting in high Rs. Inset: (a) TEM cross-section showing the morphology of the Ge/Pt stack after deposition. (b) TEM cross-section showing the morphology of the Ge/Pt stack for a germanidation temperature of 300 °C. The Ge overlayer is totally reacted to form the $PtGe_2$ phase.

sheet wafers. In Fig. 1, the XRD analysis shows the formation of the $PtGe_2$ phase for annealing temperatures above 300 °C. At 200 °C, the XRD spectrum reveals the presence of the Pt_3Ge phase and also the Pt metallic state. Below this temperature, metallic Pt is solely detected. The transformation curve in Fig. 2 supports conclusions drawn on the basis of diffraction data, highlighting the formation of a stable $PtGe_2$ phase between 300 °C and 600 °C. Above 600 °C, the layer starts to agglomerate, leading to a dramatic increase of Rs. A strong increase of the sheet resistance is also measured at 200 °C that can be related to the formation of the high-resistivity Pt_3Ge phase in Fig. 1, as recently observed in [10]. The Transmission Electron Microscopy (TEM) analysis of the sample before annealing in Fig. 2(a) confirms the Pt:Ge ratio of 1:3. After an annealing at 300 °C for 5 min, the Pt layer is totally reacted with Ge to form the $PtGe_2$ phase, as shown in Fig. 2(b).

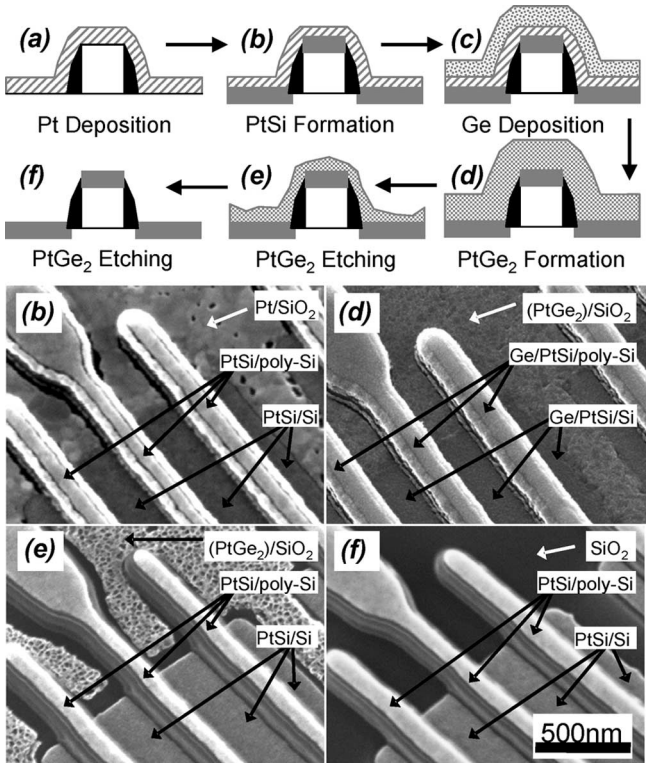

Fig. 3. Scheme of the proposed PtSi integration sequence and tilted aerial SEM views of a 35 nm device. (a) After Pt deposition. (b) After PtSi silicidation. (c) After Ge deposition. (d) After $PtGe_2$ formation. (e) and (f) After etching in SPM.

In order to study the $PtGe_2$ phase chemical reactivity, the samples annealed above 300 °C were dipped into SPM for 10 min. The corresponding SEM observations and the measurement of an infinite Rs confirm that the $PtGe_2$ phase was completely etched away. It was also checked (results not presented here) that the Ge overlayer has no measurable impact on the integrity of PtSi from the electrical (Rs) and morphological (SEM observation) standpoints, as far as a germanidation annealing up to 600 °C and a dip in SPM for 10 min are considered.

III. PtSi Integration in MOSFET Devices

From the aforementioned results, a new scheme for the integration of PtSi in MOSFET devices is presented in Fig. 3. After the definition of the active area by shallow trench isolation (STI), a 12 Å nitrided oxide was grown, on the top of which a 80 nm layer of p^+ polysilicon was deposited. Following the gate patterning, lowly doped (LDD) extensions were implanted, and SiN/SiO_2 spacers were formed. Source and drain junctions were subsequently implanted and annealed. After a deoxidation dip in hydrofluoric acid, the samples were loaded in the e-gun evaporation system. An *in situ* Ar plasma etching was realized, and a 10-nm-thick Pt layer was evaporated [Fig. 3(a)]. The samples were subsequently annealed at 500 °C for 4 min in N_2:H_2 to form a 20 nm PtSi layer [Fig. 3(b)]. In order to transform the Pt in excess into the $PtGe_2$ phase, a 30-nm-thick Ge overlayer was subsequently deposited [Fig. 3(c)] and annealed at 300 °C for

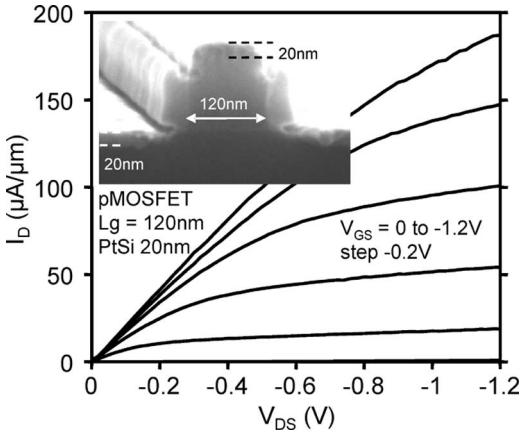

Fig. 4. Measured I_{D}–V_{DS} characteristics of a 120-nm-long p-type MOSFET with PtSi silicide contact. Inset: SEM cross-section of the electrically characterized device. As expected after silicidation from a 10-nm-thick Pt overlayer, a 20-nm-thick PtSi contact is present and left unaltered by the etching procedure using low-temperature germanidation and selective $PtGe_2$ removal in SPM.

5 min in N_2:H_2 [Fig. 3(d)]. As a final step, the selective etching of the $PtGe_2$ phase with respect to PtSi was realized using SPM [Fig. 3(e) and (f)].

The scalability and suitability of this process for MOSFETs devices was morphologically assessed using a 35-nm-gate-long transistor. Fig. 3(b) presents an aerial SEM characterization of the device after the platinum silicidation annealing step. It can be observed that large Pt grains appear on the SiO_2 STI zones and that a smooth PtSi is formed on the Si and poly-Si areas. Excess Pt is then transformed into the etchable $PtGe_2$ phase, after the deposition of the Ge overlayer and annealing, as shown in Fig. 3(d). Fig. 3(e) presents a top view SEM observation after a 5 min wet etch in SPM. The porous aspect of the $PtGe_2$ confirms that the material is being etched. After 10 min in SPM, any sign of chemical reaction (bubbling) at the sample surface vanishes, indicating that the etching of the $PtGe_2$ phase is completed. The corresponding SEM observation in Fig. 3(f) shows that the $PtGe_2$ was successfully removed from the SiO_2 areas, and that the PtSi regions do not present signs of chemical alteration. Finally, the inset of Fig. 4 shows an SEM cross section of a 120 nm device, demonstrating the successful formation of a 20-nm-thick PtSi layer of the gate, source, and drain contacts. It is also clearly observed that the Pt in excess has been successfully removed from the nitride spacers.

Fig. 4 presents the I_{D}–V_{DS} characteristics obtained on the 120-nm-gate-long device (transistors with shorter gate length could not be characterized due to problems in the back-end steps). The electrical functionality of the device fabricated according to the present PtSi integration process is demonstrated. Devices originating from an identical process flow that feature nickel silicided contacts demonstrate a current drive of 210 μA/μm. Considering that the presented PtSi silicided junction can still be optimized, a promising current drive of 190 μA/μm is obtained. The last result confirms that the proposed integration scheme of PtSi is viable and enables the safe integration of PtSi in advanced MOSFET technology.

IV. Conclusion

A new PtSi-safe etching procedure based on a sequence involving germanidation of Pt in excess and removal of the sacrificial $PtGe_2$ in SPM has been developed. PtSi source/drain contacts were integrated on a 120 nm device, showing the viability of the proposed process. The promising electrical characteristics confirm the expected benefits of PtSi as a contact silicide for the next-generation p-MOS technologies.

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