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***Abstract*—This paper presents a detailed RF study for source/drain Schottky-barrier (SB) MOSFETs. Using on-wafer *S*-parameters, high-frequency (HF) figures-of-merit (FoMs) and small-signal equivalent circuits (SSEC) are first extracted and discussed for a 120-nm-gate-length SB MOSFET. Then, using ac simulations, HF FoM's sensitivity along SB height and underlap length variations are subsequently presented. The whole study provides, for SB MOSFETs, a deep understanding of key ac-element (transconductances and capacitances) behavior as well as process-parameter optimization to achieve the best HF FoMs.**

***Index Terms*—High frequency (HF), MOSFETs, Schottky barrier (SB), silicon, silicon-on-insulator (SOI).**

I. Introduction

OVER THE past 40 years, conventional MOSFETs have demonstrated a continuous pace in performance improvement due to aggressive device scaling at the cost of more and more complex process engineering. One of the objectives of pushing technology forward is to continue to develop opportunities for future high-speed and yet very-low-power applications, thus offering even greater energy efficiency for mobile devices. Today, CMOS technologies encounter fundamental difficulties in extending CMOS lifetime to the end of the International Technology Roadmap for Semiconductors [1]. To pursue CMOS evolution, many challenges must be solved, such as the control of leakage currents, difficulties in shallow-junction formation, excess parasitic resistances and capacitances, etc. Moreover, even though nonconventional transistors such as multigated devices are recognized as alternative candidates for scaling, they still require a meticulous optimization of internal parameters to maximize their performance for digital and RF applications. As thin-film technologies are emerging for their capability to tightly control the electrostatic integrity in the channel, the resistance associated with the source/drain (S/D) extensions is identified as one of the biggest challenges to solve in order to preserve current-drive capabilities. In that context, S/D engineering takes an increasing importance in the development of leading edge CMOS generations. In order to alleviate the difficult problem of extrinsic resistances, one solution is to replace the ohmic contacts on highly doped junctions by metallic extensions. This approach readily takes advantage of the reduced sheet resistance of metal compared to heavily doped junctions and also benefits from atomically sharpened silicide/silicon junctions. Low-Schottky-barrier (SB) p-MOSFETs have recently demonstrated competitive current levels (ratio $I_{\rm on}/I_{\rm off}$ over six decades, ideal threshold swing [2]) and also excellent dynamic performance (f_T) [3], [4]. To evaluate the viability of metallic S/D extensions, Connelly *et al.* [5] as well as Xiong *et al.* [6] have theoretically demonstrated that the SB needs to be optimized to less than 0.1 eV for digital circuits. So far, only the analysis of the digital performance of SB MOSFETs has been reported, whereas high-frequency (HF) analog properties have not yet been much investigated in details [7].

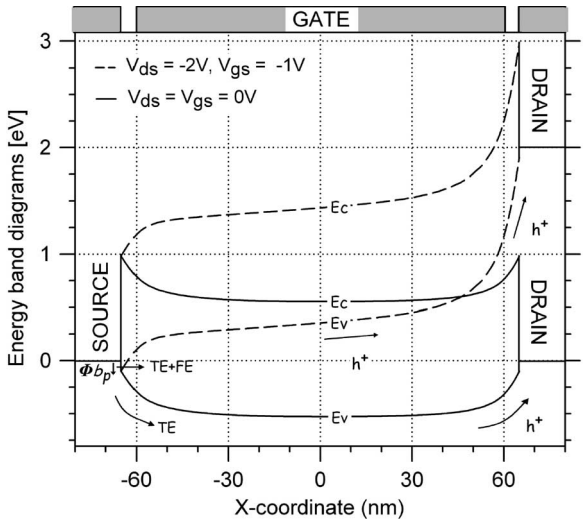

Fig. 1. Simulated energy band diagram along the channel (0.5 nm under the gate oxide) of an SB p-MOSFET for two bias conditions. Biases vary from thermal equilibrium to (solid line) $V_{\rm ds} = -2$ V and (dashed line) $V_{\rm gs} = -1$ V ($\Phi b_p = 0.1$ eV). BL is not shown.

The aim of this paper is to provide a complete small-signal analysis of p-type SB MOSFETs by means of extraction of their HF properties. It presents results of detailed RF measurements carried out on an RF nonoptimized technology with a 120-nm-gate-length SB MOSFET within the context of the constraints imposed to the process that features a single metallization level [8]. An extraction methodology of the quasi-static small-signal

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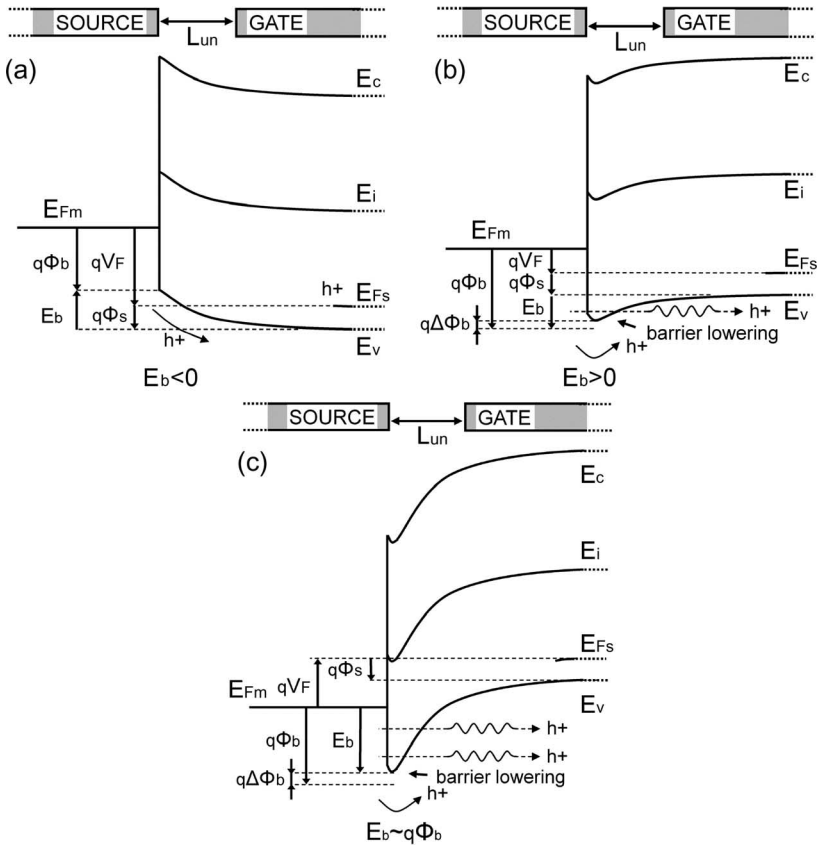

Fig. 2. Schematic illustration of band bending at the source Schottky interface for (a) $V_{\rm gs} = 0$ V and for [(b) and (c)] moderate and large negative gate bias. The barrier height Φ_b is chosen large on purpose to clearly show the band deformation. Components of thermionic and tunneling emission are shown. [(b) and (c)] The BL $\Delta\Phi_b$ is also included.

equivalent circuit (SSEC) is subsequently presented. The study is enhanced by ac small-signal simulations based on a drift-diffusion transport model that provides more insights related to the influence of barrier height and of the length of S/D extension/gate underlap on HF properties.

II. Device Structure

A. Principles of Operation of SB MOSFET

The SB MOSFET is basically a MOS structure that incorporates two back-to-back SB junctions at the S/D extensions whose internal potential is essentially controlled by the gate field. Fig. 1 shows the simulated energy bands along the interface for an accumulation p-type SB MOS at thermal equilibrium and in saturation mode. The SB height for holes $(\rm h+)$ Φb_p is 0.1 eV. It can be observed that the SB at the source side solely contributes to the reduction of the injection of carriers in the channel, whereas at the drain side, the junction operates under forward bias. As a result, the source Schottky junction limits the amount of carriers emitted into the channel, thus resulting in a reduction of the current $I_{\rm ds}$, as well as of the associated extrinsic transconductance $G_{\rm me}$ and extrinsic input capacitance $C_{\rm gg}$ [7]. In the OFF state ($V_{\rm gs} = 0$ V), the total potential barrier is composed of the SB that is superimposed to the electrostatic potential barrier generated by the gate field effect. The threshold voltage is therefore strongly related to the SB height. In the subthreshold regime, energy bands bend downward, resulting in a negative $E_b = q(\phi_b - \phi_s - V_F)$, as shown in Fig. 2(a). Under this gate-bias condition, tunneling injection is obviously not possible, leading to a current that is essentially governed by thermal emission (TE). This partly explains the very low OFF-state current and the significant advantage for deeply scaled CMOS, as described in the literature [9]. When the channel is pushed in the accumulation regime ($V_{\rm gs} = -1$ V and $V_{\rm ds} = -2$ V), current transport through the source SB is dominated by field emission (FE), i.e., tunneling emission due to holes tunneling from the metal to the semiconductor valence band [$E_b \geq 0$ eV, Fig. 2(b) and (c)], rather than by TE. Ideally, under large applied bias [Fig. 2(c)], the barrier tends to be very thin and becomes transparent to holes. Moreover, the image force effect at the Schottky interface further contributes to the lowering of the barrier height. From the previous discussion, it clearly appears that the equivalent contact resistance is bias dependent as it is strongly conditioned by the gate-induced band bending at the vicinity of the Schottky junction. It is worth noting that tunneling emission naturally vanishes when the SB height tends to zero, leading to a configuration of complete contact transparency. Under this ultimate situation, current is solely controlled by TE over the gate-controlled body barrier [10].

Two fundamental parameters are subject to fine tuning for optimizing the injection properties: the SB height and the

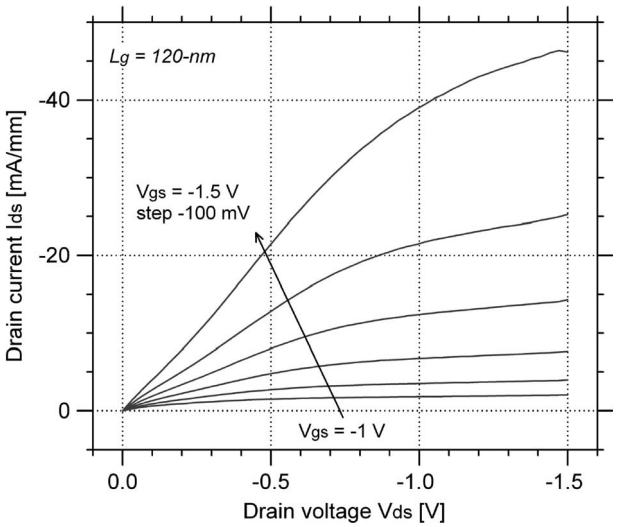

Fig. 3. Measured drain current as a function of drain voltage ($I_{\rm ds}$–$V_{\rm ds}$) for a 120-nm SB p-MOSFET.

underlap length $L_{\rm un}$ that characterizes the separation between the metal/silicon interface and the edge of the gate. Whereas the lowering of the SB remains a difficult exercise of material engineering, a proper selection of $L_{\rm un}$ constitutes a much more flexible leverage that improves FE through the control of band bending. This point is detailed in Section IV.

Before we tackle HF operation, dc $I_{\rm ds}$–$V_{\rm ds}$ characteristics measured on a 120-nm p-type SB MOSFET (Fig. 3) deserve a special attention. It clearly appears that these characteristics are nonlinear at low $V_{\rm ds}$, revealing the signature of carrier injection controlled by the SB at the source side [3], [11], [12].

B. Process and Device Description

The major process steps of the silicon-on-insulator (SOI) SB-MOSFET process under consideration are summarized in Table I. The p-type Si doping level is around 2×10^{15} cm^{-3} corresponding to a low substrate resistivity of $\sim$10 $\Omega \cdot$ cm. The buried oxide (BOX) thickness is around 50-nm, and the SOI film was thinned to 10-nm. A midgap tungsten gate is integrated on a 2.2-nm SiO_2 gate oxide. An underlap of 10-nm is expected to efficiently control short-channel effects without loss of current drive. Full process details are provided in [8]. Note that the use of a single metallization level enables the fabrication of device with only two gate fingers of 6-μm associated in parallel.

TABLE I
MAJOR PROCESS STEPS OF THE SOI SB-MOSFET PROCESS

starting material	10-nm thinned SOI p-type (001) 10Ω.cm	
isolation of active zone	MESA RIE etching	SF_6/N_2
gate oxide	dry 725°C	t_{ox} = 2.2-nm
gate material	Tungsten	L_g = 110-nm
gate patterning	e-beam litho in HSQ + RIE etching	SF_6/N_2
spacer formation	PECVD SiN deposition + RIE etching	L_{sp} = 15-nm width
S/D formation	Platitum deposition (e-beam evaporation)	5-nm
	RTA silicidation 300°C 2' FG	10-nm
	selective Pt/PtSi etch in aqua reggia	-
metal 1	Ti/Al deposition and lift-off	10-nm/500-nm
	contact sintering in forming gas	RTA 420°C 5'

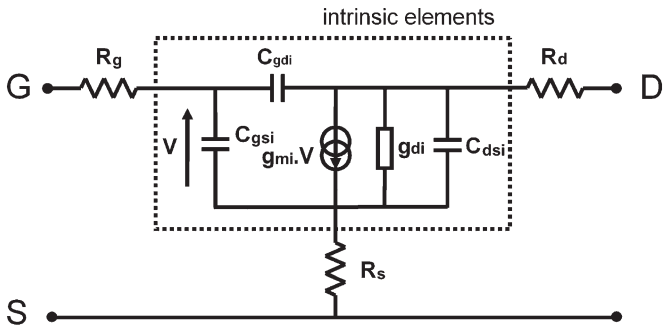

Fig. 4. Quasi-static HF SSEC used to model dynamic operation of SB MOSFETs.

III. Characterization and Modeling of Dynamic Performance

A. RF Modeling of SB MOSFETs

This section reports on the extraction of the RF SSEC of a 120-nm p-type thin-film fully depleted SOI SB MOSFET. On-wafer S-parameters have been measured, up to 6 GHz, using a microwave network analyzer (Agilent 8753ES). The probe calibration was performed using an off-wafer short-open-load-thru procedure. Corrected Y-parameters are subsequently obtained by subtracting those of the associated open test structure from Y-parameters of the device under test (DUT) in order to de-embed coplanar accesses. A more complex de-embedding with a short test structure was not useful for the considered measurement frequency range (0–6 GHz). Because the SBs are located at the S/D sides, the series resistances R_s and R_d may be considered as bias-dependent nonlinear elements. From a small-signal perspective, we assumed that thermionic and tunneling injection could be modeled, at first order, by a single resistance. This assertion is supported by the fact that there is no depletion region at the Schottky interface. As a consequence, the quasi-static SSEC that is typically used to model dynamic operation of conventional MOSFETs can be applied to SB-MOSFET devices. Thus, the usual procedure to extract the extrinsic resistances of conventional MOSFETs [13] does not apply in the present case because it involves a "cold" measurement, i.e., at $V_{\rm ds} = 0$ V. The direct consequence of the strong bias dependency of R_s is that all parameters of the SSEC have to be extracted at the same dc bias. The extraction procedure is detailed in the Appendix.

From the SSEC proposed in Fig. 4, the exact Z-parameters can be expressed as follows:

$$Z_{11} = R_g + R_s + \frac{1}{jC_{\rm gs}\omega\left(1+\frac{jC_{\rm ds}\omega}{g_d+jC_{\rm gd}\omega}\right)+jC_{\rm gd}\omega\left(\frac{g_m+g_d+jC_{\rm ds}\omega}{g_d+jC_{\rm ds}\omega}\right)} \quad (1)$$

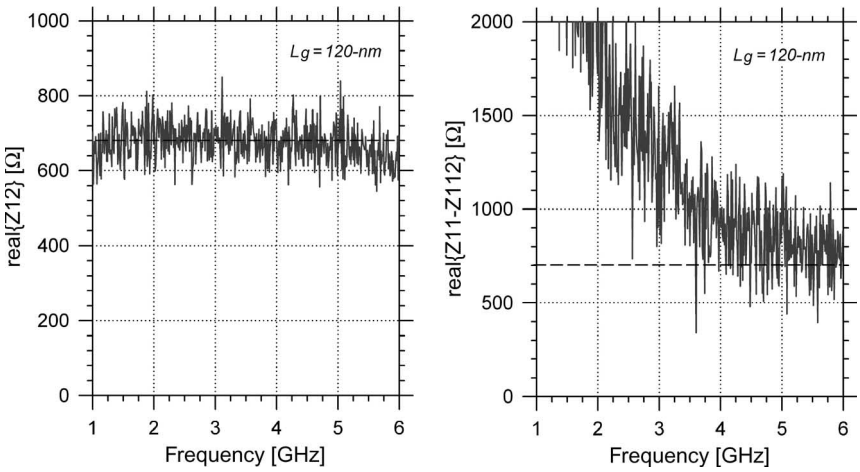

Fig. 5. Extraction of the series resistances (left) R_s and (right) R_g from the real parts of (Z_{12}) and $(Z_{11}–Z_{12})$. R_s and R_g amount to ∼700 Ω ($V_{\rm ds} = V_{\rm gs} = -1.5$ V).

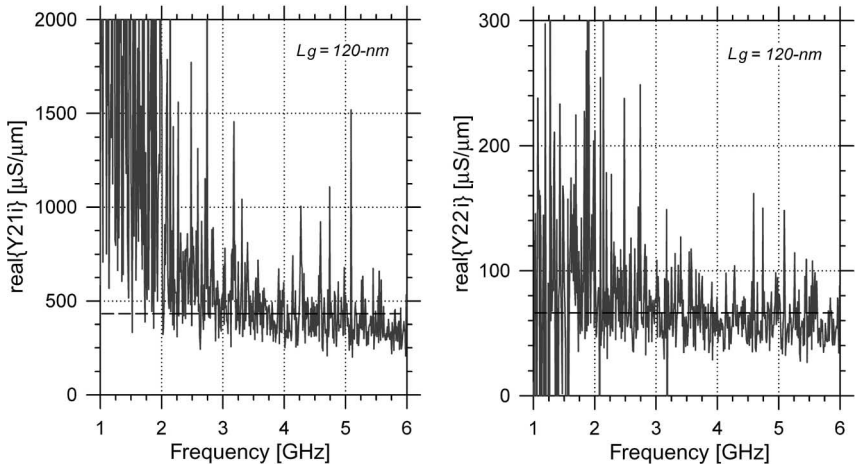

Fig. 6. Extraction of the intrinsic transconductance $g_{\rm mi}$ and output conductance $g_{\rm di}$ from the real part of (Y_{21i}) and (Y_{22i}). $g_{\rm mi}$ and $g_{\rm di}$ are evaluated at 375 and 65 mS/mm, respectively ($V_{\rm ds} = V_{\rm gs} = -1.5$ V). The ratio is about 5.5.

$$Z_{12} = R_s + \frac{1}{\left(\frac{C_{\rm gs}}{C_{\rm gd}}+1\right)} \frac{1}{\left(g_d + \frac{g_m}{\frac{C_{\rm gs}}{C_{\rm gd}}+1} + j\omega\left(C_{\rm ds} + \frac{C_{\rm gs}C_{\rm gd}}{C_{\rm gs}+C_{\rm gd}}\right)\right)} \tag{2}$$

$$Z_{21} = R_s - \frac{1}{jC_{\rm gs}\omega\left(\frac{g_d + j\omega(C_{\rm gd}+C_{\rm ds})}{g_m - jC_{\rm gd}\omega}\right) + jC_{\rm gd}\omega\left(\frac{g_m + g_d + jC_{\rm ds}\omega}{g_m - jC_{\rm gd}\omega}\right)} \tag{3}$$

$$Z_{22} = R_s + R_d + \frac{1}{g_d + \frac{g_m}{\frac{C_{\rm gs}}{C_{\rm gd}}+1} + j\omega\left(C_{\rm ds} + \frac{C_{\rm gs}C_{\rm gd}}{C_{\rm gs}+C_{\rm gd}}\right)}. \tag{4}$$

Considering the real parts of measured Z-parameters, the series extrinsic circuit elements, namely, the source R_s and gate R_g resistances, can be extracted from (1) and (2). For that sake, it is assumed that the real parts of the second terms appearing in the expressions of Z_{11} and Z_{12} are negligible with respect to $(R_g + R_s)$ and R_s, respectively. The real parts of (Z_{12}) and $(Z_{11}–Z_{12})$ are represented in Fig. 5. The observed fluctuations can be attributed to two main causes. First, the accuracy of the de-embedding procedure does not account for losses into the SOI substrate which features a thin BOX layer ($t_{\rm box} = 50$-nm) coupled to a silicon handler substrate of conventional resistivity ($\sim$10 Ω · cm). Second, the device layout features only two 6-μm-wide gate fingers, which results in a relatively high input impedance of the DUT. The accuracy of the de-embedding procedure is therefore limited because it may become difficult to clearly discriminate between the contributions of the intrinsic device from that of the extrinsic passive components.

Because the measured cutoff frequency was relatively low ($f_T \sim 20$ GHz), device measurements were limited to an upper frequency of 6 GHz to favor accuracy. From a practical standpoint, the gate and source resistances were extracted over the frequency range for which the real parts of (Z_{12}) and $(Z_{11}–Z_{12})$, respectively, do not vary, i.e., typically between 4 and 6 GHz. Following the aforementioned prescription, both R_g and R_s were estimated around 700 Ω. For completeness, it was verified, *a posteriori*, that the extracted figures were consistent with the assumption that $(R_g + R_s)$ and R_s dominate the real parts of Z_{11} and Z_{12}, respectively. It

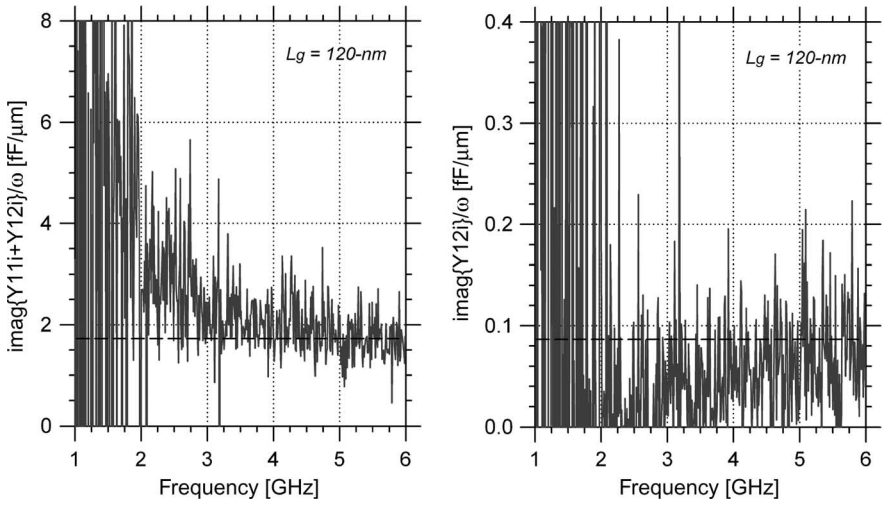

Fig. 7. Extraction of intrinsic gate-to-source capacitance $C_{\rm gsi}$ and gate-to-drain capacitance $C_{\rm gdi}$ from the imaginary parts of (Y_{11i}) and (Y_{12i}). $C_{\rm gsi}$ and $C_{\rm gdi}$ are evaluated at 1.65 and 0.08 fF/μm, respectively ($V_{\rm ds} = V_{\rm gs} = -1.5$ V). The ratio is about 20.

TABLE II
EXTRACTED PARAMETERS OF THE SSEC

L_G = 120-nm, W_{TOT} = 2*6-μm, Vds = -1.5V, Vgs = -1.5V

Element	Value	Normalized value (μm^{-1})
g_{mi} (μS)	4500	375
g_{di} (μS)	800	66
C_{gsi} (fF)	19.8	1.65
C_{gdi} (fF)	0.96	0.08
R_s (Ω)	700	8.4 kΩ.μm
R_g (Ω)	700	84 Ω/square
f_c (GHz) *	35.9	-
f_T (GHz) **	20.0	-
f_{max} (GHz) ***	15.5	-

* f_c is calculated as $f_c = g_{mi}/2\pi C_{gsi}$
** f_T is calculated following Eq. (10).
*** f_{max} is calculated following Eq. (11).

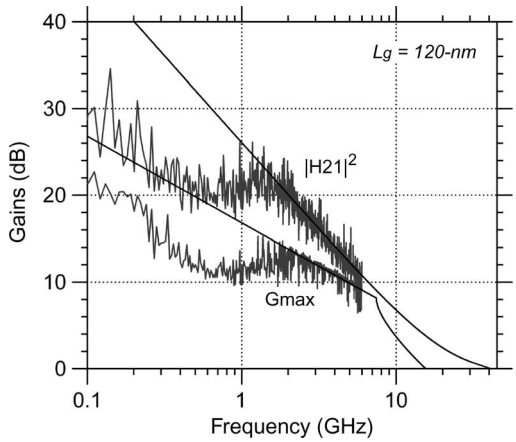

Fig. 8. Comparison between measured and retro-simulated gains as a function of frequency ($V_{\rm ds} = V_{\rm gs} = -1.5$ V). This device shows an f_T of 20 GHz and an $f_{\rm max}$ of 13 GHz.

finally turns out that the normalized source resistance is equal to 8.4 k$\Omega \cdot \mu$m, whereas the gate sheet resistance amounts to 84 $\Omega/\square$. These normalized resistances can be considered as relatively large when compared with their counterparts in conventional S/D MOS technologies. As far as the source resistance is considered, the reason behind its large value is related to the nonoptimized Schottky contact associated to a long underlap. On the other hand, the large gate resistance is due to a nonoptimized contact between the first metal level and the tungsten gate. At this stage, it is important to summarize the following important features that render the extraction of SSEC elements in SB MOSFETs, which are markedly different from that in conventional S/D devices: 1) The strong bias dependence of R_s with barrier height and gate bias precludes the application of "cold" measurements as conventionally used for conventional S/D MOS architectures, and 2) the simplified extraction procedure used to evaluate R_g and R_s applies only in the limit of large resistances, a condition that is fulfilled for the fabricated devices under consideration. After de-embedding the extrinsic series resistances, the main intrinsic SSEC elements can be subsequently extracted from the intrinsic admittance parameters using the following:

$$g_{\rm mi} = \Re e\{Y_{21i}\} \tag{5}$$

$$g_{\rm di} = \Re e\{Y_{22i}\} \tag{6}$$

$$C_{\rm gsi} = \frac{\Im m\{Y_{11i} + Y_{12i}\}}{\omega} \tag{7}$$

$$C_{\rm gdi} = \frac{-\Im m\{Y_{12i}\}}{\omega} \tag{8}$$

$$C_{\rm dsi} = \frac{\Im m\{Y_{22i} + Y_{12i}\}}{\omega}. \tag{9}$$

Intrinsic elements $g_{\rm mi}$, $g_{\rm di}$, $C_{\rm gsi}$, and $C_{\rm gdi}$ are again evaluated over the frequency range for which fluctuations are the smallest, i.e., typically between 4 and 6 GHz (Figs. 6 and 7).

The measured and corresponding normalized values for each SSEC element are summarized in Table II.

According to a first-order calculation, the current-gain cutoff frequency f_T and the maximum frequency of oscillation $f_{\rm max}$

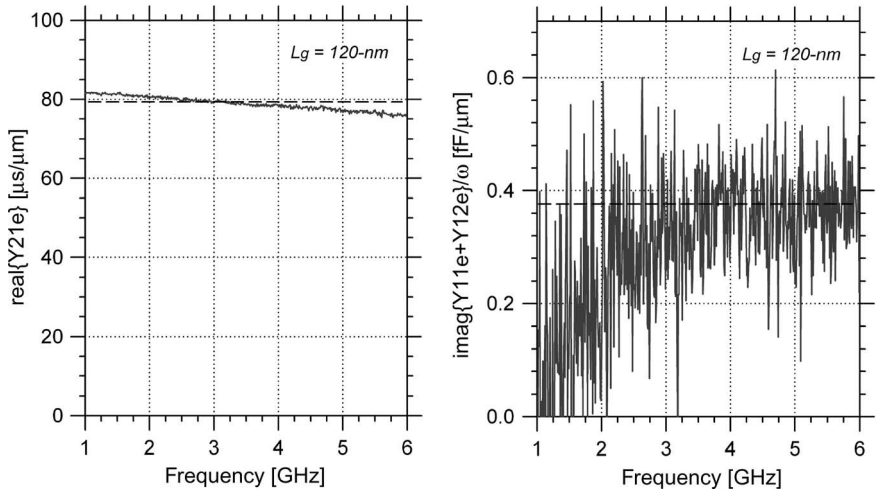

Fig. 9. Extraction of the (left) extrinsic transconductance $G_{\rm me}$ and the (right) extrinsic gate-to-source capacitance $C_{\rm gse}$ from the real part of (Y_{21}) and the imaginary part of $(Y_{11}+Y_{12})$. Extracted values are 79 μS/μm and 0.38 fF/μm ($V_{\rm ds}=V_{\rm gs}=-1.5$ V).

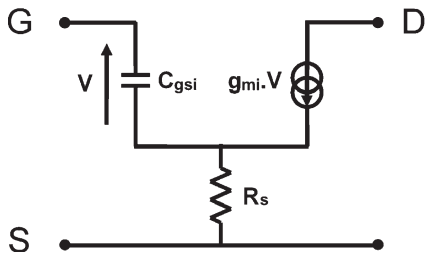

Fig. 10. Simplified small-signal model for SB MOSFET.

are given by (10) and (11) [14].

$$f_T=\frac{f_c}{\left(1+\frac{C_{\rm gdi}}{C_{\rm gsi}}\right)+(R_s+R_d)\left(\frac{C_{\rm gdi}}{C_{\rm gsi}}\left(g_{\rm mi}+g_{\rm di}\right)+g_{\rm di}\right)}$$

$$\text{with } f_c=\frac{g_{\rm mi}}{2\pi C_{\rm gsi}} \tag{10}$$

$$f_{\max}=\frac{f_c}{2\cdot\left(1+\frac{C_{\rm gdi}}{C_{\rm gsi}}\right)\sqrt{g_{\rm di}(R_g+R_s)+\frac{1}{2}\frac{C_{\rm gdi}}{C_{\rm gsi}}\left(R_s g_{\rm mi}+\frac{C_{\rm gdi}}{C_{\rm gsi}}\right)}}. \tag{11}$$

Using the extracted parameters of the SSEC given in Table II, the cutoff frequencies can be retro-simulated and compared to experimental ones. For that sake, Fig. 8 shows the variations of $|H_{21}|^2$ and $G_{\max}$ as a function of frequency, from which f_T and $f_{\max}$ are extracted. Measured values of f_T and $f_{\max}$ are 20 and 13 GHz, respectively, which are in excellent agreement with those evaluated using (10) and (11) and those reported in Table II.

From a more general standpoint, the following remarks can be drawn as far as the impact of SSEC elements on RF device performance is considered. The intrinsic gate-to-drain capacitance for SB MOSFETs in saturation region is essentially composed of the fringing capacitance because the gate does not overlap the S/D silicide contacts. Hence, for this device, a ratio $C_{\rm gsi}/C_{\rm gdi}$ as high as 20 is obtained, which is much

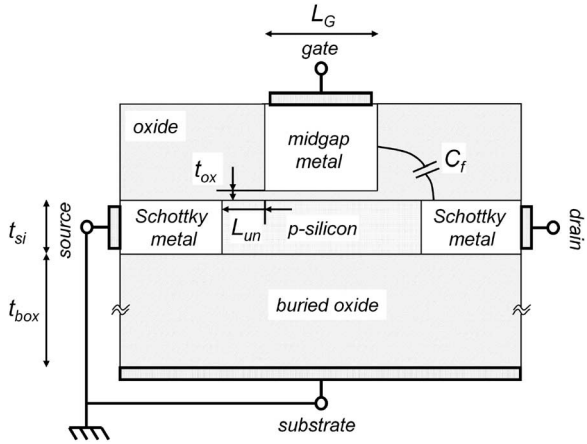

Fig. 11. Schematic representation of the simulated SB MOSFET. Source and drain are Schottky contacts.

TABLE III
NOMINAL PARAMETERS OF METAL S/D p-TYPE DEVICES

parameters	*range*	*description*
L_g	120-nm	Gate length
t_{si}	10-nm	Body thickness
L_{sp}	5-nm/Tuned	Spacer Width
N_{Asi}	2.10^{15} cm^{-3} (p-type)	Channel Doping
Wf_g	Midgap Tungsten	Gate Workfunction
Φb_p	0.1 eV/Tuned	Barrier Height of metal S/D
t_{ox}	2.2-nm (SiO_2)	Gate dielectric stack
t_{box}	400-nm	Buried Oxide thickness

higher than the ratio that is usually observed in standard 130-nm CMOS technology [14], [15]. Metal S/D in SB MOSFETs provides lower resistance through an optimized barrier height, as well as reduction in parasitic capacitances. In the saturation regime, the intrinsic gate–source capacitance $C_{\rm gsi}$ is close to 2/3 $C_{\rm ox}$ ($\sim$16 fF) to which fringing capacitance is added. This last observation confirms that the charge control in SB MOSFETs is similar to the one of a conventional MOSFET. From an extrinsic point of view, the extrinsic transconductance $G_{\rm me}$ and the extrinsic capacitance $C_{\rm gse}$, which constitute apparent

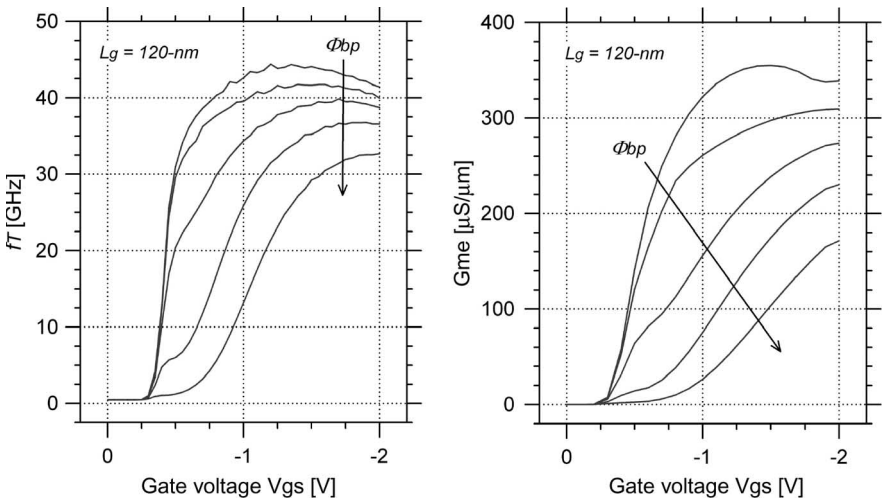

Fig. 12. Extraction of (left) current-gain cutoff frequency f_T and (right) extrinsic transconductance $G_{\rm me}$ for different SB heights varying from 0 to 0.2 eV by a step of 50 meV ($V_{\rm ds} = -2$ V).

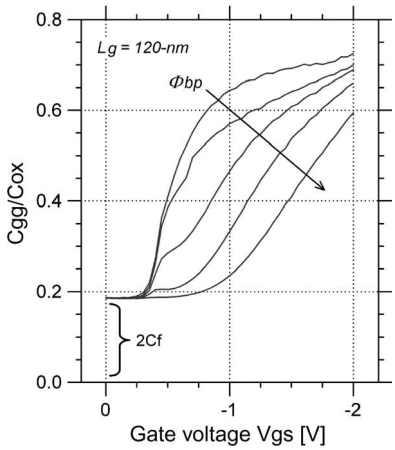

Fig. 13. Extraction of the extrinsic total input capacitance $C_{\rm gg}$ for different SB heights varying from 0 to 0.2 eV by a step of 50 meV ($V_{\rm ds} = -2$ V).

elements including the series-resistance contribution, are lower than their intrinsic counterparts (Fig. 9). In order to explain the significant discrepancy obtained between the intrinsic/extrinsic transconductances and capacitances, a simplified analysis is proposed on the basis of intrinsic equivalent circuit model of the SB MOSFET (Fig. 10). This first-order schematic circuit is composed of the intrinsic transconductance $g_{\rm mi}$ and of the intrinsic gate-to-source capacitance $C_{\rm gsi}$ associated in series with the source resistance. The gate-to-drain feedback capacitance is neglected.

From a first-order analysis, Y_{11} and Y_{21} are expressed as

$$Y_{11} \approx j \cdot C_{\rm gse} \cdot \omega \approx j \cdot \frac{C_{\rm gsi}\omega}{(1+g_{\rm mi}R_s)}$$
$$Y_{21} \approx G_{\rm me} \approx \frac{g_{\rm mi}}{(1+g_{\rm mi}R_s)}. \quad (12)$$

From this simple analysis, it is easily deduced that both extrinsic parameters $G_{\rm me}$ and $C_{\rm gse}$ are weighted by the term $1/(1 + g_{\rm mi} \cdot R_s)$. Thus, the extrinsic transconductance $G_{\rm me}$ and capacitance $C_{\rm gse}$ can be strongly affected by the occurrence of a high source resistance. The net result is that charge control in the channel does not predominantly depend on the gate field effect, but it is also markedly influenced by the equivalent resistance of source/channel Schottky junction. In order to better evaluate the impact of Schottky junction of HF performance, the following section offers a simulation study that quantifies the role of the barrier height and of the underlap length.

IV. Simulation

A. Structure

Consistent with the fabricated SB MOSFET, the simulated structure of the device is shown in Fig. 11. Table III provides the list of the nominal device parameters. Note that the electrostatic fringing capacitances are intrinsically taken into account.

B. Device Modeling

The modeling task was achieved based on 2-D drift-diffusion transport model available in the Silvaco/Atlas device simulation code [16]. In order to improve the mobility model in the high-field region [17], the coefficients of the Caughey–Thomas model are modified to $\beta = 1$, vsat $= 2.2 \times 10^7$ cm/s for electrons and $\beta = 0.65$, vsat $= 1.5 \times 10^7$ cm/s for holes, as suggested by Bude in [18]. Using this modified drift-diffusion-like model, it is proven in [18] that the channel velocity agrees well to that computed by Monte Carlo simulations. Therefore, it is assumed that this parameter selection partially compensates the inherent limitation of the drift-diffusion transport model [16], specifically for sub-100-nm devices. Special care has been taken to model carrier injection at the Schottky junction by using a physically sound approach that accounts for TE, FE, and barrier lowering (BL) models by the image force. The tunneling current model is based on the universal Schottky tunneling approach described in [16], [19], and [20], and the tunneling probability is calculated using the Wenzel–Kramers–Brillouin approximation, assuming a triangular potential profile. The values chosen for the effective mass of electron and hole are $0.258m_0^{[001]}$ and $0.275m_0^{[001]}$,

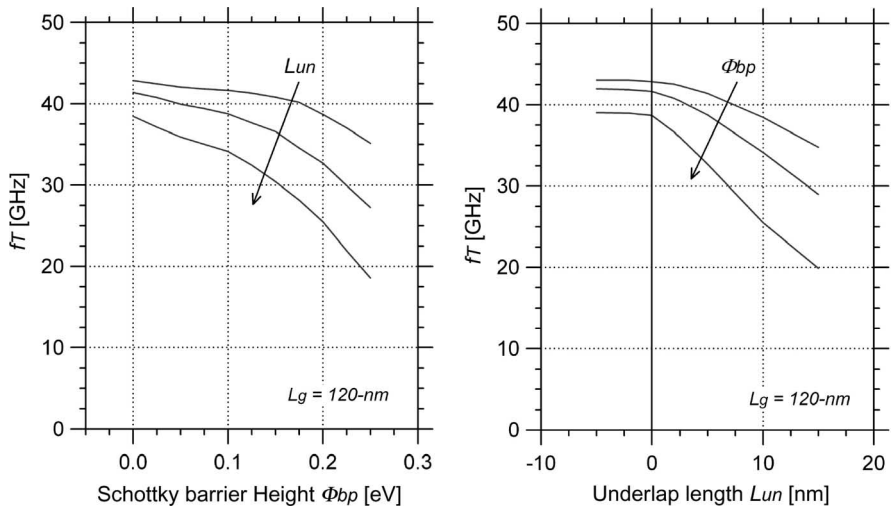

Fig. 14. Extraction of the current-gain cutoff frequency f_T as a function of (left) SB height for different underlap lengths ranging from 0 to 10 nm by a step of 5 nm and as a function of (right) underlap length for three SB heights: 0, 0.1, and 0.2 eV ($V_{\rm ds} = V_{\rm gs} = -2$ V).

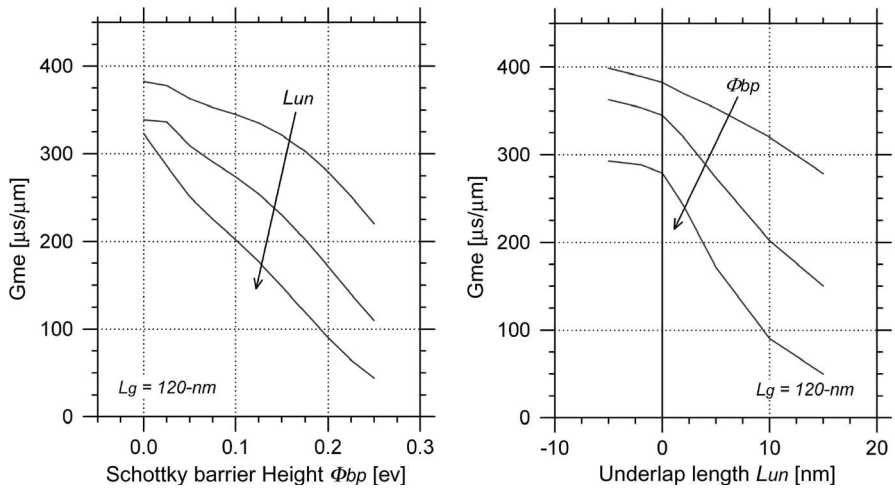

Fig. 15. Extraction of the transconductance $G_{\rm me}$ as a function of (left) SB height for different underlap lengths varying from 0 to 10 nm by a step of 5 nm and as a function of (right) underlap length for three SB heights: 0, 0.1, and 0.2 eV ($V_{\rm ds} = V_{\rm gs} = -2$ V).

respectively, according to [21]. Note that the choice of carriers' effective mass affects very sensitively the injection rate at the Schottky interfaces. As outlined in [6], tunneling is the dominant transport mechanism at high-bias condition.

C. Results

The variation of simulated cutoff frequency f_T as a function of gate voltage $V_{\rm gs}$ is shown in Fig. 12, when the device is biased in the saturation regime ($V_{\rm ds} = -2$ V).The largest f_T is consistently obtained when Φb_p is minimum, i.e., $\Phi b_p = 0$ eV, with a maximum performance of 45 GHz. As Φb_p increases, f_T slightly decreases first and subsequently decays at an accelerated rate when Φb_p becomes larger than 0.1 eV. The extrinsic transconductance $G_{\rm me}$ is also shown in Fig. 12 at the same operating conditions. From the inspection of this last parameter, two major observations can be made. First, nonlinear effects are clearly observed around the threshold voltage for the largest Φb_p because the emission rate at the Schottky junction is mainly driven by the thermionic rather than the FE process in the very low injection regime. Second, the decrease of $G_{\rm me}$ observed that accompanies an increase of the barrier height does not impact f_T proportionally. For instance, $G_{\rm me}$ typically varies from 320 mS/mm at $\Phi b_p = 0$ eV to 150 mS/mm at $\Phi b_p = 0.1$ eV, keeping $V_{\rm gs}$ equal to -1 V. Surprisingly, this $\sim$50% loss in extrinsic transconductance is not reflected on f_T (Fig. 12), which degrades by less than 20%. This last point is of utmost interest because it shows that Φb_p does not need to be aggressively reduced to 0 eV to approach the best achievable f_T performance.

Because f_T is essentially related to $G_{\rm me}$ and $C_{\rm gg}$, the previous discussion naturally suggests that a detailed analysis of $C_{\rm gg}$ with gate bias is required. In that spirit, the ratio $C_{\rm gg}/C_{\rm ox}$ is represented as a function of the gate voltage in Fig. 13. Regardless of the SB height, it is observed that $C_{\rm gg}/C_{\rm ox}$ asymptotically approaches 2/3 (neglecting the rigid shift introduced by fringing capacitances), as expected when the device operates in the saturation regime. However, the rate at which this limit is reached is delayed as the barrier height increases. As a result, the weak dependence of f_T on the

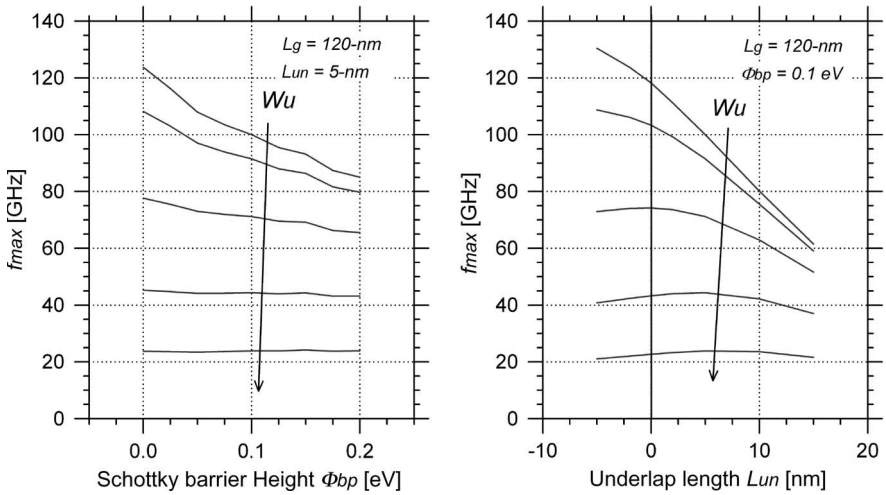

Fig. 16. Extraction of the maximum frequency of oscillation $f_{\max}$ as a function of (left) SB height, keeping $L_{\rm un} = 5$ nm, and as a function of (right) underlap length (keeping $\Phi b_p = 0.1$ eV) for different gate unit widths varying from 1, 2, 4, and 8 to 16 μm ($R\Box = 10\ \Omega/\Box, V_{\rm ds} = V_{\rm gs} = -2$ V).

barrier height can be explained by the simultaneous reduction of both $G_{\rm me}$ and $C_{\rm gg}$. This effect is particularly well exemplified when Φb_p is lower than 0.15 eV: It is clearly shown that the loss of $G_{\rm me}$ (Fig. 12) is counterbalanced by the reduction of $C_{\rm gg}$ (Fig. 13) that finally results in only a slight reduction of f_T. In conclusion, a fine optimization of the SB height and underlap length is of paramount importance to achieve the best HF device performance without necessarily resorting to extreme Schottky contact engineering to approach the zero barrier height.

D. Variations of Performance With S/D Engineering

The optimization of the ac performance through the modulation of the SB and underlap length is discussed in this section. The variations of f_T and $G_{\rm me}$ as a function of the SB and underlap length are represented in Figs. 14 and 15 for $V_{\rm ds} = V_{\rm gs} = -2$ V. When the underlap reduces to zero, f_T degrades by less than 5% when the barrier height varies from 0 and 0.15 eV. In contrast, an f_T reduction of more than 20% is observed for $L_{\rm un} = 10$-nm. The same type of observation also applies to $G_{\rm me}$ which exhibits an accelerated degradation for the same coordinated variations of the underlap and barrier height: When Φb_p varies from 0 to 0.15 eV, the $G_{\rm me}$ degradation amounts to 15% at $L_{\rm un} = 0$- μm while it reaches 50% at $L_{\rm un} = 10$-nm.

Complementary to the f_T analysis, the maximum frequency of oscillation is shown in Fig. 16 as a function of barrier height and underlap length for different gate unit widths W_u (from 1 to 16-μm). The gate sheet resistance is assumed to be equal to 10 $\Omega/\Box$. Note that a first-order analysis predicts that $f_{\max}$ is independent of the number of gate fingers (N_f) but dependent on W_u through the product $R_g \cdot g_d$ [(11)].

However, it must be kept in mind that once the gate resistance is minimized through the optimal choice of W_u, the S/D series resistance dominates $f_{\max}$ behavior [(11)]. This last remark is well exemplified in Fig. 16 which clearly shows that $f_{\max}$ is a very sensitive function of $L_{\rm un}$. $f_{\max}$ varies typically from 120 to 60 GHz when $L_{\rm un}$ increases from 0 to 15-nm at $\Phi b_p = 0.1$ eV and for a unit gate width of only 1-μm (small R_g), whereas $f_{\max}$ stays constant when large W_u is considered (large R_g).

This section actually demonstrates that the design constraint to achieve the best FoMs lies in either of the following: 1) to have $L_{\rm un}$ less than 0-nm if Φb_p is not optimized or 2) to realize Φb_p as low as possible if $L_{\rm un}$ is not optimized. This is encouraging, particularly for n-type SB MOSFET whose S/D metal features the lowest SBs for electrons around 0.27 eV [22], [23]. In addition, smaller gate resistance can further enhance the $f_{\max}$ performance of the SB.

V. Conclusion

This paper proposed a complete ac study of p-type SB-MOSFET, including SSEC extraction supplemented by careful HF simulations. It was first shown, using careful experimental data, that in strong inversion operation, the intrinsic-gate-capacitance SB MOSFETs reach the classical value obtained for conventional MOSFETs (2/3 $C_{\rm ox}$). Nevertheless, it was revealed and strengthened through ac simulations that the charge control was governed by the SB, e.g., carrier injection at the salicide/silicon source side, for the whole gate biasing variation. It turns out that SB MOSFETs compete or are even better than conventional MOSFETs for their RF performance, subject to a fine optimization of the SB height or/and underlap length (spacer width), which is performed to optimize the S/D contact resistances. The overall study demonstrates that metallic S/D contact MOSFETs are a serious and reliable architecture to pursue the silicon roadmap beyond the 22-nm node.

Appendix

This appendix synthetizes in Table IV the procedure to extract different elements of the SSEC from HF measurement of RF devices using a vectorial network analyzer.

TABLE IV
TYPICAL STEPS OF EXTRACTION OF THE SSEC

1. Measurements of scattering parameters of Device Under Test (DUT) and Open Test Structure (OTS) $[S]_{DUT}$, $[S]_{OTS}$
2. Mathematical transformations $[S]_{DUT} \rightarrow [Y]_{DUT}$ $[S]_{OTS} \rightarrow [Y]_{OTS}$
3. OTS de-embedding $[Y]_{DEVICE} = [Y]_{DUT} - [Y]_{OTS}$
4. Mathematical transformation $[Y]_{DEVICE} \rightarrow [Z]_{DEVICE}$
5. Extraction of series resistances
6. Extraction of Intrinsic Z $[Z]_{INTRINSIC} = [Z]_{DEVICE} - [Z]_R$ $[Z]_R = \begin{bmatrix} R_g + R_s & R_s \\ R_s & R_d + R_s \end{bmatrix}$
7. Mathematical transformation $[Z]_{INTRINSIC} \rightarrow [Y]_{INTRINSIC}$
8. Extraction of Intrinsic Elements

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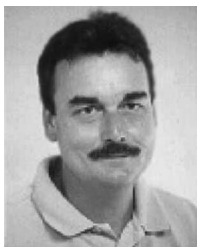

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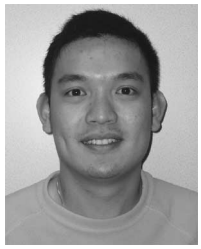

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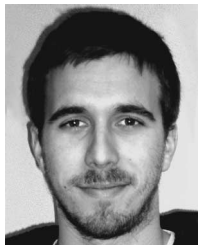

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