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# Single carbon nanotube transistor at GHz frequency

J. Chaste,<sup>1,2</sup> L. Lechner,<sup>3</sup> P. Morfin,<sup>1,2</sup> G. Fève,<sup>1,2</sup> T. Kontos,<sup>1,2</sup> J.-M. Berroir,<sup>1,2</sup> D.C. Glatli,<sup>1,2,4</sup> H. Happy,<sup>5</sup> P. Hakonen,<sup>3</sup> and B. Plaçais<sup>1,2,\*</sup>

<sup>1</sup>*Ecole Normale Supérieure, Laboratoire Pierre Aigrain, 24 rue Lhomond, 75005 Paris, France*

<sup>2</sup>*CNRS UMR8551, Laboratoire associé aux universités Pierre et Marie Curie et Denis Diderot, France*

<sup>3</sup>*Low Temperature Laboratory, Helsinki University of Technology, Otakaari 3A, Espoo, 02015 Finland*

<sup>4</sup>*Service de Physique de l'Etat Condensé, CEA Saclay, F-91191 Gif-sur-Yvette, France*

<sup>5</sup>*Institut d'Electronique, de Microélectronique et de Nanotechnologie, UMR-CNRS 8520, BP 60069, Avenue Poincaré, 59652, Villeneuve d'Asq, France*

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We report on microwave operation of top-gated single carbon nanotube transistors. From transmission measurements in the 0.1–1.6 GHz range we deduce device transconductance  $g_m$  and gate-nanotube capacitance  $C_g$  of micro- and nanometric devices. A large and frequency-independent  $g_m \sim 20 \mu\text{S}$  is observed on short devices which meets best dc results. The capacitance per unit gate length  $\sim 60 \text{ aF}/\mu\text{m}$  is typical of top gates on conventional oxide with  $\epsilon \sim 10$ . This value is a factor 3–5 below the nanotube quantum capacitance which, according to recent simulations, favors high transit frequencies  $f_T = g_m/2\pi C_g$ . For our smallest devices, we find a large  $f_T \sim 50 \text{ GHz}$  with no evidence of saturation in length dependence.

PACS numbers:

Carbon nanotube field effect transistors (CNT-FETs) are very attractive as ultimate, quantum limited devices. In particular, ballistic transistors have been predicted to operate in the the sub-THz range [1, 2]. Experimentally, a state-of-the-art cut-off frequency of 30 GHz has been reached in a low impedance multi-nanotube device [3], whereas 8 GHz was achieved with a multigate single nanotube transistor [4]. Indirect evidence of microwave operation were also obtained in experiments based on mixing effects or channel conductance measurement in single nanotubes [5, 6, 7, 8, 9].

The extraordinary performances of nanotubes as molecular field effect transistors rely on a series of unique properties. High-mobility "p-doped" single walled nanotubes can be obtained by CVD-growth, with a semiconducting gap  $\Delta \sim 0.5\text{--}1 \text{ eV}$  (diameter 1-2 nm) [10]. Low Schottky-barrier contacts, with Pd metallisation, and quasi-ballistic transport result in a channel resistance  $R_{ds}$  approaching the quantum limit,  $h/4e^2 = 6.5 \text{ k}\Omega$  for a 4-mode single walled nanotube [11]. High saturation currents, limited by optical phonon emission, allow large biases,  $I_{ds} \sim 20 \mu\text{A}$  at  $V_{ds} \gtrsim 1 \text{ V}$  in short nanotubes [12, 13]. The above numbers and the good gate coupling explain the large transconductances,  $g_m \sim I_{ds}/\Delta \gtrsim 10 \mu\text{S}$ , observed in dc experiments [1]. In the ac, an intrinsic limitation is given by the transit frequency  $f_T = g_m/2\pi C_g$ , where  $C_g$  is the gate-nanotube capacitance. Here  $C_g = C_{geo}C_Q/(C_{geo} + C_Q)$  is the series combination of the quantum and geometrical capacitances,  $C_Q$  and  $C_{geo}$ . Ultrathin oxide coating in CNT-FETs allows to approach the quantum limit with a capacitance per unit gate length  $l_g$ ,  $C_{geo}/l_g > C_Q/l_g =$

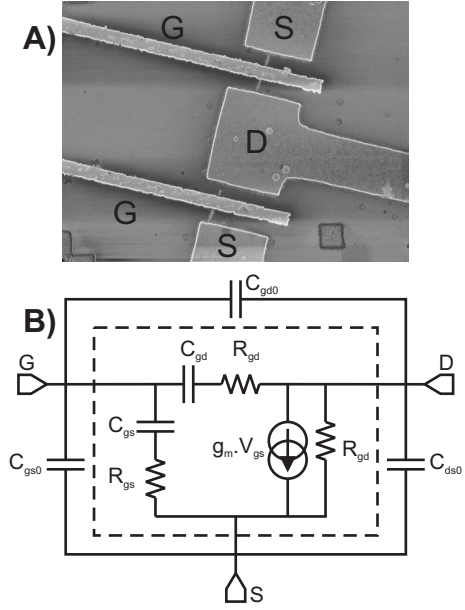


FIG. 1: Panel A : scanning electron microscope image of a single carbon-nanotube double-gate transistor. Gate length is 300 nm. Panel B : small-signal equivalent circuit of the carbon-nanotube transistor. Extrinsic components are displayed outside the dashed rectangle. Notations are explained in the text.

$4e^2/hv_F \sim 400 \text{ aF}/\mu\text{m}$  for  $v_F \sim 4 \times 10^5 \text{ m/s}$ , a typical value for semiconducting NTs [14].

Beside basic interest for quantum limited nano-devices, single nanotube transistors offer new opportunities for fast charge detection due to unique combination of short time response and high charge sensitivity. At present, charge counting experiments performed in nanotube or semiconducting quantum dots use either single electron

\*Electronic address: Bernard.Placais@lpa.ens.fr

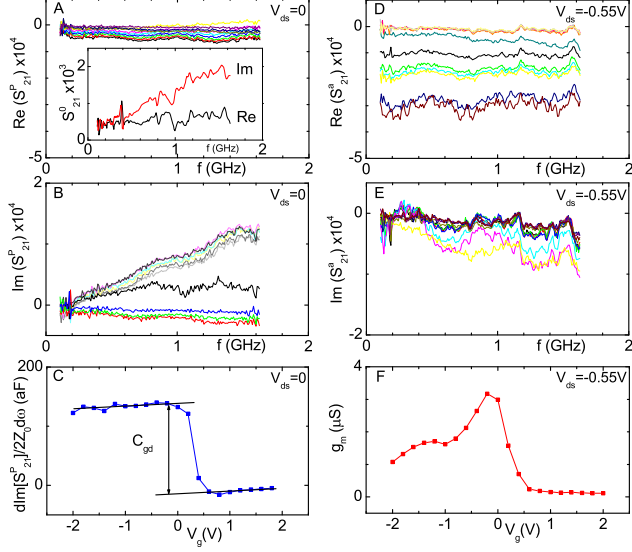


FIG. 2: A 3  $\mu\text{m}$  gate transistor. Transmission amplitude  $S_{21}$  as function of frequency. Background contribution (inset of panel A), passive zero-bias (panels A and B) and active biased (panels D,E) contributions. Panels A and D (resp. B and E) have same scales for direct data comparison. Lines correspond to  $V_g = -2$ – $2\text{V}$  with an increment of 0.4V. Panel C gives the slope  $\langle d\Im[S_{21}^a(\omega)]/d\omega \rangle$  as function of gate voltage. It shows a discontinuity at the opening of channel conductance associated with the gate-drain capacitance. Panel F shows device transconductance.

transistors [15, 16] or quantum point contact detectors [17] which operate on microsecond timescales. High sensitivity of NT-FET has been demonstrated recently by monitoring tunneling events between the nanotube and a nearby gold particle [18] at the dc limit. Performing such experiments with quantum dots at nanosecond timescales would allow to extend charge counting in the coherent regime relevant for full quantum electronics [19]. Given the shot noise limitation of a nanotube detector of bandwidth  $1/\tau = 1\text{ns}^{-1}$ , overestimated by the poissonian value  $\sqrt{I_{ds}\tau}/e = 250$  electrons for  $I_{ds} \sim 10 \mu\text{A}$ , single charge resolution requires a charge gain  $g_m\tau/C_g \gtrsim 250$  or equivalently a transit frequency  $f_T = g_m/2\pi C_g \gtrsim 40 \text{GHz}$ .

In this letter we demonstrate room-temperature broadband GHz operation ( $f = 0.1$ – $1.6 \text{GHz}$ ) of nanotransistors made of a single carbon nanotube, with  $l_g = 0.3 \mu\text{m}$  and  $3 \mu\text{m}$  (channel lengths 1 and  $3.5 \mu\text{m}$  respectively). Our main results are the high  $g_m \sim 10$ – $20 \mu\text{S}$  in short tubes, and the scaling  $C_g \propto l_g$ . From the latter we deduce  $C_g/l_g \sim 60 \text{aF}/\mu\text{m}$ , in accordance with previous low-frequency determinations [20], and  $f_T \sim 50 \text{GHz}$  for our  $l_g = 300 \text{nm}$  devices.

Double-gate carbon nanotube transistors were fabricated by e-beam lithography in a coplanar strip-line ge-

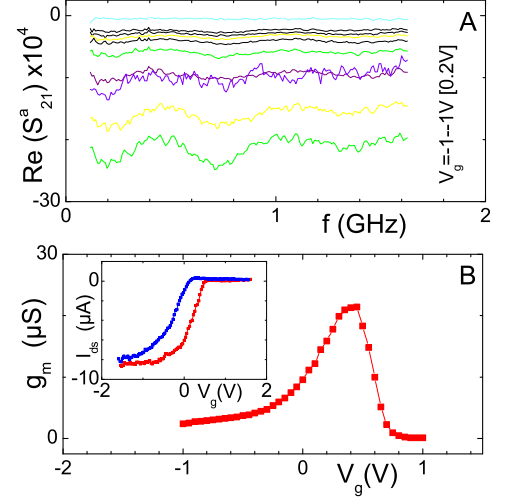


FIG. 3: Characterisation of a 300 nm gate transistor. Transmission amplitude of active contribution (panel A) and transconductance (panel B). Inset shows hysteresis in the dc characteristics as  $V_g$  is swept.

ometry, with two symmetric top gates (see Fig.1), on oxidized high-resistivity silicon substrates (resistivity 3–5  $\text{k}\Omega\cdot\text{cm}$ ). Nanotubes were synthesized from nano patterned catalyst pads using a standard CVD recipe. Palladium contact evaporation is followed by multistep oxidation of thin aluminium, for a total oxide thickness of  $\simeq 6 \text{nm}$ , and finally gold-gate deposition. This process provides full oxidation of Al into  $\text{Al}_2\text{O}_3$  with  $\epsilon \simeq 9.8$ . From sample geometry and dielectric constants, we estimate  $C_{geo}/l_g \sim 100 \text{aF}/\mu\text{m}$ .

Devices were characterized in a standard  $S$ -parameter measurement using an RF probe station and a network analyzer. Attenuators ( $-6 \text{dB}$  and  $-10 \text{dB}$ ), followed by bias tees, are mounted directly at the input and output ports of the station to minimize standing waves in the  $Z_0 = 50 \Omega$  cables due to large impedance mismatch  $R_{ds}/Z_0 \sim 300$ . To compensate for small voltage gain,  $Z_0 g_m \sim 10^{-3}$ , output signals are amplified by two 0.1–2 GHz bandwidth low noise amplifiers in series. As a consequence,  $S$ -parameter measurement is restricted to the transmission coefficient  $S_{21}(V_{ds}, V_g)$ , which in turn can be accurately calibrated.

Data reduction and analysis are based on the standard equivalent circuit of Fig.1-B. Extrinsic elements,  $C_{gs0} \sim C_{ds0} \sim 10$ – $20 \text{fF}$ , estimated from independent reflection measurements, and  $C_{gd0} \sim 2 \text{fF}$  measured as explained below, are minimized by the coplanar sample design. The gate capacitance  $C_g = C_{gd} + C_{gs}$  is splitted into gate-drain  $C_{gd}$  and gate-source  $C_{gs}$  contributions. These are associated to charge relaxation resistances  $R_{gd}$  and  $R_{gs}$ . We have  $R_{gd} \gg 1/C_{gd}\omega$  in the OFF state ( $V_g \gtrsim 1 \text{V}$ )

and  $R_{gd} \ll 1/C_{gd}\omega$  in ON state ( $V_g \lesssim 0$  V). Considering that  $Z_0 C_{gs0}\omega \sim 10^{-2}$ ,  $Z_0 C_{gd0}\omega \sim 10^{-3}$  and  $Z_0 g_m \sim 10^{-3}$  in the low-frequency range  $\omega/2\pi \leq 1.6$  GHz of our experiment, we obtain

$$S_{21} = S_{21}^0 + S_{21}^p(V_g) + S_{21}^a(V_{ds}, V_g) \quad \text{with} \quad (1)$$

$$S_{21}^0 \approx j 2Z_0\omega C_{gd0} \quad (2)$$

$$S_{21}^p \approx j 2Z_0\omega C_{gd}/(1 + j\omega C_{gd}R_{gd}) \quad (2)$$

$$S_{21}^a \approx -2Z_0g_m + \Delta S_{21}^p(V_{ds}) \quad (3)$$

being, respectively, the background transmission amplitude in the pinched state, the passive contribution at the onset of channel conduction in the zero bias state, and the active contribution under bias. Note that  $\Delta S_{21}^p = S_{21}^p(V_{ds}) - S_{21}^p(0)$  constitutes the imaginary part of  $S_{21}^a$ .

In order to check the validity of our analysis, we first consider the case of long FETs ( $l_g = 3 \mu\text{m}$ ) where gate capacitance contributions are easily resolved. Typical datas are exhibited in Figs.2. The inset of Fig.2.A shows both quadratures of the background transmission  $S_{21}^0(f)$ . From the slope of  $\Im(S_{21}^0(f))$  and Eq.(1) we deduce the small  $C_{gd0} \sim 1.5$  fF. Substraction of this contribution, keeping zero bias conditions, gives the  $V_g$ -dependent passive contribution  $S_{21}^p(f)$  shown in (Figs.2.A,B). In the ON state  $\Im(S_{21}^p)$  has a linear frequency dependence, whose slope is plotted in Fig.2-C as a function of  $V_g$ . The pinch-off transition appears here as a strong discontinuity associated with the divergence of the charge relaxation resistance  $R_{gd}$ . From the step amplitude and using Eq.(2), we deduce  $C_{gd} \simeq 170$  aF. This value is very representative of the five long samples which we have measured with an average of 160 aF and a standard deviation of 50 aF. A small monotonic dependence in  $\Re(S_{21}^p)(V_g)$  (Fig.2.A) is also observed which is possibly due to a residual substrate conduction, not taken into account in our analysis.

The active contribution (Figs.2.D-E) is obtained from the bias dependence of  $S_{21}(f)$  at constant  $V_g$ . The in-phase signal  $\Re(S_{21}^a)(f)$  is prominent and almost frequency independent. Slow frequency oscillations are reminiscent of calibration imperfections. Averaging  $\Re(S_{21}^a)$  over 0.2–1.6 GHz gives, according to Eq.(3), the transconductance as function of  $V_g$  shown in Fig.2.F. It has a maximum  $g_m \lesssim 3 \mu\text{S}$  close to the maximum observed at the dc ON-OFF transition. Representative values are  $g_m \lesssim 1\text{--}4 \mu\text{S}$ . The small negative part,  $\Im(S_{21}^a) \sim -\Im(S_{21}^p)$  in Fig.2.E, is a capacitive contribution due to a shift of the pinch-off under bias. Altogether, these measurements show that one can quantitatively analyze the dynamical properties of a single nanotube transistor. With  $g_m \sim 1.5 \mu\text{S}$  and  $C_g \sim 85\text{aF}$  (per gate finger), the transit frequency of the  $3 \mu\text{m}$  device of Fig.2 is  $f_T \sim 3$  GHz.

For short NT-FETs ( $l_g = 300$  nm in Fig.1) we observe smaller  $C_{gd}$  and larger  $g_m$  due to smaller channel resistance. Example shown in Fig.3 represents a new state-of-the-art for RF operation with a maximum of  $g_m(V_g) \gtrsim 20 \mu\text{S}$  (double gate fingers). Gate drain ca-

pacitance is  $C_{gd} \simeq 35$  aF (standard deviation 25 aF). Average values for the six short NT-FETs measured are  $g_m \simeq 12 \mu\text{S}$  and  $C_{gd} \simeq 35$  aF (double gate fingers). As seen on the dc characteristics in the inset of Figs.3.B, hysteresis is observed in these measurements which has been omitted elsewhere for clarity. Comparing our data for the 300 nm and  $3 \mu\text{m}$  devices shows that, within experimental uncertainty,  $C_{gd}$  scales with  $l_g$ . Assuming symmetric distribution of gate-drain and gate-source capacitances at zero bias, we obtain  $C_g/l_g \simeq 2C_{gd}/l_g \simeq 60$  aF/ $\mu\text{m}$ . With  $g_m \sim 10 \mu\text{S}$  and  $C_g < 30\text{aF}$  (per gate finger), the transit frequency of the 300 nm device of Fig.3 is  $f_T \gtrsim 50$  GHz.

These measurements show that NT-FET performances do improve drastically upon gate size reduction down to the nanometric scale (factor of 15 in  $f_T$  for a factor 10 in size). We now discuss possible routes for improvements. First one is to increase  $g_m$  by reducing access resistance due to the ungated NT sections at drain and source (see Fig.1-A). This effect is significant on devices using deposited CNTs, it is minimized with *in situ* CVD-grown NTs which are naturally p-doped in the absence of gating. Actually ungated regions are needed to reduce direct gate-drain/source capacitive coupling. Our values for gate capacitance are close to estimate for the geometrical contribution and in accordance with previous low-frequency measurements in similar top-gated devices [20]. They are still smaller than above numbers for the quantum capacitance. One may wonder whether better performance could be achieved by working closer to the quantum limit in using high- $\kappa$  and/or thinner oxides. This would improve gate coupling, but at the same time slow-down electron dynamics due to the screening of electronic interactions as discussed in Ref.[21]. In the absence experimental data and theoretical model, we shall rely on recent numerical simulations showing that transit frequency is maximized for  $C_Q \gtrsim 3\text{--}5 \times C_{geo}$  [14]. This condition which is close to our experimental realization. The most promising route is further size reduction below 100 nm as we have not observed evidence for saturation down to 300nm. Finally noise performance remain to be characterized, in particular the conditions for shot-noise limited resolution.

In conclusion, we have demonstrated high-transconductance SWNT-FET properties up to 1.6 GHz. We observe that high sensitivity is preserved, and that gate capacitance scales with gate length down to 300 nm. Transit frequencies as high as 50 GHz have been inferred, indicating that nanotube FETs are promising fast sensors.

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