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Short-circuit limitation thanks to a series connected VSC

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Abstract- Interconnection of medium voltage grids associated to the modulation of the transmission line impedance can improve system operation and power quality. However it also leads to rise of the short circuit power. To cope with this constraint and make this new distribution scheme a viable alternative to radial distribution in the future, investigations on short-circuit limitation with a particular line's compensator relying on a series connected Voltage Source Converter (VSC) (also called SSSC for Static Synchronized Series Compensator) has been achieved. Short-circuit limitation is also motivated because power systems grow and become more constrained (due to Distributed Generation (DG) widespread). This paper presents a new concept for a combined short-circuits circuit limiter and dynamic series compensator for medium voltage grids. In non-fault use, it is designed to regulate active and reactive power flow in order to optimize grid behavior. Indeed, coordination of several units dispatched through the grid could lead to more efficient grid exploitation (i.e. grid losses, loop flow, voltage drop reductions). During fault use (short-circuit) it will limit short-circuit currents to protect the grid and itself. Two innovative short-circuit limitation methods have been developed and experimented thanks to a test bench. The significant operation improvement is expected to justify the cost of the new device.

Key words: Distributed generation; Fault-current limiter; FACTS; Interconnected grid; Power controller; SSSC.

INTRODUCTION

The place of power electronics devices dedicated to electrical networks, transportation and distribution is rather small. This is due to several reasons: the cost [1], the reliability, the maintenance, the lack of needs, the system complexity, and even the culture. Only a new electrical context will imply a demand for power electronics devices in power systems (US or European).

This new context is about to take place thanks to Distributed Generation (DG) connected to low and medium voltage grids, essentially due to systems relying on renewable energies. This dramatically increases the number of uncontrolled power flow exchanges. In addition the growing of consumption it also expected. Then, grid will be more constrained.

Positive and negative effects will be observed concerning DG. It will reinforce the power facilities to meet the increase of energy demand, however, excessive introduction could cause a decline of the power system as intermittent power plants will be uniformly spread through the grid and because they will contribute to short-circuit currents. Distribution network operators (utilities) have to make investments (intellectual and financial) to cope with these mutations.

It has been shown that grid interconnections could reduce electrical constraints (i.e. voltage drops and lines losses) as power flows can use several way to feed customers, what lead to grid efficiency improvement [2]. However this will also increases short-circuit currents as line impedances values become smaller. Previous works showed that series

connected Power Electronic (Series Static Synchronous Compensator in our study) devices could interconnect grids and control power flows [3] [4] [5] in order to have an optimal exploitation (cost reductions). However the short-circuit problem is still not solved.

Conventional short-circuits limiters are based on pyrotechnic solutions but appear not flexible as they aren't reusable and also because they need long manual intervention after fault [6]. Although they have shown good results, previous works on short-circuit limiters based on Power Electronics (PE), relying on fast connecting high impedance, imply using additional equipment [7] if power flow control is needed.

In this paper we present two methods for short-circuit limitation supported by experimentations with the series connected PE device used for power flow control (i.e. relying on a Voltage Source Converter (VSC)). Presentation of the test bench appears at the end of the paper (APPENDIX). In the first part a method based on the use of a control strategy will be studied. In a second part, another solution exploiting directly the VSC topology will be presented.

I-FIRST METHOD: LIMITATION WITH CONTROL STRATEGY

A. Principle

This first method consists in creating a zero voltage difference in the grid in order to limit the fault-current rate. Fig. 1.a illustrates the case of a

downstream three-phases short-circuit of the VSC at $t = 0,2s$. If it is able to generate a voltage (v_s) which is the same voltage as the measured upstream voltage, v_{up} , (same modulus and phase shift), (Fig. 1.c); the short-current will decrease until complete cancellation (Fig. 1.b).

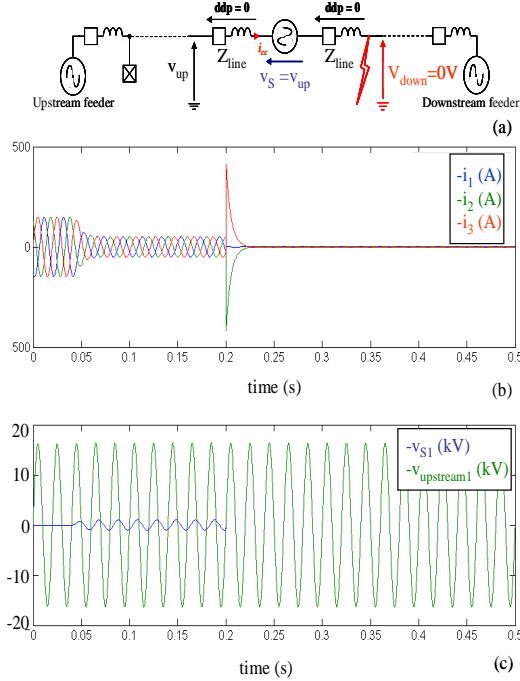


Fig.1: Three phases short-circuit limitation principle – (a) electrical circuit and (b, c) current and voltage waveforms

Eq.(1) gives expression of the fault-circuit current in each phase for the above described short-circuit. It can be seen that the limitation is sensible to the quality of the measurement.

$$i_{cc} = \frac{v_{amont} - v_s}{2 \cdot Z_{ligne}} \quad (1)$$

This also brings the need for the VSC to be able to generate in each phase a voltage with the amplitude of the network (generally 20kV RMS between phases in distribution grids). However in non-fault use, the DC bus voltage (V_{dc}) is not set to generate in each phase such a high voltage because only few kV are needed to realize power flow control [5]. So, the limitation is confronted to two major issues:

- The charge of the DC bus voltage when an i_{cc} detection occurs. Indeed, switches (IGBTs) losses are proportional to the DC bus voltage (V_{dc}), so in non-fault use V_{dc} must be smaller as possible [5] but at the fault detection V_{dc} must go from few kV to a value near 16,5kV (corresponding to the peak single phase voltage $\frac{20}{\sqrt{3}} \cdot \sqrt{2}$);

- The generation of three voltages close to the references. The smaller the difference between the

voltage upstream (or downstream) and the voltage injected by the SSSC, the smaller the fault current will be. Indeed, Fig. 1 presents the ideal case but due to filter and transformer a close loop control must be settled to have the outputs voltages close to the references.

The first limitation is solved thanks to the active part of the voltages injected through lines at the fault limitation. So, let's analyze the electrical values at the fault detection. In our case study, the voltage reference of the VSC is the voltage measured upward on the line in order to create a zero voltage difference. This voltage is composed of an active and a reactive part. Fig. 2 illustrates this property. VSC consumes active power what leads to the load of DC bus.

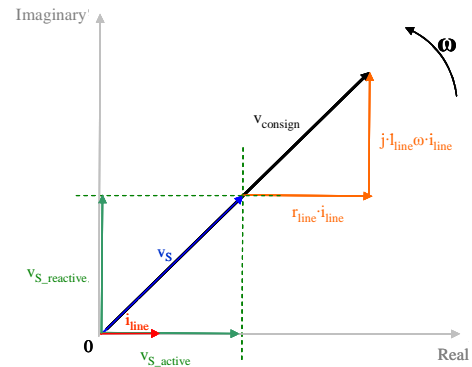


Fig.2: Electrical values of the VSC during limitation

The faster the load is, the faster the limitation will be. In some cases there may be a need to dissipate the excess of energy stocked by the DC bus through a crowbar (resistive dissipater). Indeed, V_{dc} can reach in some ms the needed value to generate a 16,5kV amplitude voltage in each phase but while still having a high i_{cc} . The DC bus capacitor value, C_{dc} , the value of the current and also the line parameter directly set the time response of the limitation (if the time response of the control of the outputs voltages is negligible).

Fig. 3 illustrates the case of a single phase fault (phase 1) in an interconnected grid at $t = 0,5s$. In order to present the most constrained case (higher i_{cc} rate for ground fault), grid structure is choose with a null neutral to ground impedance. The SSSC relies on three single phase VSC with crowbar devices.

Limitation benefits on currents can be observed in Fig. 3.a where the current's value of the fault phase is limited to some hundred Amperes, versus some kA without limitation. In the other phases, the current rate is cancelled as limitation is activated even in the non-fault phases (Fig. 3.b) in order to avoid line voltage unbalance.

Fig. 3.c shows the V_{dc} of each VSC (V_{dc1} , V_{dc2} and V_{dc3}). Rapid increasing of V_{dc1} followed by the crowbar action appears (in the non-fault phases no load is observed). Crowbar is still in action during

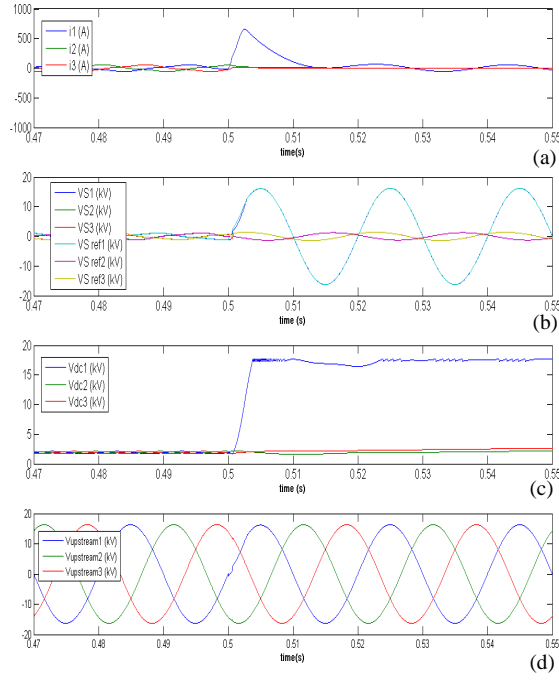


Fig.3: (Simulation results) Single fault-circuit limitation with three single phase VSC equipped with crowbar – Limitation with control strategy

the fault limitation but has low contribution. V_{dc1} is maintained to the needed value during the whole limitation. As V_{dc} fluctuates, if it decreases due to excessive crowbar action, this leads to i_{cc} increases which lead to V_{dc} increases and crowbar action and so on.

Grid voltages upstream of the limiter (V_{up1} , V_{up2} and V_{up3}) show the benefit effects on power quality and on the time response for a well designed device as they are not affected by the short circuit (Fig. 3.d).

As simulations introduce the principle with three single phases VSC, experimentations have to be done to completely validate the strategy and to observe the limitations induced by the use of a three-phase VSC.

B. Experimentation

This strategy has been experimentally validated thanks to a hybrid test bench (APPENDIX). It consists in a real-time software which models electrical grids (20kV) (Table 2) interfaced with a physical three phase 10kVA VSC (Table 3) which injects an image of its output voltages into the simulation in order to have a closed loop functioning.

Tests have been realized for four different short-circuits (symmetrical, non-symmetrical, to the ground and isolated of the ground), upstream and downstream the structure. In this paper two cases will be presented, the first will be a three phase fault and the second a single phase fault.

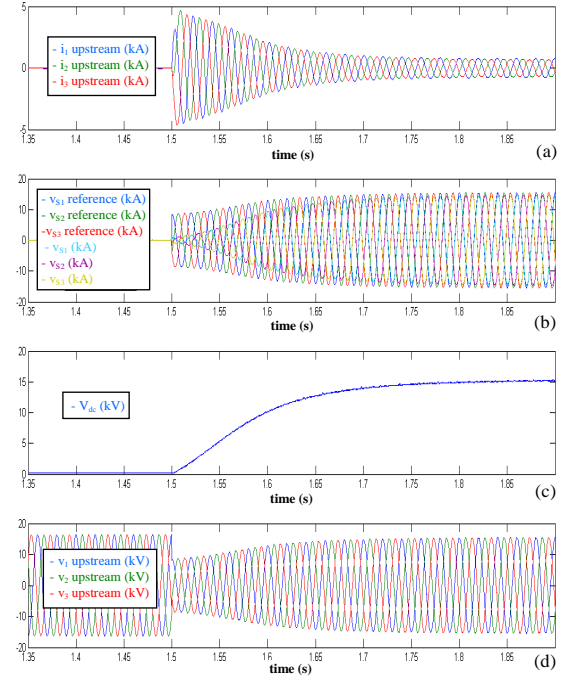


Fig. 4: (Experimentation results) Electrical values during three phases short-circuit limitation thanks to a three-phases VSC – Limitation with control strategy

Tests realized upstream and downstream the devices lead to the same results.

Fig. 4 illustrates the case of a three phase short-circuit (symmetrical isolated from the ground) downstream of the structure at $t = 1.5s$. Positive effect on current's amplitude can easily be seen on Fig. 4.a. Without limitation the current will be up to 5 kA. The time response limitation is due to the VSC's parameters which are not optimized in this test. Indeed, the test bench is a generic, not dedicated application. In Fig. 4.b voltages delivered by the VSC and their references can be observed. Fig. 4.c concerns the load of V_{dc} and finally Fig. 4.d grid's voltages upstream ($v_{upstream}$) the VSC. Differences with simulation results are due to non optimized parameter value, however it validates the strategy.

The second experimentation concerns a single phase fault upstream of the system in phase 1 (Fig. 5). In this case the limitation is non-effective as the fault current is partially limited and also because in the non-fault phases (2 and 3), the currents rise. Indeed, the three phase converter has only the possibility to generate equilibrate system (i.e. $v_{S1} + v_{S2} + v_{S3} = 0$) which is in contradiction with the need for a limitation for a non-equilibrate fault (phase to ground faults).

In the case of earth faults, there is a need for the VSC to be able to generate a homopolar component. So, series connected single phase VSC are required to cover all fault limitation cases.

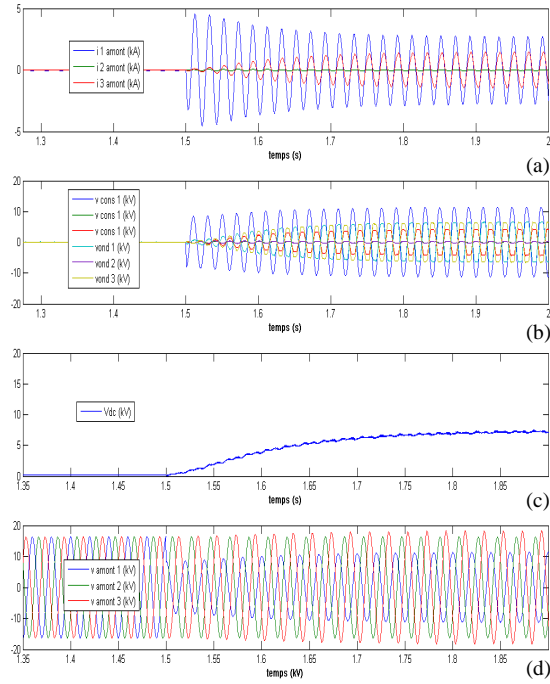


Fig. 5: (Experimentation results) Electrical values during single phase short-circuit limitation thanks to a three-phases VSC – Limitation with control strategy

C. Conclusion

The principle has been validated; limitations have been shown thanks to experimental tests as a three phase device can't be used. Moreover, the final control architecture is complex (Fig.6), because the reference is processed through lots of elements and especially with a time anticipating function [8] and resonant controllers [9].

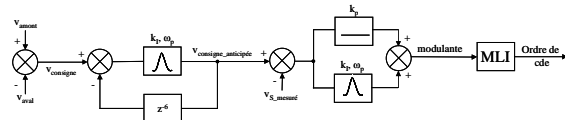


Fig. 6: Complete control scheme for fault current limitation with series connected VSC

The use of a time anticipating function is needed because i_{cc} limitations are very sensitive to phase shifting between the reference (v_{ref}) and the output signal (v_s). The higher the delay between the reference and the output voltage is, the higher the fault current will be. By the use of resonant controller time anticipation can be taken [8]. Resonant controllers are also used to allow a close matching between v_{ref} and v_s without using Park transformation [10]. In the same way that integrator controllers (i.e. Proportional and Integer) process continuous signals, resonant controllers process signals with determinate frequency (i.e. $f = 60\text{Hz}$ or 50Hz in our cases). Indeed, these controllers (2) have an infinite module value at the defined

working frequency which enables in close loop, a close matching between v_{ref} and v_s . (2) illustrates this property as $|C_R(j\omega_0)|$ has in theory an infinite value with $\omega = \omega_0 = 2\pi f$.

$$C_R(p) = K_p + \frac{K_I}{p - j\omega_0} + \frac{K_I}{p + j\omega_0} = K_p + \frac{2K_I p}{p^2 + \omega_0^2} \quad (2)$$

However the main drawback is that this principle is very sensitive to the quality of the measurements to create V_{ref} and the settlement of the controller parameters which are in great number. In addition, the limited current can't be determined analytically. So, to overcome these limitations a simpler strategy has been investigated.

II SECOND METHOD: LIMITATION WITHOUT COMMUTATIONS

A. Principle

In order to increase the reliability of the current limiter, a key point of such systems, investigations have been done and a new strategy has been found. It still consists of high impedance insertion but with the aim of limiting VSC constraints and the possibility of determining the value of the limited fault current.

The simplest strategy consists in stopping IGBTs commutations at i_{cc} detection. Then a current rectifier behaviour (Fig. 7) will be observed as the current flows only through diodes. This will result in a C_{dc} charging, until a voltage determined by the amplitude of V_s .

When V_{dc} is equal or above the output voltage filter (v_s), the current through electronic switches will cancel itself ($i_{Lf} = 0$). Fig. 8 presents simulation results for a single phase fault current case at $t = 0,15\text{s}$ and using three single phase VSC.

Good results for fault circuit limitation can be observed in Fig. 8.a where the fault-current pass

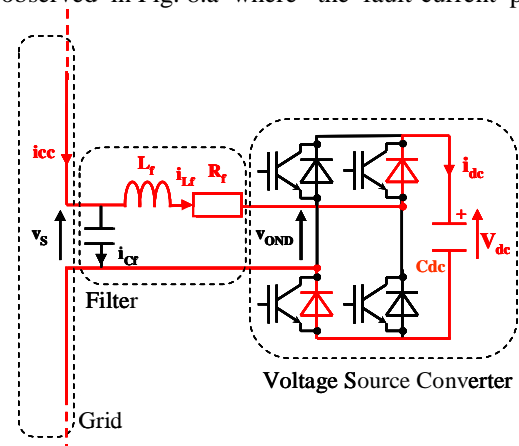


Fig. 7: Current rectifier behaviour of the SVC with off state IGBTs

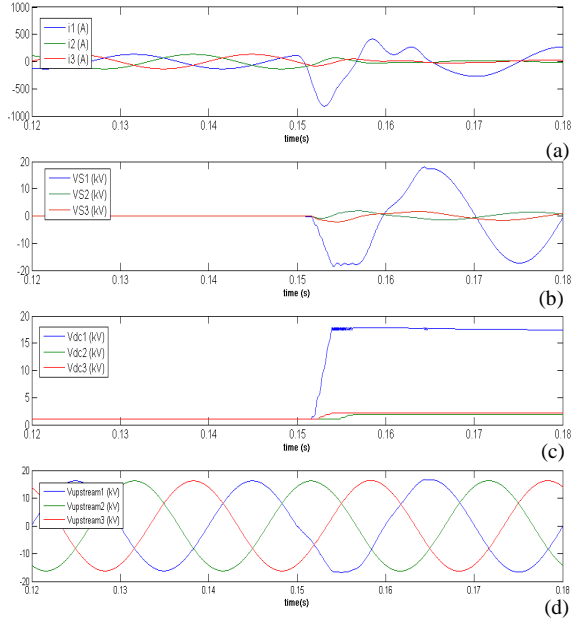


Fig. 8: (Simulation results) Single phase fault-circuit limitation with three single phase VSC equipped with crowbar – Limitation without commutations

from 100A in normal use to a value limited to 200A after a peak at 800A. This first result validates the strategy as without limitation the current will have an amplitude of some kA. In non fault phases the current decreases until reaching a value near zero Amps.

Fig. 8.b presents the output voltages of the VSC. In this studied case as the grid has null impedance for the neutral to earth connection the VSC support the grid voltage in each phase after a transient (i.e. 11,5kV RMS).

Fig. 8.c presents DC bus voltages (V_{dc1} , V_{dc2} and V_{dc3}). V_{dc1} increases until it reaches the amplitude of the line's grid ($v_{upstream1}$). It appears a low rise of v_s 's amplitude following the fault so crowbar comes into limitation to protect the DC bus until the voltage returns to his original value. Causes of the rise of v_s will be developed in the three phase fault case. Contrary to the other method, the crowbar is only active during this transient.

Finally, Fig. 8.d lets appear the low disturbance on grid voltages.

This study validates the limitation method. Moreover, it appears more interesting than the other principle as:

- Limitation is simple and effective. Few parameters are employed, so reliability is higher;
- Crowbar only process during the transient, so fewer losses have to be dissipated with this method.

The same method is used, but for a three phases fault (Fig. 9). Good results can be observed too with well designed parameters. Currents through electronics devices are presented on Fig. 9.a. It appears that only currents flow in the rectifier

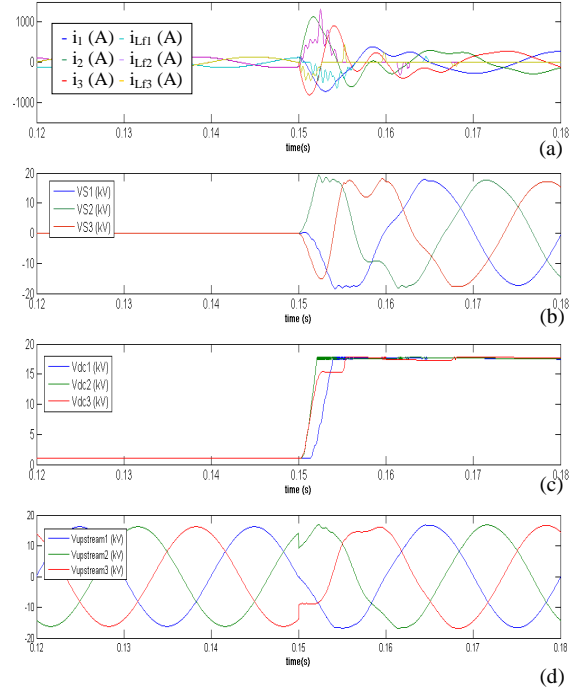


Fig. 9: (Simulation results) Three phase fault-circuit limitation with three single phase VSC equipped with crowbar – Limitation without commutations

during the transient. Theirs duration are 10ms or 20ms. For the case of a 20ms response, it is due to the DC bus voltage which does not reach the $v_{upstream}$ amplitude in 10ms. This is the case for V_{dc3} (Fig. 9.c). Finally Fig. 9.d shows constraints on the grid voltage which are acceptable as the transient is fast.

This study presents interesting issues:

- The limitation time response is at maximum 20ms;
- Current is almost zero in electronics after the transient. The low remaining current allows the compensation of C_{dc} losses and V_{dc} decreases;
- IGBTs and diodes can be dimensioned differently as they don't have the same stress because IGBTs are not crossing by the fault current, only the non-fault, when the system is used for power flow regulation.

The only drawback is the high voltage rate needed by the device. Indeed, as the previous method, the structure has to be dimensioned to support the grid voltage.

After the transient, i_{cc} amplitude will be defined by the capacity value of the filter's capacitor because the current rectifier behaviour results in an infinite impedance value. Thus design of the output filter is crucial. Indeed, the lower the value of C_f will be, the lower i_{cc} will be. This will be more developed in the discussion part.

Approximate expression of current's amplitude through electronic switches has been set in order to

provide an estimation of the design. This has been done as a function of the filters and VSC parameters (3). It doesn't give an exact value nor replaces simulation and experimentation but gives an approximate value to design the system and also allows evaluating the influence of each parameter on the limitation. We consider that the output voltage is null at $t = 0$ s (fault apparition) and that the expression is valid for $t = [0 ; 20\text{ms}]$.

$$I_{\max} = V_{s_max} \left[\frac{2 \sin \frac{\varphi}{2}}{\sqrt{R_f^2 + L_f \omega^2}} \cos \left(\frac{\varphi}{2} + \varphi_2 \right) \right]$$

with

$$\varphi = \arctan \left(\frac{R C_{dc} \omega}{1 - L_f C_{dc} \omega^2} \right) \quad (3)$$

$$\varphi_2 = \arctan \left(\frac{L_f \omega}{R_f} \right)$$

This expression has shown the important role of C_{dc} . Indeed, the current rate is very sensitive to the difference between v_s and V_{dc} which increases as C_{dc} increase (3). This expression lead to a limit value of $C_{dc} = 80\mu\text{F}$ in order to have a current through electronics switches at a maximum of 1kA. Simulations have validated this value.

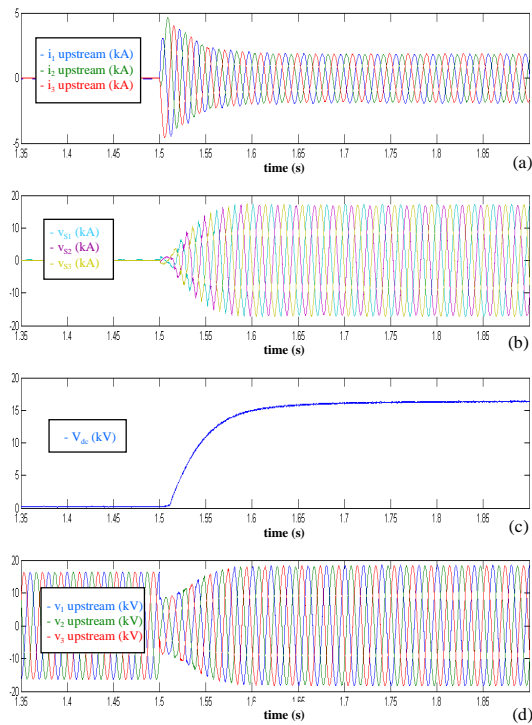


Fig. 10: (Experimentation) Electrical values during three phases short-circuit limitation thanks to a three-phases VSC – Limitation without commutations

B. Experimental results

Same experimentations than with the other strategy have been successfully carried out with this method. Fig. 10 shows results for a three-phase limitation.

I_{cc} decreasing is observed in Fig. 10.a to a value defined by the filter capacitor which is not optimal in our test-bench. However this emphasizes the viability of the method.

Tests lead for single phase faults give the same conclusion as for the previous method: single phase VSC is not adapted for earth faults. So the results are not presented here.

Contrary to the previous method the value of the limited current is known. We can also underline the simplicity of the method and especially the fact that the IGBTs's diodes may be dimensioned to the maximum short-circuit current through the structure as IGBTs can be dimensioned for non-fault applications. However, as the previous method it still implies that the VSC needs supporting the maximum grid voltage.

DISCUSSION

Through this paper series connected VSC has shown its possibilities to limit fault currents. This can be an additional function to a device which can already fulfill power flows control in order to optimize the grid functioning. The significant operation improvement is expected to justify the cost of the new device. Moreover, grid losses reduction realized in normal use can be sufficient to be economically interesting. Study case with coordination of several SSSC units with high DG penetration level have to be done to estimate the money saving.

The second limitation method allows fixing the limited current value as it is directly linked to the capacitor value of the output filter C_f . Fig. 11 gives limitation examples for simulation of a three phase fault limitation with three different cases of filter parameter (Table 1).

1 ^{er} jeu	2 ^{ème} jeu	3 ^{ème} jeu
$L_f = 0,36 \text{ mH}$	$L_f = 0,72 \text{ mH}$	$L_f = 1,08 \text{ mH}$
$C_f = 100 \mu\text{F}$	$C_f = 50 \mu\text{F}$	$C_f = 33 \mu\text{F}$

Table 1: Filters parameter influence on permanent limited fault current amplitude

The lower the capacitor value is, the more the limitation will be effective. (4) gives expression for i_{cc} during limitation. It is available for each fault phase whatever the kind of short-circuit, as the grid architecture has been choose with a null impedance between the neutral point and the ground.

$$i_{cc} = \frac{V_{grid}}{\sum R_{line} + j \sum L_{line} \omega - \frac{1}{j C_f \omega}} \quad (4)$$

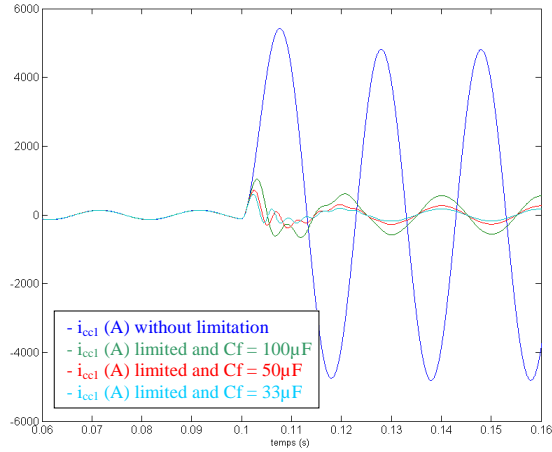


Fig. 11: (Experimentation) Electrical values during three phases short-circuit limitation thanks to a three-phases VSC – Limitation without commutations

It can be noticed that the reactive part of the line is compensated by the limiter.

Studies about physical realization have been done thanks to a modular conception and relying on losses estimation [11]. A dimensioning tool has lead to the lowest losses thanks to a good choice of components.

CONCLUSION

Two novels methods for short-circuit limitation relying on a series connected VSC have been developed and experimentally validated. The interest is to use a device which already fulfils a non-fault function (power flow control or Dynamic Voltage Restorer) in order to save losses (money) and to have a better power quality.

In addition, this system does not only protect the grid but also itself and above all it proposes a solution for medium voltage grid interconnections. The second method appears to be more efficient than the first one as the control is simpler, efficient and because very few losses are observed after the transient. The other advantage is the possibly to determine the value of i_{cc} after the transient, what helps dimensioning the system.

In conclusion series connected power electronic devices appear very interesting in the case of grids exploitation with DG connection and to solve the problem of fault current rate increase.

APPENDIX

Table 2 gives the grid parameters use for tests (in simulation and during experimentations).

RMS voltage between phases	20kV
Apparent power	1143kVA
Load aggregate number	13
Line section number	14

Table 2: Grid parameters use for simulations and experimentations

Fig. 11 presents an overview of the test bench used for experimentations.

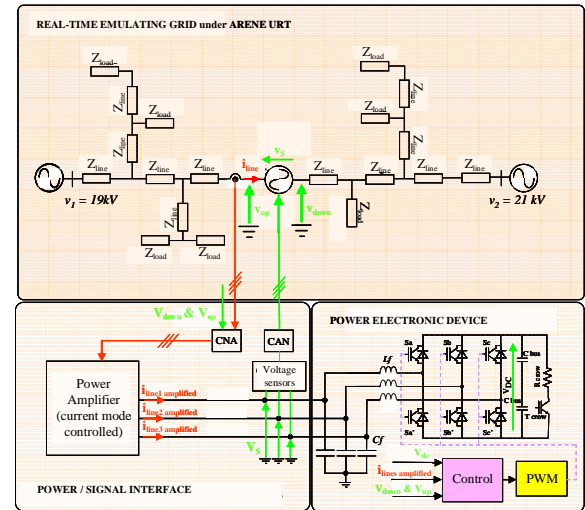


Fig. 11: Overview of the test bench used for experimentations

It is composed of three parts:

- The real-time emulating network where the physical description and the simulation are done;
- The interface. It converts line's currents from simulation into power signals which are then send to the VSC. It also digitalizes VSC's output voltages and inserts them into the simulation to have a closed loop behaviour;
- The physical VSC. Composed of a three phase voltage converter connects to the power interface thanks to a filter (Table 3).

Parameters	Abbreviation	Value
Filters :	L_f	0,36 mH
- Inductor	C_f	100 μ F
- capacitor		
Apparent maximal power	S_N	10 kVA
Sample frequency	T_S	100 μ s
Commutation frequency	F_C	10 kHz
Max Vdc value	V_{DC}	400V
Capacitor DC bus value	C_{bus}	1,1 mF

Table 3: Physical characteristic of the VSC

Fig. 12 gives a picture of the test bench where all the components appear physically.

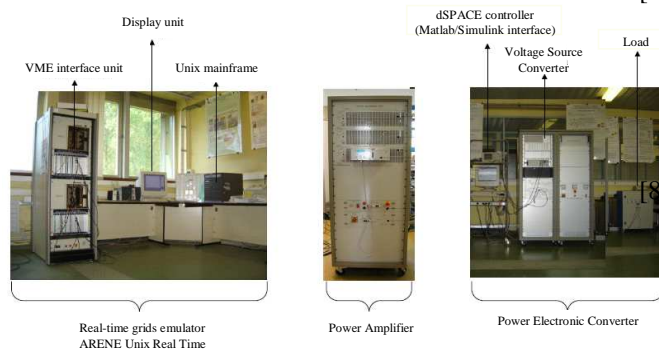


Fig. 12: Overview of the test bench use for experimentations

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