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OSCILLATOR SYNCHRONISATION PROBLEM IN A BiCMOS ANALOG-DIGITAL INTEGRATED CIRCUIT DEDICATED TO A CAPACITIVE PRESSURE SENSOR

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ABSTRACT : A new type of hybrid pressure sensor has been realised using silicon/Pyrex capacitive sensing cell and a digital output BiCMOS transducer. A ratiometric scheme has been used to self-compensate thermal drifts and nonlinearities. Two demonstrators have been designed, mounted and tested. The first one, implemented with four chips to evaluate the feasibility, is characterised by a relative sensitivity close to -1.85%/bar, a nonlinearity in the order of 1.1%FS and an offset thermal coefficient smaller than 20 ppm/°C. A simple analytical model specifies that stray capacitors induce a decrease in sensitivity and a nonlinearity increase. The second demonstrator has been implemented with two integrated chips. It consists, on the one hand, of two pairs of converters and counters integrated in the same chip, and on the other hand, of a reference and measurement capacitors into the same sensing cell. This configuration reduces stray capacitors by a factor two but provokes interference and synchronisation phenomena. Characterisation and PSPICE modelling have permitted to understand, to localise causes and then to propose some solutions to avoid or minimise these problems.

INTRODUCTION

Since few years, pressure sensors are widely used in automotive, aeronautics, biomedical and environmental applications. The recent development of macro and micro-systems which can integrate multi-sensor networks requires the concomitant development of digital-output sensors. Among many analog-to-digital conversion techniques [1]-[3], a simple solution consists in using variable oscillators coupled with counters. In addition, this solution allows the use of sensing capacitors which provide such advantages as low power consumption, small temperature dependence and high sensitivity [4].

In accurate sensors, the thermal drift [5] and the nonlinearities [6] are compensated. Conventional techniques of compensation turn out to be efficient but expensive.

In what follows, capacitive pressure sensor demonstrators based on a digital ratiometric principle are presented. They are both essentially composed by a silicon/Pyrex capacitive pressure sensing cell and an analog-digital BiCMOS transducer. This type of converter is based on the principle of charge and discharge of a capacitor with a constant current. The feasibility of this sensor type has been evaluated with a four chips hybrid demonstrator. A two-chip implementation has been designed to yield a high value of self-compensation for nonlinearities and thermal drifts, with stray capacitors as small as possible in order to obtain the best features.

SENSOR DESCRIPTION

Sensing Cell

Designed and realised in LAAS, the sensing cell is basically a miniature variable capacitor composed by a silicon diaphragm and a metal plate deposited on a rigid Pyrex 7740 substrate [7]. Silicon and Pyrex are bonded by means of anodic bonding [8]. This type of cells can be electrically modelled by a pure capacitor at medium frequencies (5 to 500 kHz) because of its negligible conductance (≈ 10 nS) and access resistance (few ohms). It presents a high pressure sensitivity, an excellent long term stability and can withstand elevated overpressures [9]. The specimen used to implement the sensor demonstrator has a capacitance in the order of 34 picofarad at rest.

The experimental behaviour for pressures P between 1 and 6 bars and for temperatures θ varying from -10°C to 90°C is almost linear and can be modelled by :

$$C(P,\theta) = C_o(\theta) + S(\theta)\, P + NL(P,\theta) \qquad (1)$$

where C_o is the sensor capacitance when P=0, which is referred to as the offset capacitance hereafter ; S is the sensitivity parameter depending on the diaphragm structure and its geometry (+ 1.35 pF/bar in this case) ; and NL is the nonlinearity : with respect to a linear model computed using the least squares curve fitting,

the nonlinearity, expressed in percentage of the full measurement scale, is in the ± 2.5 % FS range.
The thermal behaviour of the sensing cell can be evaluated by both the offset and the sensitivity thermal coefficients respectively TC[C_o] and TC[S] defined by TC[X] = $\partial X/(X\partial\theta)$. As the drifts are quasi-linear between -10°C to 90°C, and very small, these thermal coefficients can be approximated by constants : TC[C_o] ≈ - 60 ppm/°C and TC[S] ≈ - 220 ppm/°C.

Interface circuit

The circuit described in this paper consists of two main blocks : (i) an analog one with two triangular oscillators and (ii) a digital one which gives an 11-bits output number proportional to the capacitance and then to the pressure [10].

Analog block : Capacitance/Period Converter. Several alternative approaches can be used to convert capacitance variations into electrical signal [1][11][12]. This converter has been designed to generate a triangular wave-form with time period proportional to the capacitance. It operates on the principle of charge and discharge of a capacitor with constant current, between two thresholds voltages V_L and V_H. As it is shown in Fig. 1, this type of oscillator can be modelled by a charging current source (I_o), a discharging one ($2I_o$), a Metal-Oxide-Semiconductor Transistor (MOST) switch and a Control Logic Circuit (CLC) which drives the switching on and the switching off.

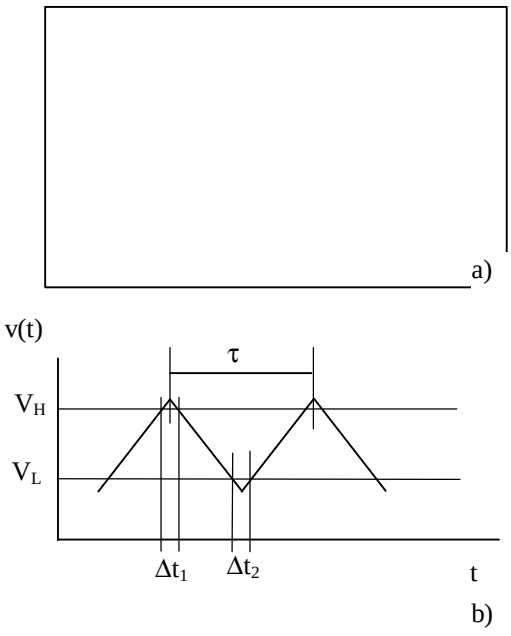

Fig. 1 : Principle of the capacitance to time period converter : a) simplest electric scheme ; b) wave-form of the voltage signal.

The CLC consists of two threshold NPN-input comparators and a RS logic-gate.

Considering the switching delay Δt, the theoretical time period τ of the signal is given by :

$$\tau = \tau_d + kC \qquad (2)$$

where $\tau_d = \Delta t_1 + \Delta t_2$

and $k = 2 \times \frac{(V_H - V_L)}{I_o}$.

Even if the CLC has been designed with fastest components, the offset τ_d remains close to 350 ns (≈ 4 Δt).
In order to keep k as constant as possible, threshold voltages are defined by using a high stability reference voltage source (V_{ref}) called "Band-gap source". By design, the theoretical current value I_o is 20.2 µA and the peak-to-peak amplitude (V_H - V_L) of the oscillations is equal to 1.2 V.
Detailed analysis of converter's offset and sensitivity reveal the existence of a leakage current I_f and stray capacitors C_s. In the order of 450 nA, I_f is essentially due to comparators' input impedance (Z_{in}) while intrinsic stray capacitors have been estimated in the range of 3 pF. Moreover, in addition to the current source thermal behaviour, these two parameters make the converter's thermal drifts much more important (e.g., TC[offset] exceeds 0.2%/°C).
The easiest improvement to reduce significantly the leakage current consists in replacing the NPN-input comparators by NMOS input comparators.

Digital block : Ratiometric Digital Output. This block consists of two converters connected to the capacitors C and C_r where C stands for the sensing cell and C_r for a constant reference capacitor. The main goal of this block is to generate a binary number proportional to τ_r/τ (i.e., C_r/C) in order to obtain a maximum level of self-compensation for both nonlinearities and thermal drifts [13].
While the reference counter counts a constant number N_o of periods τ_r, the second one counts N periods τ such as $N\tau = N_o\tau_r$. Consequently, N is given by :

$$N = N_o\, \tau_r / \tau \qquad (3)$$

Theoretically, from eqn. (2), if τ_d << kC, the relationship (3) being independent of the current. So, its drifts have no impact on the response and then N becomes proportional to C_r/C.

SENSOR CHARACTERISATION

In order to identify the primary parameters determining the sensor behaviour, two demonstrators were implemented and tested.

Four chips hybrid sensor

This mock-up results from the assembly of two sensing capacitors and two distinct but similar converters. Pressure is only applied to one of the sensing cells, the other being used as a reference capacitor.
As the devices are matched, this implementation offers a high level of self-compensation [13].
Figure 2 shows the ratio $R = N/N_o$ between 1 and 6 bars for temperatures from -10°C to 90°C.

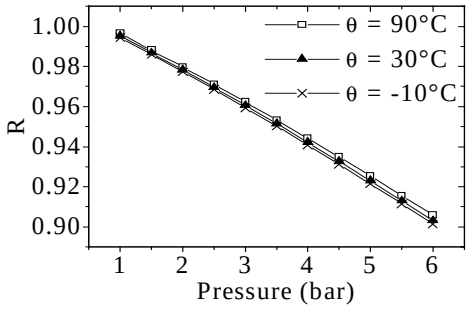

Fig. 2 : Normalised response of the four chips mock-up; measurements carried out from -10°C to 90°C.

Irrespective of temperature, the response is almost linear. The nonlinearity is situated in the range of ± 1.1 % FS. As expected, it is significantly less than that of the sensing cell but not as low as computed in [9]. In addition, the relative sensitivity of this demonstrator is about 1.85%/bar. It is quite two times smaller than that expected.
These results can be explained by stray capacitors C_s connected in parallel to C and C_r. With the simplest model :

$$R = \frac{C_r + C_s}{C + C_s} \qquad (4)$$

C_s has been evaluated in the order of 10 pF. Few experiences have shown that these stray capacitors are essentially due to interconnections (with 3 pF from intrinsic capacitors). They introduce a decrease of sensitivity (- 10%) and make the nonlinearity increase (+ 0.7 %FS) [13].

As the offset thermal coefficient of this demonstrator doesn't exceed 20 ppm/°C (up to one hundred lesser than that of the converter), the self-compensation of thermal drifts is very efficient.

Two chips implementation

This mock-up has been mounted using two converters integrated into the same chip and a silicon/Pyrex sensing cell which contains both the reference and the measurement capacitors. The main goal of such an implementation is to obtain the best possible "matching" of converters, to reduce as much as possible stray capacitors and to assess the feasibility of integration.
Figure 3 represents the comparison between the experimental sensor response and the computed one C_r/C.

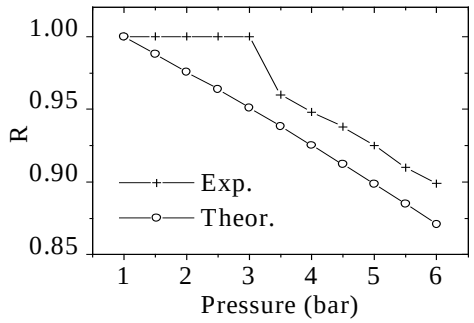

Fig. 3 : Comparison between experimental and theoretical response of the two-chip implementation sensor.

It clearly appears that the sensor does not work normally for pressures lower than or equal to 3 bars. That corresponds to a difference of capacitance between C and C_r close to 2.5 pF. For pressure greater than 3 bars, the "semi-integrated" sensor seems to work correctly. Even if there are some interference, its response is quasi-linear with a relative sensitivity in the range of - 2.5%/°C. This result indicates that stray capacitors have been reduced by two.

DISCUSSION

Phenomena description

Figure 3 shows that the ratio R remains constant and equal to 1 for $P \leq 3$ bars. This implies that the two oscillators are working at the same frequency, or in other words, they are synchronised.
Experimentally, the two oscillator output signals have been visualised. It appears that each transition relative to a switch commutation on one oscillator introduce a parasitic voltage pulse on the other. Figure 4 represents these two signals with $\tau_r \approx 4\tau$ for a better clarity.

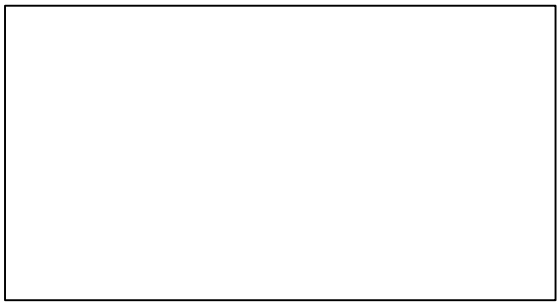

Fig. 4 : Schematic representation of oscillators output signals (voltage vs. time) with $\tau = 4\tau_r$.

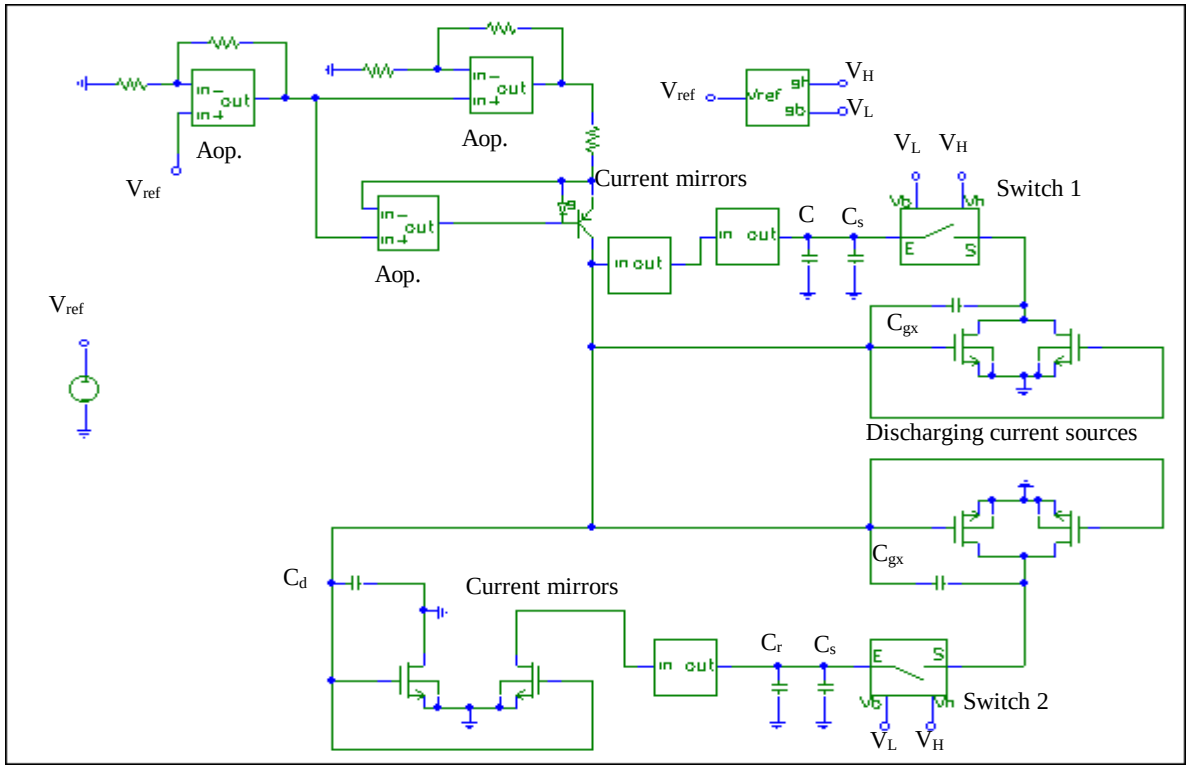

Fig. 5 : Simple electric sensor model with PSPICE level 2.

PSPICE Modelling

The complete sensor behaviour has been modelled with PSPICE level 2 as it is shown on Fig. 5. The switch block consists of MOST switch with its CLC.
By design, a switch commutation generates charges injection that provokes a current pulse and then a voltage variation on the triangular wave-form. According to the simple electrical scheme (Fig. 5), it appears that a direct link connects oscillators together through the discharging current sources. Thus, this pulse can be transferred on the other oscillator through MOST grid-to-channel capacitance (C_{gx}). Figure 6 shows the simulated effect of the reference oscillator switch commutation on the triangular wave-form.

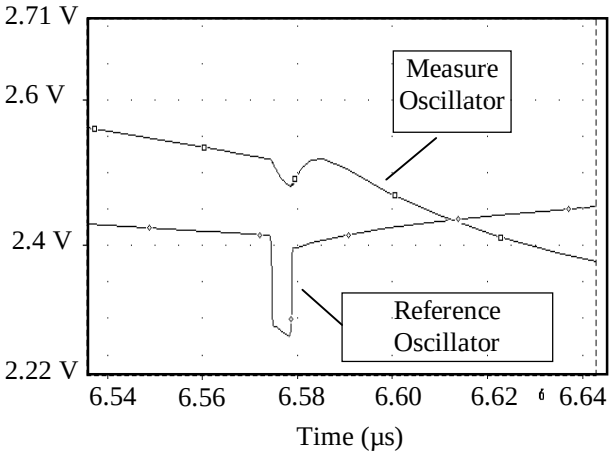

Fig. 6 : Modelling of interference between oscillators during a commutation.

In a first approximation, the magnitude (ΔV_C) of these pulses on the triangular signal is directly proportional to the d.c. voltage source (V_{DD}) as it is described in the relation (5).

$$\Delta V_c = \frac{C_{eq}}{C_{eq} + C} \times \Delta V_{DD} \qquad (5)$$

where C_{eq} is the equivalent grid-to-channel capacitance of MOST switch and C is the measured capacitance.
With the nominal value V_{DD} = 5 V, the experimental peak-to-peak magnitude reaches 50 mV. Thus, even if

this voltage pulse is strongly reduced on the other triangular wave-form, it still exists. So, for C slightly greater than C_r, the switch commutation in reference oscillator introduce a pulse which make the other oscillator commute prematurely. It implies that each time commutations happen quasi-simultaneously on both oscillators, it makes the ratio remaining constant.
This problem introduce measurement errors in the range of 5 %.

Design optimisation

The most efficient method to eliminate the oscillators synchronisation is to design two distinct oscillators with their own current source. But, this method procures two main drawbacks : first, the integrated circuit area will be more important and then makes the sensor more expensive ; secondly, the matching between current sources will be poor due to component dispersion. That implies a worst efficiency of self-compensation (see section "Four chips hybrid sensor").
From eqn. (5), one solution to minimise pulses magnitude and make them negligible consists in reducing the ratio C_{eq}/C.
Assuming that MOST capacitances (C_{gs} and C_{gd}) are directly proportional to the channel width W, electrical simulations have shown that one method consists in reducing this parameter (i.e. MOST dimensions). But, even if the voltage variation due to switch commutation seems to be proportional to W, the MOST dimensions can't be indefinitely reduced. Effectively, the MOST output conductance increases while its sizes decrease. Thus, the discharging current will not be constant and then disrupts sensor operation.
So, an other way to minimise this coupling effects is to add a decoupling capacitance C_d between current mirror grids and ground. PSPICE simulations, as it is shown in Fig. 7, indicate the attenuation efficiency of C_d on the transmitted pulse magnitude.

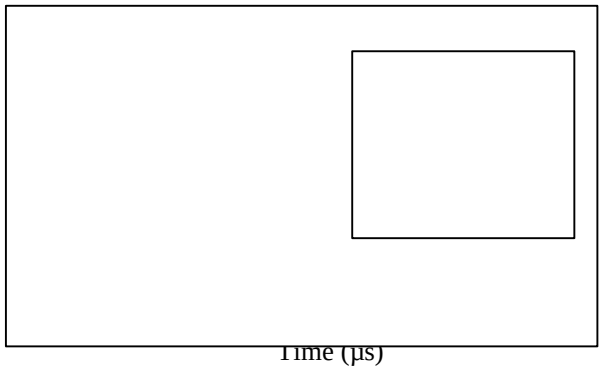

Fig. 7 : Simulation of pulse attenuation efficiency of a decoupling capacitance.

The last designed circuit includes a 30 pF integrated capacitor. The experimental response of this new two-chip implementation sensor is illustrated on Fig. 8 with $C - C_r = 2.5$ pF at rest.

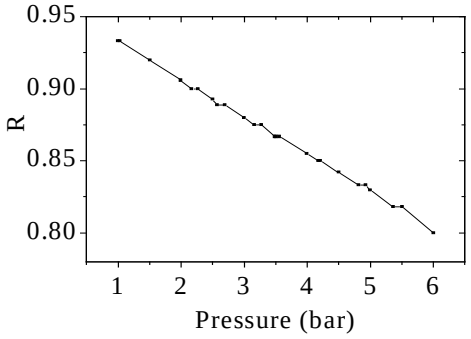

Fig. 8 : Example of a sensor response with $C - C_r = 2.5$ pF ; visualisation of small errors introduced by oscillator synchronisation.

Experimental pulse magnitudes remain greater than that simulated but the measurement errors on the sensor response have been reduced by 10.

CONCLUSION

The pressure sensor described here is an hybrid association of a capacitive sensing cell in Silicium/Pyrex technology, and a capacitance/frequency transducer based on the charge and the discharge of a capacitor with constant current. The modelling response of each part allows us to explicit the transfer function of the sensor. Accurate evaluation of different parameters is achieve by both numerical simulation and experimental characterisation of the sensing cell and the electronic circuit. Studies on a simple and a ratiometric architecture show the feasibility of pressure sensor which is able to mainly self-compensate nonlinearity and drifts. In the range of ten percent of the offset frequency, the demonstrator nonlinearity is less than one percent and its thermal coefficient is about twenty parts of million by Celsius degree. Numerical simulations show that to optimise ratiometric sensor performances, it is necessary to use a perfect symmetrical architecture. These optimal performances can be obtained by integrating both converters on the same silicon substrate. Experimental results also point out several problems of interference between oscillators through grid-to-channel capacitances. One way to minimise these coupling effects is to add a 30 pF decoupling capacitance at least. All the results obtained allow us to conclude that measurement principles and the associated technologies used are adequate to develop a new family of miniature pressure sensor which can be relatively accurate (about 1% of the full scale), cheap and easily connected with numerical communication networks.

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REFERENCES

[1] Mitsuhiro Yamada, Member, IEEE, and Kenzo Watanabe, Fellow, IEEE, "A Capacitive Pressure Sensor Interface Using Oversampling Δ-Σ Demodulation Techniques", IEEE Transactions on Instrumentation and Measurement, Vol. 46, No. 1, Feb. 1997, pp 3-7.

[2] H. Matsumoto, H. Shimizu and K. Watanabe, "A Switched Capacitor Charge Balancing analog-to-digital converter and its application to capacitance measurement", IEEE Tans. Instrum. Meas., vol. IM-36, Dec. 1987, pp. 873-878.

[3] C. A. Leme, P. Malcovati and H. Baltes, "Oversampled interface for IC sensors", in Proc. Instrumentation and Measurement Tech. Conf., 1994, pp. 652-655.

[4] P. Pons and G. Blasquez, "Low-cost high sensitivity integrated pressure and temperature sensor", Sensors & Actuators A, vol. 41-42, 1994, pp. 398-401.

[5] F.V. Schnatz, U. Schöneberg, W. Brockherde, P. Kopystynski, T. Mehlhorn, E. Obermeier and H. Benzel, "Smart CMOS capacitive pressure transducer with on-chip calibration capability", Sensors & Actuators A, Vol. 34, 1992, pp. 77-83.

[6] B. Puers, E. Peeters, A. van den Bossche and W. Sansen, "A Capacitive Pressure Sensor with Low Impedance Output and Active Suppresion of Parasitic Effects", Sensors & Actuators A, Vol. 21-23, 1990, pp. 108-114.

[7] G. Blasquez, Y. Naciri, P. Blondel, N. Benmoussa and P. Pons, "Micromachined Silicon Capacitive Sensor", Proc. 2nd Int. Conf. Passive Comp. Mat. Tech. Processing, Paris 18-20 nov. 1987, pp. 142-146.

[8] T. Rogers and J. Kowal, "Selection of Glass : Anodic bonding conditions and material compatibility for silicon-glass capacitive pressure sensors", Sensors & Actuators A, Vol. 46-47, 1995, pp. 113-120.

[9] P. Pons, G. Blasquez, R. Behocaray, "Feasability of Capacitive Pressure Sensor Without Compensation Circuits", Sensors & Actuators A, vol. 37-38, 1993, pp. 112-115.

[10] Ph. Dondon, Ch. Zardini and J. L. Aucouturier, "BiCMOS integrated circuit for capacitive pressure sensors in automotive applications", Sensors & Actuators A, vol. 37-38, 1993, pp. 596-599.

[11] D.R. Harrison and J. Dimeff, "A diode-quad bridge for use with capacitive transducers", Rev. Sci. Instrum., vol. 44, Oct. 1973, p. 1468.

[12] G. Blasquez, P. Pons, Ph. Menini, D. Herbst, M. Schulz, and B. Höfflinger, "Capacitive pressure mock-up without compensation circuits", Proc. Transducers'95 - Eurosensors IX, June 1995, Stockholm, Sweden, pp. 628-631.

[13] G. Blasquez, P. Pons, Ph. Menini, X. Chauffleur, Ph. Dondon and C. Zardini, "Efficiency of a BiCMOS ratiometric circuit to self-compensate for nonlinearities and thermal drifts in capacitive pressure sensors", 10th European Conference on Solid State Transducers (Eurosensors X), Leuven, Belgium, 8-11 sept. 1996, pp. 359-362.