A 60GHz, 13dBm Fully Integrated 65nm RF-CMOS Power Amplifier

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***Abstract*—A 65nm CMOS, 60GHz fully integrated power amplifier (PA) from STMicroelectronics has been designed for low cost Wireless Personal Area Network (WPAN). It has been optimized to deliver the maximum linear output power (OCP1) without using parallel amplification topology. The simulated OCP1 is equal to 8.9 dBm with a gain of 8dB. To obtain good performances and consume an ultra compact area of silicon, the PA has been matched and optimized with a mixed technique, using lumped and distributed elements. The chip size is 0.48mm*0.6mm including pads.**

I. INTRODUCTION

In the ISM band, a 7GHz unlicensed bandwidth around 60GHz is employed [1] [2] [3] [4]. Communications systems are able to ensure 1-3 GBit/s for directional links using an ASK, PSK modulation, or using an Omni-directional link with OFDM modulation with a rate higher than 500Mbps [5]. The 60GHz band is of special interest because of the attenuation (10 to 15dB/Km) due to vibrations of atmospheric oxygen molecules at this frequency. In this respect, this band is suitable for short range communications (distance < 10m), such as the indoor environment.

This application covers a big market, such as the exchange of large files between wireless devices and also the High Definition Television Video (HDTV) signal streaming in WPAN network [6]. The CMOS technology was chosen to reach these goals. Its high integration level and its low cost at high volumes are sufficient reasons to set aside the (III-V) semiconductor technology which is known as offering the best performance in gain, efficiency and output power.

In this paper, a fully integrated CMOS power amplifier is reported. It operates in 57 to 63 GHz frequency range. Initially, a brief description of the technology is provided. Then, a modeling effort is made to forecast the response of active and passive elements. This study will be concentrated distinctly in small and large signal analysis. Finally, the performances of the simulated PA will be presented and discussed.

II. CMOS TECHNOLOGY

The Power amplifier illustrated in this paper was designed with a 65nm CMOS on bulk (resistivity ρ=20mΩ.cm) from STMicroelectronics [7]. Low power (LP) transistors were chosen as active devices. They offer a cut-off frequency F_t and a maximum frequency of oscillation f_{max} around, 200 and 250GHz respectively. Compared to the general purpose (GP) transistors, LP transistors benefit from a smaller leakage current and a higher supply voltage (1.2V). They unfortunately have a lower tranconductance [4].

There are several benefits from this scaling technology. In addition to the evident reduction of silicon area, technical performances are improved. Indeed, the reduction of the gate resistance increases the gain and the power added efficiency (PAE).

III. SIMULATION METHODOLOGY

The principal reason of using this technology is the high f_{max} and its capability to operate at 60GHz. At this frequency, we have to take into account some other considerations, principally the electromagnetic effects, responsible for the degradation of performances. Therefore, small and large analyses were done to characterize the circuit, especially the post layout simulation.

A. Transistor Layout Caracterisation

The size of the transistor depends on the maximum power defined by the user. In our case, it was estimated to 10 dBm. We must not forget that the relationship between these two parameters is not linear. In fact, losses and the complexity of modeling increase with the size of the transistor. This is mainly due to capacitive and inductive effects of routed elements and silicon substrate loss. The

other important point is the electro-migration phenomenon and the ageing of components. The nanometer transistors have a low gate oxide thickness and therefore a low breakdown and supply voltage. Thus, we must have a strong current to provide the power. At high frequencies, the effective lines' width remains small and hence, insufficient to sustain a high current due to the skin depth. An architecture using a parallel amplification topology is better [8]. We need to know the maximum power delivered with a single amplification. In other terms, what is the maximum size of transistor needed to have a good trade-off between the size and the losses?

Once we have estimated the size of the transistor, it was important to optimize these three following parameters:

- Finger length (w): it directly affects not only the gate series resistance responsible for the degradation of gain, but also f_{max} (1), which is proportional to f_t:

$$f_{\max} = \frac{1}{2} f_t \sqrt{\frac{R_{ds}}{R_g}} \qquad (1)$$

$$\text{where} \quad f_t = \frac{g_m}{2\pi \cdot C_{gs}}$$

- Number of fingers per transistor (N_f): it decreases the total gate resistance which is favorable for f_{max}, but this can induce the system instability.

- Number of parallel transistors (N_c): Obviously, The system provides more power when we increase N_c. However both output impedance and optimal load (R_{opt}) of the transistors drop. The impedance transformation ratio (r) which is proportional to power losses caused by the mismatch network, defined in (3), increases.

$$r = \frac{R_L(50)}{R_{opt}} \qquad (2)$$

We have fixed the size of the driver transistors to 100µm with (N_{f1}, N_{c1}) = (100, 1) and for the output stage a size 200µm with (N_{f2}, N_{c2}) = (100, 1). The routing of the transistor is based on reducing gate-drain capacitance C_{gd} in order to minimize the S_{12}, and thus maximize f_t, f_{max}, and S_{21}. To have signals coming from all transistors' fingers, in phase, an equal distance access to the transistors' pins was respected.

B. Transistor simulation

As shown in Fig.1, an effort of modeling was necessary to carry out the small and large signal analysis.

- Small signal: to perform this analysis, a microwave approach was necessary. Accesses to gate, drain, and source were simulated with Ansoft HFSS electromagnetic simulator and represented by S-parameters blocks. The overall system illustrated in Fig. 1(a) was simulated in Cadence environment. This took into account the effects of distributed elements and the influence of the ground return path.

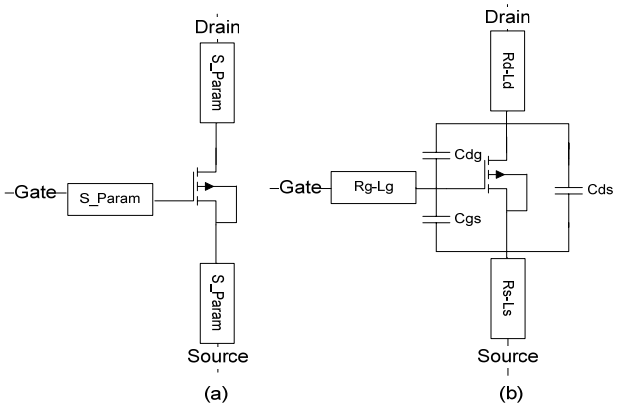

Fig. 1: Transistor modeling.

- Large signal: the S-parameters do not have significance in a non linear regime. A model with lumped elements is needed [9] and will be compared to the S-parameters mentioned above. Routing with high level metals induce inductive effects and signal delay represented by L_g, L_d, L_s. On the other hand, high currents run through the PA requiring the use of wide lines. This generates non neglected capacitive effects modeled by C_{gd}, C_{ds}, and C_{gs}.

  These reactances are important enough to change the impedance localization in Smith-chart and to cause substrate losses.

  Conductor losses are modeled by the intrinsic resistances of accesses; R_g, R_d, R_s. Fig. 1(b) shows all extracted element.

IV. CIRCUIT DESIGN

The 60GHz PA shown in Fig. 2 is a single-ended two stages common source structure. The output transistor is biased at the optimum linearity current density [10] of (70mA/200µm) whereas the driver favors the PA gain. Both two stages are supplied with 0.9V on the drain and 1V on the gates.

The first stage is biased by a tee polarization (LT, CT) outside the chip. The second transistor is biased with a current mirror.

To avoid the series resonance and to have a good quality factor around 60 GHz. We use 60pH and 72pH inductors. For capacitances values less than 45fF, MoM capacitors are used for mismatch, otherwise MIM capacitors are suitable for both decoupling and mismatch.

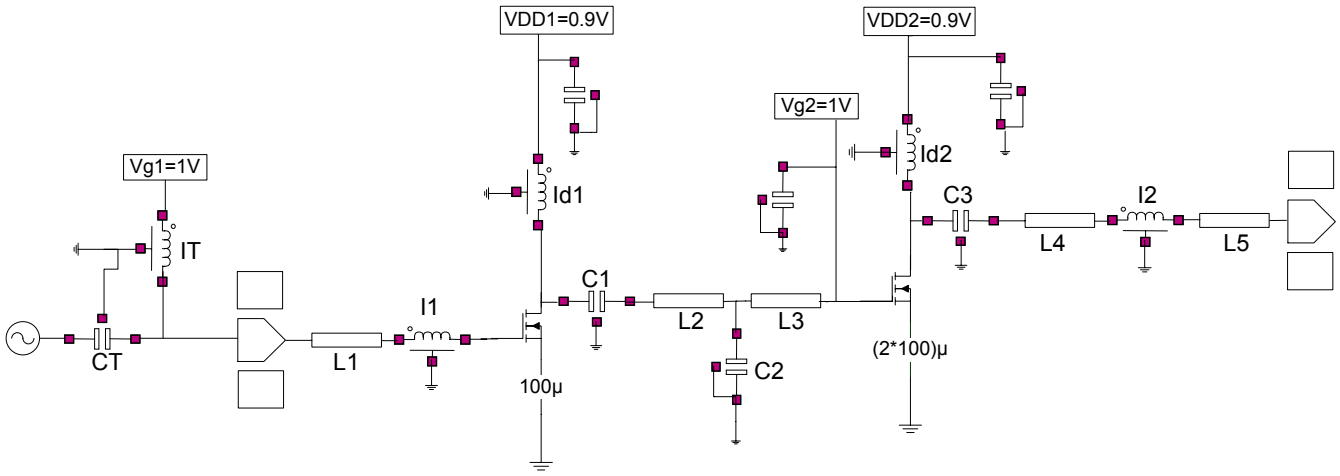

Fig.2: Schematic of the 60GHz fully integrated 65nm CMOS PA.

We have to control the characteristic impedance of the transmission lines employed for inter-elements routing. These lines measure up to λ/20 and can change the impedance. This change will be all the more significant as the characteristic impedance is high. It explains the choice of microstrip lines that are represented by *L1*, *L2*, *L3*, *L4*, and *L5*. In addition to this; Thin-film microstrips (TFMS) have the advantage of the ground plan shielding that isolates the conductive substrate. The disadvantage is that the line-width of TFMS is the unique degree of freedom, to control the characteristic impedance, once the process parameters are fixed.

Microstrip lines offer low characteristic impedance and hence consume a compact area of silicon. The chip size is 0.48*0.6mm² including pads as shown in Fig.3. The input and output matching impedance of the integrated PA are set to 50Ω.

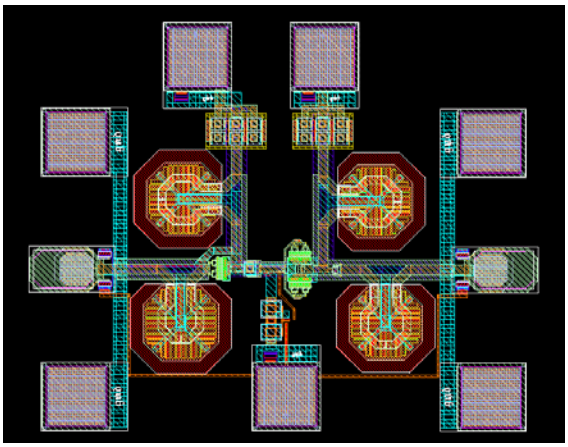

Fig.3: Layout of the integrated PA.

V. SIMULATED RESULTS

Fig.4 presents the PA scattering parameters from the EM simulation and from the equivalent developed lumped model. The PA was designed to operate from 57 to 64 GHz frequency range. The return loss (S_{11}) of the PA is less than -10dB in all the bandwidth. It reaches -22dB at 60GHz. The simulation shows a maximum small signal gain (S_{21}) of 7.6dB.

Thanks to load pull simulations the output was matched at the optimal load (R_{opt}= 10 Ω) in order to deliver a maximum power at 60GHz. Stability criteria, isolation results are reported in table [1].

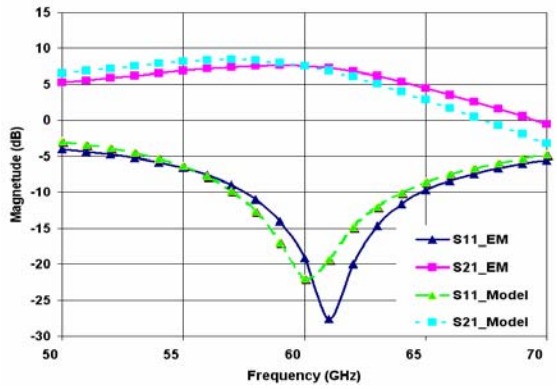

Fig.4: Simulated S parameters.

Large signal simulations, at 60GHz, were performed in Cadence environment. Fig5 shows the power transfer characteristic. Thanks to the high bias current, the PA has a good OCP1 of 8.9dBm and a saturation power of 13dB. Fig.6 shows a maximum PAE (3) of 11% in the compression region.

$$PAE = \frac{Pout - Pin}{Pdc_{stage1} + Pdc_{stage2}} \quad (3)$$

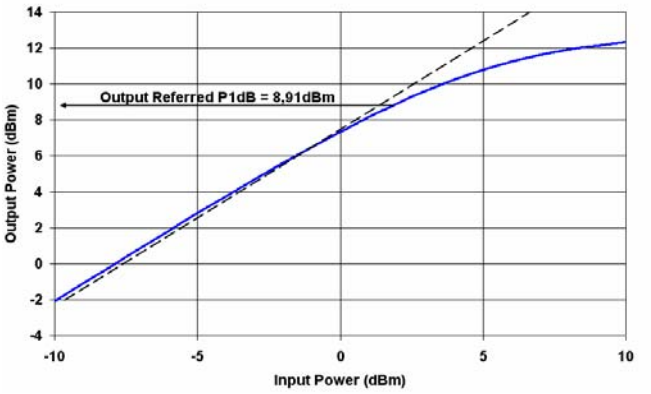

Fig.5: Output power versus available input power.

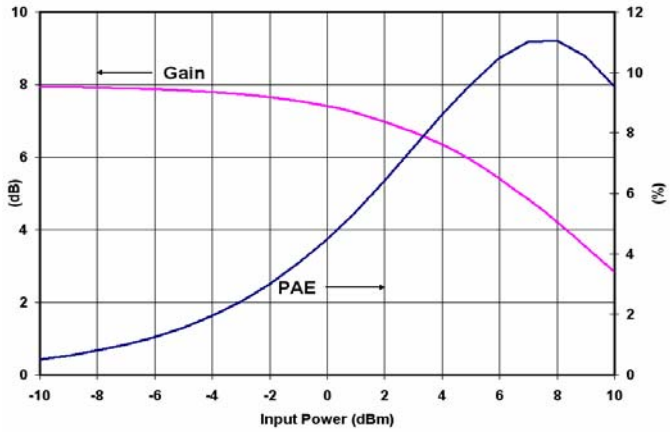

Fig. 6: Power added efficiency and amplifier gain versus input power.

references	This work (simulated)	[1]	[10]	[4]
Technology (nm)	65	90	90	130
Gain (dB)	8	9.8	5.2	12
Psat (dBm)	13	-	9.3	-
PAE (%)	11	20	7	-
OCP1 (dBm)	8.92	6.7	6.4	2
Consumption (mA@V)	72@0.9	14@1	28@1.5	36@1.6
(S_{11},S_{12}) (dB, dB)	(-22,-25)	(-13,-)	(-10,-30)	(-20,-)

Table. 1 Performance comparison of different 60GHz CMOS power amplifiers.

VI. CONCLUSION

In this paper, a 65nm CMOS, 60GHz fully integrated power amplifier was designed and sent to STMicroelectronics foundry. It is composed of two common source stages. To perform small and large signal analysis, a microwave and system approaches were necessary.

The power amplifier was optimized to ensure a linear operation for powers up to 10mW it has an OCP1 of 8.9dB and a maximum power added efficiency of 11% with a gain of 8dB. These results can be improved by adding a third stage or using parallel amplification structure.

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