Proposition of IGBT modules assembling technologies for aeronautical applications

Adrien Zéanh, Olivier Dalverny, Moussa Karama, Eric Woirgard, Stephane Azzopardi, A. Bouzourene, J. Casutt, Michel Mermet-Guyennet

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A. Zéanh[1, 2, 3, 4, *], O. Dalverny[2], M. Karama[2], E. Woirgard[3], S. Azzopardi[3], A. Bouzourene[1], J. Casutt[1], M. Mermet-Guyennet[4]

[1] *THALES Avionics Electrical Systems. 41 boulevard de la république - BP 53, 78401 Chatou, France*
[2] *ENI de Tarbes – LGP. 47, avenue d'Azereix - BP 1629, 65016 Tarbes Cedex, France*
[3] *Université Bordeaux – Laboratoire IMS. 351 cours de la Libération, 33405 Talence Cedex, France*
[4] *PEARL, Alstom Transport Tarbes. Rue du Docteur Guinier - BP4, 65600 Séméac, France*

* E-Mail: adrien.zeanh@enit.fr
*Tel.:+33(0)562534424
*Fax: +33(0)562534481

Abstract

In this paper, two IGBT (Insulated Gate Bipolar Transistor) modules assembling technologies with double side cooling capabilities and high level of integration are proposed for aeronautic applications after a state of the art and failures analysis. These technologies are compared using Design of Experiment based on non-linear Finite Element Analysis with various materials, with respect to their potential failures under thermal and power loading profiles. The configurations optimizing the lifetime and reliability level were pointed out by loading profile and failure mode. Then recommendations were done in order to choose the optimal configuration of assembly for each application.

1 Introduction

One of the current trends in the aircraft industry is the replacement of hydraulic actuators by electric actuators, in order to reduce the weights and operational costs by improving reliability. This translates into higher demand of electric power, leading to an increasing use of IGBT modules in power converters. Although such modules have been well studied and known in railway and the automotive domains, they will be subjected to stresses and operational cycles specific to the aeronautical environment. They are predicted to be used in harsh environment such as in the engine nacelle, near the actuators they drive. Consequently, this requires manufacturers to answer some questions about their lifetime and reliability issues.

Many works studied solders lifetime [1] and evaluated modules reliability by probabilistic approaches [2], but the question of an optimal design for a specific application was generally treated as state of the art.

The objective of this work is to propose specific technologies of IGBT modules, materials choice for aeronautic applications.

To tackle this problem, two sandwich assemblies with double side cooling capabilities were proposed based on a state of the art and selection criteria specific to aeronautics. Then these technologies were compared with different materials under thermal and power loading profiles. For this, Design of Experiments (DOE) method was used based on non-linear Finite Element simulation results with respect to chips junction temperatures (thermal impedances), chips and ceramic substrates brittle fracture (maximal principal stresses) and critical solders joints fatigue (Inelastic Strain Energy Densities - ISED). The most significant factors with their effects were pointed out for each response, and then recommendations were proposed.

2 State of the art of IGBT modules

For high power electronic applications, such as in power transmission, industrial drives, and locomotive traction control systems, many IGBT modules packaging approaches were proposed by industrials and research laboratories. The most common of these technologies are presented hereafter, with some of their main advantages and drawbacks.

2.1 Wire bonding connection module

This approach is the most used in IGBT module packaging.

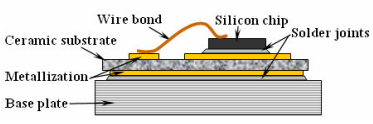

Fig. 1 Structure of a wire bonding IGBT module

The chips are brazed on a metallized substrate and base plate, the electrical connections being achieved by wire bonds. These wires bonds are main cause of failure under power cycling (**Fig. 2**).

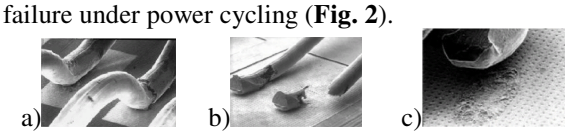

Fig. 2 Rupture (a), corrosion (b), and lift-off (c) of wire bonds [3]

Large solder joints cracks (**Fig. 3a**) are main failures mode under thermal cycling. The delamination starts at solder joint corners (**Fig. 3b**), causing thermal impedance degradation and then chips excessive heat.

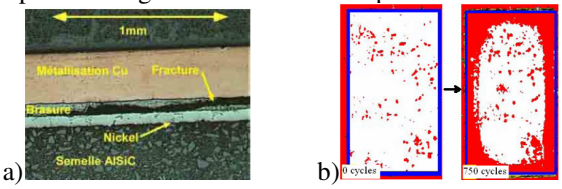

Fig. 3 Base plates solder fatigue fracture (a) [4], and delamination progression (b) [5]

The substrates and silicon chips also exhibits high risk of brittle fracture.

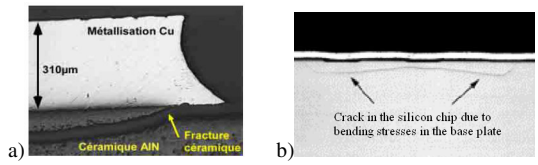

Fig. 4 Fracture of ceramic substrates (a) [4] and silicon chip (b) [3]

Other concerns with the use of this technology in aeronautical environment are about the worst electromagnetic compatibility due to high parasitic inductances, the poor thermal management and low integration level.

2.2 Other approaches

Some other approaches were used as an alternative of wire bonding assemblies. The Pressure Pack technology (**Fig. 5**) exhibits a good reliability because of the absence of solder joints, a good thermal management.

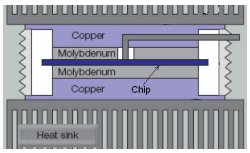

Fig. 5 Pressure Pack assembling stack

However, it necessitates special isolation and cooling systems, leading to excessive weight and cost.
Layered connection technologies were also proposed, the chips are mounted on metallized substrate with top connections obtained by alternating conducing and dielectric layers. The most known variants of this technology are Power Overlay Technology, Planar Power Polymer Packaging and Embedded Power [6, 7].

In an other approach, the chips connections were realized with solder bump arrays (Bump Array Contact Modules).
The most known variants of this approach are Dimple Array Interconnexion, Flip Chip on Flex [6, 7] and Power Bump Connection [8].
Direct Solder connection technology was also proposed [9], in order to improve the thermal impedance and reliability by balancing the module structure [10]. The chips are sandwiched by two metallized substrates with connections by direct solder.

3 Proposition of IGBT modules technology

Selection criteria were defined on the basis of thermal and thermomechanical efficiency, (chips connection possibilities, integration level, thermal management, electromagnetic compatibility, weight, volume, materials safe operating areas and toxicities, cost, processing …).
Two sandwich technologies with Power Bump (PB) (**Fig. 6**) and Direct Solder (DS) (**Fig. 7**) connection technique were retained. Both assemblies allow double side cooling with good integration levels.

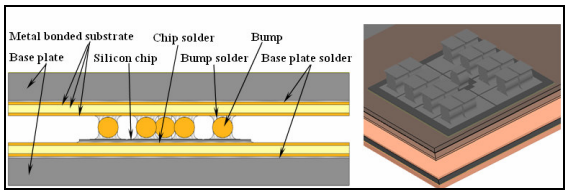

Fig. 6 PB assembly (infineon 1200V – 150A chip)

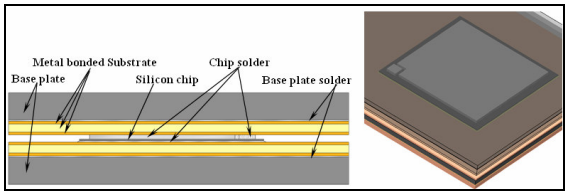

Fig. 7 DS assembly (ABB 1200V – 150A chip)

3.1 Potential failure modes

From a mechanical point of view, two main failures are susceptible to occur in these technologies: solder joints thermomechanical fatigue and brittle materials (ceramics and silicon chips) fracture. Beside these failures, the electronic components (IGBT and Diodes) failures by excessive heat due to poor thermal management were also taken into account.

3.2 Materials

The two basic assemblies will be compared with different materials chosen according to their availability, their compliance with aeronautic criteria and with the directives on the restriction of the use of certain hazardous substances in electrical and electronics equipments (RoHS, WEEE) [1, 12].

Aluminium Nitride (AlN) and Silicon Nitride (Si_3N_4) ceramic substrates were retained with copper and aluminium as metallizations. The assembling process of these packaging necessitates the use of two solders with high and low melting point. According to their good mechanical strength, melting points and wetting properties, the eutectic $Sn_{96.5}Ag_{3.5}$ were retained for all the connections, except the chips bottom (collectors or anodes) solders which are realized with $Pb_{92.5}Sn_5Ag_{2.5}$ solder. Two Metal Matrix Composites (Al-SiC(63%) and Cu-C(40) [13]) are considered as base plates.

4 Materials thermal and mechanical behaviour

Thermal and mechanical properties were gathered from bibliographical searches, for all the materials regarding their operating conditions, melting point, yield stress, ultimate tensile strength (UTS), coefficients of thermal expansion (CTE), etc.

4.1 Base plates

The thicknesses of base plates lead stresses to remain in their elastic domains. Linear elastic law was used to model their mechanical behaviour.

Table 1 Base plates properties [4, 13]

	Al-SiC(63%)	Cu-C(40)
λ (W/(K·m))	175	300// 160⊥
C (J/(kg·°C))	741	420
ρ (kg/m3)	4000	6100
CTE (10-6/K)	7.9	8.5
E (GPa)	192	75
ν	0.24	0.3

4.2 Metallizations

As suggested by L. Dupont, elastic linear law with kinematic hardening was used to model metallization mechanical behaviour [4].

Table 2 Metallizations properties [4]

	Aluminium	Copper
λ (W/(K·m))	220	398
C (J/(kg·°C))	880	380
ρ (kg/m3)	2700	8850
CTE (10-6/K)	24	17.3
E (GPa)	70.6	128
ν	0.34	0.36
Yield Stress (MPa)	17.8	98.7
Tangent modulus (MPa)	350	1000

4.3 Chip and the ceramic substrates

Regarding the observed failures at their level, and their traditional operating conditions, these materials will be modelled with elastic linear law, with brittle fracture.

Many models based on weakest link theory were proposed to describe the ceramics rupture [14]. These approaches need the material parameters to be identified, but a more simple way is to consider the Rankine's (maximal principal stress) criterion which is widely sufficient within a comparison purpose.

Table 3 Chips and ceramics properties [4]

	Silicon chip	AlN ceramic	Si_3N_4 ceramic
λ (W/(K·m))	146	190	60
C (J/(kg·°C))	750	750	800
ρ (kg/m3)	2330	3300	3290
CTE (10-6/K)	2.5	4.5	3.3
E (GPa)	130	344	310
ν	0.22	0.25	0.27
UTS (MPa)	200	400	800

4.4 Solders joints

The solders, operating at temperatures above the third of their melting points, were described using Anand's unified viscoplastic model [15].

Table 4 Solders properties [16]

	$Pb_{29.5}Sn_5Ag_{2.5}$	$Sn_{96.5}Ag_{3.5}$
λ (W/(K·m))	35	33
C (J/(kg·°C))	129	200
ρ (kg/m3)	11300	7360
CTE (10-6/K)	29	30.2
E (MPa)	24028-28·T(°C)	47200-191·T(°C)
ν	0.44	0.4
Anand's Parameters		
s_0 (MPa)	33.07	7.72
Q/R (K)	11024	14100
A (s^{-1})	105000	1630000
ξ	7	1.61
m	0.241	0.13
h_0 (MPa)	1432	58700
$\hat{s}$ (MPa)	41.63	11.99
n	0.002	0.017
a	1.3	2.09

Concerning the solders fatigue, inelastic dissipation is believed to better capture the accumulated damage. Many authors proposed ISED based models for solders joints lifetime prediction [1, 17, 18]. These models show that the number of loading cycles before solder failure is a monotonic decreasing function of the ISED dissipated per cycle. The analysis of the various assembling configurations is for this reason done hereafter according to the ISED dissipated in solder joints per loading cycle.

5 Numerical DOE

With respect to the potential failure modes and loading profiles, nine design responses were defined and considered for this analysis: thermal impedances for chips junction temperatures, maximal principal stresses for chips and ceramic substrates brittle fracture, and the inelastic strain energy densities for critical solders joints fatigue, for both loadings profiles. **Table 5** lists the responses considered, with their given labels.

Table 5 DOE responses definition

	Responses
Y1	Thermal impedance
Y2	Base plate solder ISED under thermal cycling
Y3	Chip solder ISED under thermal cycling
Y4	Substrate stress ratio (max. stress/UTS) under thermal cycling
Y5	Chip stress ratio (max. stress/UTS) under thermal cycling
Y6	Base plate solder ISED under power cycling
Y7	Chip solder ISED under power cycling
Y8	Substrate stress ratio (max. stress/UTS) under power cycling
Y9	Chip stress ratio (max. stress/UTS) under power cycling

The nine plans were built following the Yates Algorithm [19]. 3 factors listed in **Table 6**, with 2 levels each other, were considered with their first order interactions.

Table 6 DOE factors and levels

	Factors	Levels	
		-1	1
A	Connection	PB	DS
B	Metallization	Copper	Aluminium
C	Ceramic Substrate	Si_3N_4	AlN

The responses calculations were performed with the non-linear finite element models presented below.

5.1 Finite Element Modelling

Two parameterised finite element model generated using python scripts under ABAQUS™ were used.
The geometries of the elementary modules are based on standard thicknesses used in automotive and railway domains: base plates (3 mm), ceramic substrates (635 µm) metallizations (300 µm), base plate solder joints (100 µm) bumps cylinders (ϕ 1.4 mm x 1.5 mm) and direct connection solder joints (200 µm).
Three-dimensional solid elements (linear brick and tetrahedron were used for meshing the geometry, the interfaces being supposed perfect.
As suggested by A. Guédon-Gracia in [18], the assembling process and storage were simulated for the various configurations in order to compute residual stresses across the whole assemblies before cycling. The two loading profiles considered are presented below.

5.1.1 Power cycling

To model the power cycling, 250 W heat dissipation was generated in the whole volume of the IGBT chip within relative short cycles as shown in **Fig. 8**. An overall heat transfer coefficient corresponding to water cooling, at 70°C reference temperature was applied on the two external sides of the base plates as boundary conditions.

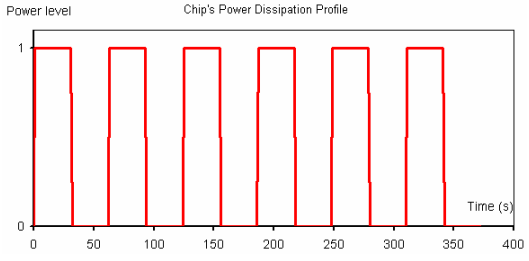

Fig. 8 Power cycling profile

5.1.2 Thermal cycling

The International Standard of Atmosphere (ISA) gives the aircraft external temperature profile during a flight cycle. To represent these loadings, an accelerated thermal profile defined according to the Military Standard Handbook 883F was considered.

As depicted in **Fig. 9**, the profile starts at 25°C, the ramp rate was 20°C/min and the dwell time at -55°C and 125°C was 20 min.

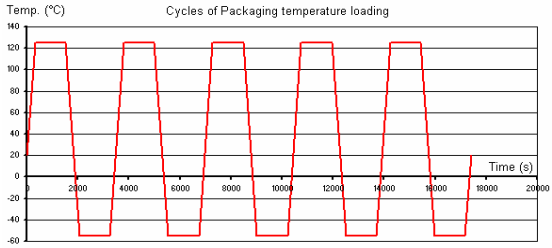

Fig. 9 Thermal cycling profile

5.2 Simulations - responses calculation

The heat flux balance across assemblies and the thermal impedances were evaluated from the power cycling simulations.
The thermal impedances (Y1) were calculated from the chip maximal temperatures, measured after the steady state is reached (**Fig. 10**).

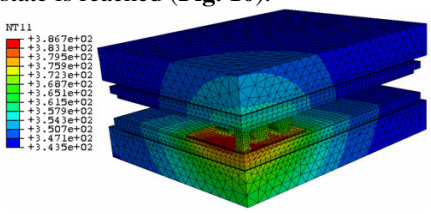

Fig. 10 Temperature distribution in solder bump assembly (K)

For all the configurations, the responses Y4, Y5, Y8 and Y9 were computed by the ratio of maximal principal stresses in the ceramic substrates (**Fig. 11**) and chips, over their mechanical strengths.
The maximal principal stress in the ceramic substrate is localized at the periphery of the bonded metallization.

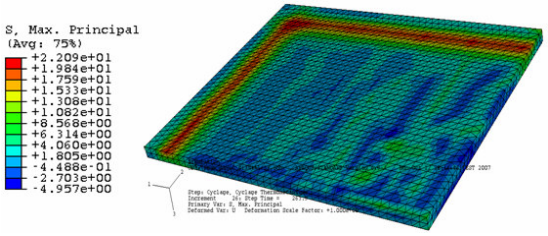

Fig. 11 Maximal principal stress distribution in ceramic substrate (MPa)

In order to evaluate Y2, Y3, Y6 and Y7, inelastic strain energy densities were computed over the solder joints (**Fig. 12**).
Many works [5] showed that the crack in large area solders propagates from solder joint corner (**Fig. 3b**). The ISED distribution in base plate solder (**Fig. 12a**) is consistent with this result, and then, for more accuracy in this analysis, Y2 and Y6 were evaluated in the corner elements instead of the whole solder joint.

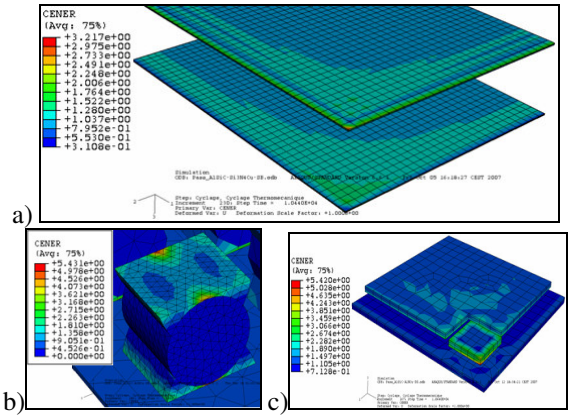

Fig. 12 ISED distribution in base plate solder (a) bumps solder (b) and direct connection solder (c) after thermal cycling (mJ/mm^3)

Regarding connection solders, the ISED were found to be maximal in the bump solder in solder bump assemblies (**Fig. 12b**) and in the gate solder for direct solder assemblies (**Fig. 12c**). Due to the relative small size of these solders, Y3 and Y7 were evaluated in their whole volume.

In order to reduce the computation time, Y2, Y3, Y6 and Y7 were evaluated within the third thermal cycle. These values could be different from these at stabilized cycles [18], but are widely sufficient for this comparative analysis.

5.3 DOE results and analysis

Basing on simulation results, the effects of the factors were evaluated for the nine responses. A Student test with a risk of 5% helped identifying the most significant factors for the nine models. All the 9 responses models built with the identified factors passed successfully a Fischer-Snedecor test with a 5% risk. **Table 7** sums these results, with the significant effects highlighted in bold.

Table 7 DOE effects and significance test results

Responses	I	A	B	C	AB	AC	BC
Y1	**0.152**	**-0.031**	**0.007**	**-0.013**	*-0.002*	*0.003*	*-0.001*
Y2	**471749**	*1927*	**-14631**	**-16313**	*-2083*	*-342*	*2487*
Y3	**319290**	*27350*	**-51018**	*-13670*	*4212*	*-278*	*-2644*
Y4	**0.138**	*0.005*	**-0.046**	**0.040**	*0.008*	*0.001*	*-0.018*
Y5	**0.621**	**-0.054**	*-0.006*	**-0.046**	**-0.047**	*-0.006*	*0.005*
Y6	**31656**	*-713*	**-29262**	*-7259*	*821*	*861*	*6989*
Y7	**15983**	**-7660**	**2198**	**-4235**	**-855**	**1775**	**-418**
Y8	**0.109**	*0.001*	**-0.029**	**0.032**	*-0.004*	*-0.001*	*-0.008*
Y9	**0.399**	*-0.035*	*-0.037*	*-0.040*	*-0.078*	*-0.034*	*-0.012*

The assembling configurations minimising the responses, and therefore maximising the modules lifetimes and reliabilities were then identified with respect to the loading.

Regarding thermal impedance and fluxes balance, it appears that the three factors are significant, without their interactions. Direct solder connection with AlN substrate and copper metallization should be preferred, but considering the intrinsic contribution of the metallization within the thermal impedance model (4.6%), aluminium could be an excellent alternative. The fluxes should be more balanced across the assemblies in order to minimize thermal stress concentrations. Regarding this characteristic, direct solders assemblies are superior with 47% of thermal flux balance through bottom and 53% through top cooling faces, compared to solder bump ones which lead to a partition of 26% - 74%. Other simulation with the two base plates showed that Cu-C is superiors than Al-SiC with about 6.3% of thermal impedance improvement.

Considering base plates solder fatigue, the only significant factors are the ceramics and metallizations. The use of AlN substrate with aluminium metallization reduces significantly the inelastic strain energy density for both loading profiles. Regarding base plate materials, Cu-C are superiors than Al-SiC in power cycling, due to their better thermal performances, but less interesting in thermal cycling because of higher coefficient of thermal expansion.

For chip connections solder fatigue, only aluminium metallizations are recommended for thermal cycling. Considering power cycling loading, direct solder connexion, AlN substrate with copper metallization should be recommended.

Regarding ceramic fracture, the stress ratio only depends on the metallization and the ceramic substrate for both loading profiles. Aluminium and Si_3N_4 ceramic minimises ceramic cracking failures risk.

For chip fracture, the recommendations are direct solder connexion, AlN substrate with aluminium metallization during thermal cycling. None of the factors considered have not significant effects on chips stresses during power cycling.

5.4 Discussion

Some contradictions appear in the above analysis when trying to take into account the recommendations for all the responses and loading profiles together. To solve these contradictions, the materials choices could be done with respect to the most critical design outputs and the most preponderant profile, knowing that IGBT modules really operate under a combination of thermal and power loadings. The significant effects presented in **Table 7** could then help doing the appropriate design.

The Direct Solder connection assembly with aluminium bonded AlN appears as the most consensual configuration.

A good solution could be the use of AlN substrate with copper bonded at the chip side and aluminium bonded at base plate side, with suitable thicknesses in order to avoid substrates fracture by bimetallic effect.

6 Conclusion

The objective of this study was to propose IGBT modules technologies based on available materials, and propose design rules to optimise the lifetime for aeronautic applications. Non-linear FEM based DOE was done with respect to the main failure modes under thermal and power cycling loading profiles.

This work showed that there was not optimal configuration of assembly (connection techniques, materials and dimensions) for all the applications, the designer should then take into account the most representative profile with the most critical design parameters to define the module. To do this, the results presented in this paper could be helpful.
Five configurations are being manufactured for thermal and power cycling tests, in order to verify the predicted thermo-mechanical performances and failures criteria.

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