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# Failure mechanism of Trench IGBT under short-circuit after turn-off

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## Abstract

Power semiconductor devices under short-circuit are submitted to high current and high voltage simultaneously that induce high electrical and thermal stresses. Several types of event leading to failure can appear under short circuit conditions in IGBT depending on the device structure, current load and voltage levels. One particular short circuit event appears once the device has turned off. After a while, the device seems to be turned on again and the current increases drastically leading to the device failure. The purpose of this study is to investigate the behaviour of Trench IGBT under such failure by the mean of 2D physically-based device simulations in order to bring some useful data for the device optimization. The physics allows to provide essential points of view on the failure description. In the proposed study, the failure does not come from latch-up but from the parasitic NPN bipolar component due to an enhancement of the conduction under thermal effect.

## 1. Introduction

One of the figures of merit of IGBT is the short-circuit capability which must be considered in the way of reliability design. During short-circuit, the electrical runaway can occur at any distinct time leading in the most cases to the device failure. Depending on the device switching conditions, several types of short-circuit can occur [1-14]. Almost no detail can be found in the literature concerning the device internal behaviour under the proposed short circuit event [6-8].

This paper deals with the investigation of the short circuit failure occurring several micro seconds after turn off. The device dynamics are investigated by the mean of 2D physically based device simulations. The analysis of internal parameters allows to point out that the failure is due to a thermal phenomenon.

## 2. Failure modes

Figure 1 allows to distinguish four failure modes under short circuit operation [11]. The failure mode A occurs at the beginning of the short circuit during the turn on. The reason can be the high applied voltage leading to early breakdown or to the latch-up phenomenon [4,5,12]. The failure mode B occurs during the on state of the device, between turn on and turn off. The main origin is the second breakdown associated to the rapid increase of the intrinsic temperature [6,7,8,13]. The failure mode C occurs during the turn off transient, and [12] explains that this kind of failure can occur due to a dynamic latch-up. The failure mode D occurs several micro seconds after turn off. Therefore, this mechanism is closely associated to the temperature [9,10,14].

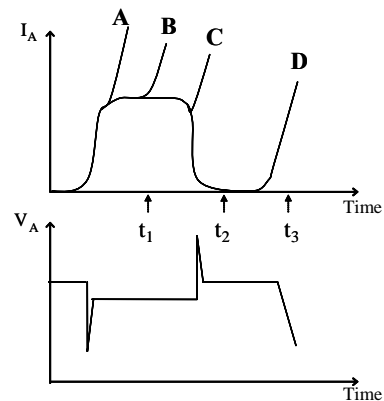


Figure 1 - Different failure modes under short circuit.

## 3. Device structure

The Trench IGBT investigated is controlled by a trench gate and it is a punch through type.

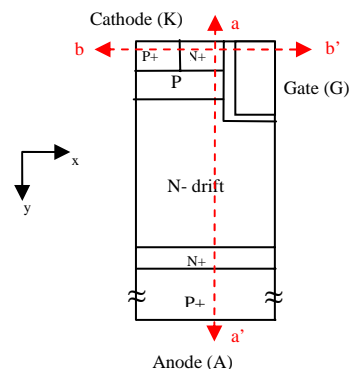


Figure 2 - The structure of the IGBT

So, the PNP emitter and the base are separated by a heavily doped N+ layer (figure 2). Lifetime is controlled by ion implantation. This device is designed for a rated current of 200A. In this condition, the maximum time during short circuit is 10 $\mu$ s. The structure width starts at 0.5 $\mu$ m to 2.5 $\mu$ m.

#### 4. Device model & simulation circuit

In order to fit the measured short circuit curves with 2D simulation results, it is necessary to consider electrical elements attached to the physical structure (figure 3). These elements are associated to the packaging and the measurement test set: parasitic inductances ( $L_A$ ,  $L_K$ ) and parasitic collector resistance  $R_A$ . A ballast resistance  $R_K$  is also added to adjust the short circuit current level. The physical simulation is performed with GENESIS ISE-TCAD software [15].

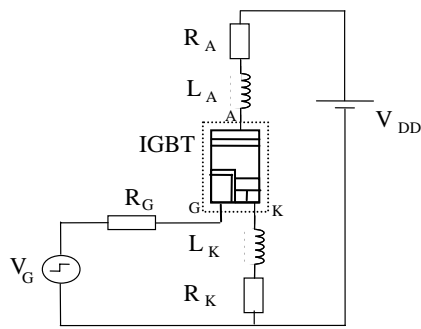


Figure 3 - Simulation circuit

A previous study, performed on static curves allowed to fit static characteristics (figure 4).

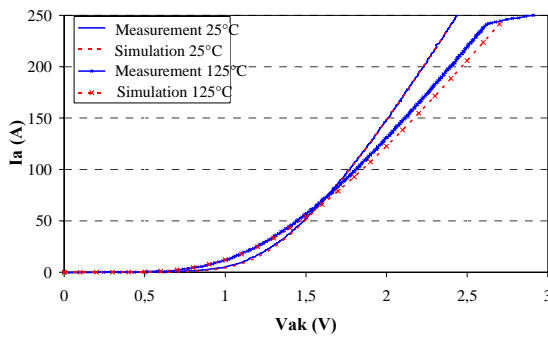


Figure 4 - Simulation and experiment of the static characteristic  $I_K=f(V_{AK})$  at 25°C and 125°C

Then, in the simulator software, and by taking into account main physical mechanisms like mobility degradation, recombination and impact ionization, always with temperature computation, it is possible to have a good matching for the short-circuit event as shown in figure 5.

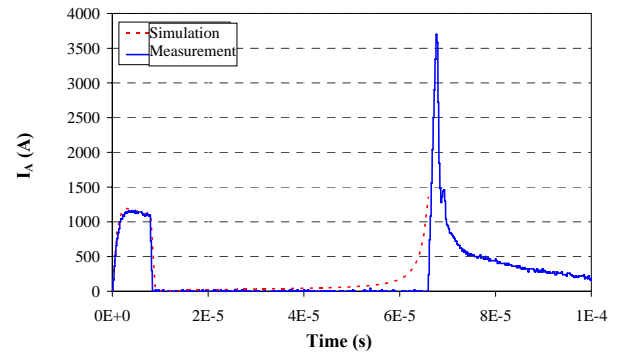


Figure 5 - Simulation and experiment of the dynamic characteristic of short circuit after turn off.

The evolutions of the main physical parameters in the 2D structure are observed for three distinct instants pointed out in figure 1. Note that  $t_1$  is located in the middle of the turn on time,  $t_2$  is after the turn off and  $t_3$  is just before the failure. Furthermore, two vertical cut lines a-a' (vertical at 1.5 $\mu$ m) and b-b' (horizontal at 0.5 $\mu$ m) along the structure (figure 2) are done to observe the device behaviour under 1D.

#### 5. Results and discussion

The failure analysis of the Trench IGBT is initiated under  $V_{DD}=650V$  and  $I_{csat}=1200A$  short circuit conditions.

At time  $t_1$  which corresponds to the time for a maximum current conduction under a high collector voltage, figure 6(a) depicts that the main current (electron current) runs through the channel of the MOSFET. A part of this current (hole current) is also running through the P+ / Pbase region to reach directly the cathode contact of the IGBT (figure 6(b)).

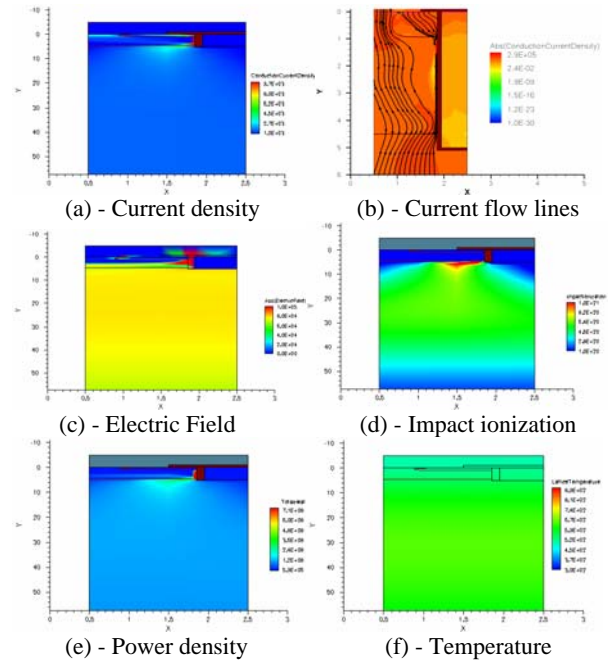


Figure 6 - 2D physical distribution of some parameters at  $t_1$ .

At that time, since the collector voltage is very high, the electric field within the structure depicted in figure 6(c) is maximum in the N-drift region near the

Pbase / N-drift junction. At this location, the highest value of the impact generation rate can also be observed as indicated in figure 6(d). The power density which is related to the dot product of the electric field and the current density is maximum at the Pbase / N-drift junction close to the channel where the current density is also high (figure 6(e)). As a consequence, the mapping of the temperature indicates that in this area the temperature reaches a maximum value (figure 6(f)).

At time  $t_2$ , the gate voltage has been reduced to zero and the channel of the MOSFET has been cut off. The device turned off and the whole current has been removed from the structure (figure 7(a)). However, figure 7(b) indicates that a hole current is still flowing within the device corresponding to the current tail. The electric field stays high along the reversed biased Pbase / N-drift junction due to the high voltage continuously applied on the device (figure 7(c)). At the vicinity of this junction, the impact ionization shown in figure 7(d) is spreading a little bit and figure 7(e) illustrates that the power density is almost zero (very low current). At this instant the temperature mapping (figure 7(f)) reaches a high value (but not the highest one during the short-circuit). From that graph we can not conclude that the impact ionization is responsible for the device failure since the generated current is not so large and the observation of 1D graph along the cut line xx' shown hereafter will allow to have a better understanding of the failure.

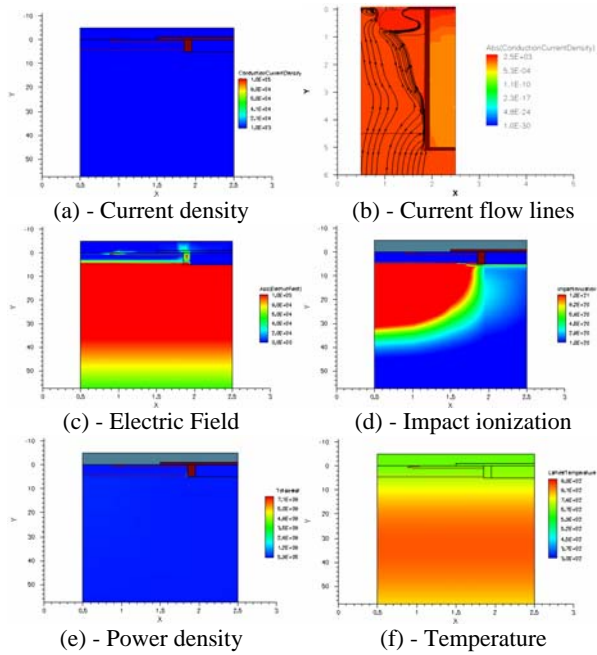


Figure 7 - 2D physical distribution of some parameters at  $t_2$ .

At time  $t_3$ , without any control on the gate electrode, the current starts running again inside the structure as depicted in figure 8(a). However, we can observe that the current runs not only close to the channel area but also just under the P+ / Pbase region through the Pbase / N-drift junction (figure 8(b)). The electric field is still high but the value starts decreasing with the decrease of the applied voltage and the increase of the current as shown in figure 8(c). The

impact generation rate depicted in figure 8(d) indicates that the generated carriers increase but the generated current still remains very low compared to the total current. The increase of the total current in the device induces an increase of the power density as it was the case during the turn-on phase at time  $t_1$  (figure 8(e)). This final stage corresponds to the device failure since the current can not be controlled: no pulse has been applied on the gate electrode. In that case, the temperature mapping illustrated in figure 8(f) shows an increase of the temperature within the device with a highest value close to 900K.

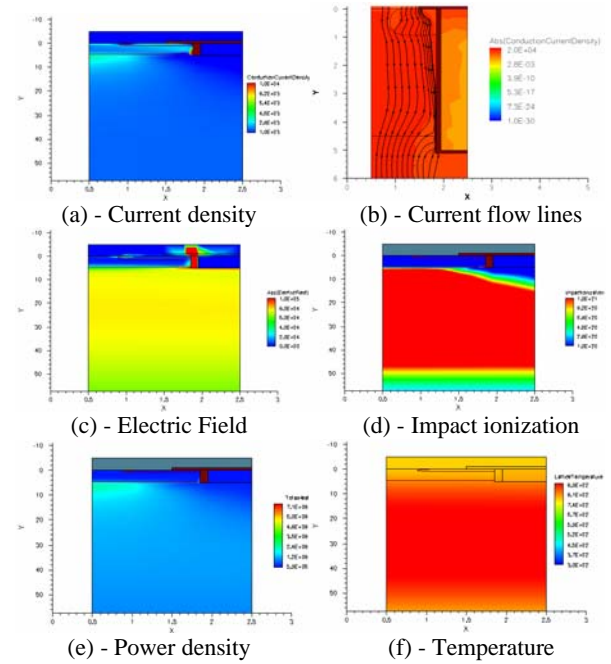


Figure 8 - 2D physical distribution of some parameters at  $t_3$ .

In order to have a better understanding on the failure mechanism, we propose to analyze 1D graphs taken along a-a' and b-b' cut lines from figure 2. First of all, when we consider the temperature mapping along line a-a', as for the 2D representation, we can observe that the maximum temperature (figure 9) is located at the vicinity of the maximum electric field during turn on. So, this maximum is located in the Pbase region close to the collector-base junction of the PNP component. At time  $t_3$ , the simulated value is a little bit more than 900K.

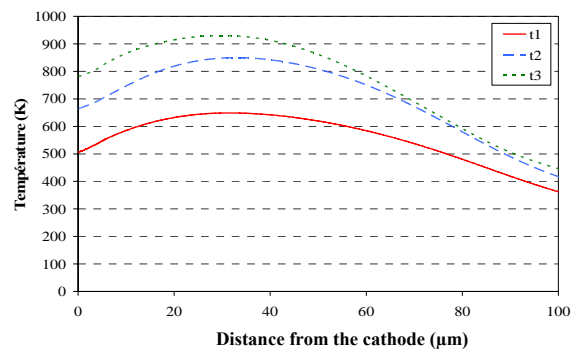


Figure 9 - 1D temperature distribution during the whole short circuit event along a-a' cut line

During turn-on ( $t_1$ ), the maximum electric field is located in the drift region due to the current flow. During turn off ( $t_2$ ), this maximum is located at the collector-base junction of the PNP component (Pbase / N-drift region) as shown in figure 10. The voltage is the highest at that time: the decrease of the current induces an increase in the voltage applied to the device due to stray inductance.

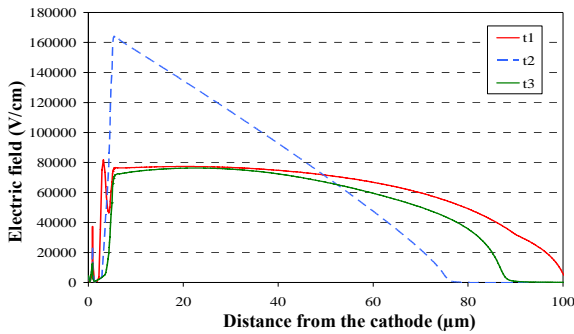


Figure 10 - 1D Electric field distribution during the whole short circuit event along a-a' cut line

Whereas it seems that the impact generation rate increases with time during turn-on, the carrier generation issued from impact ionization reaches a maximum value at time  $t_1$  along the cut line a-a' as depicted in figure 11. This first information leads us to think that the failure which will occur at time  $t_3$  is not induced by a breakdown phenomenon since the impact ionization rate is not predominant before the device failure.

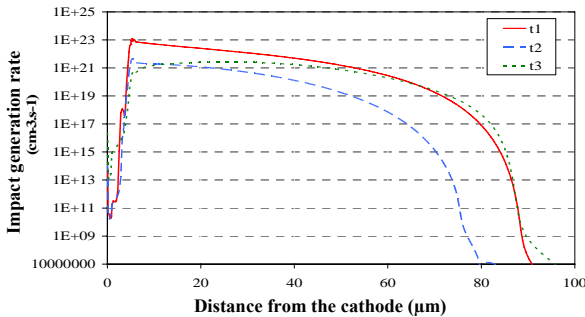


Figure 11 - 1D impact generation rate distribution during the whole short circuit event along a-a' cut line

The depth of the metallurgic junction (N+ / Pbase junction) is estimated at 1.5  $\mu\text{m}$ . Under zero current, the electrostatic potential plotted versus temperature in figure 12 indicates a value around -0.9V at 300K (negative normalization).

This can be considered as a reference. Furthermore, figure 13 shows a kind of “quasi-linear” decrease of this potential with the temperature when a current runs through the device. During transient turn-on, the voltage is about -0.7V (figure 13). During turn-off, its value decreases instead of increasing due to the reduction of the current. But the value simulated at  $t_3$  is lower whereas the current rises suddenly. This indicates that the temperature increase at the vicinity of the cathode may be responsible for the device failure.

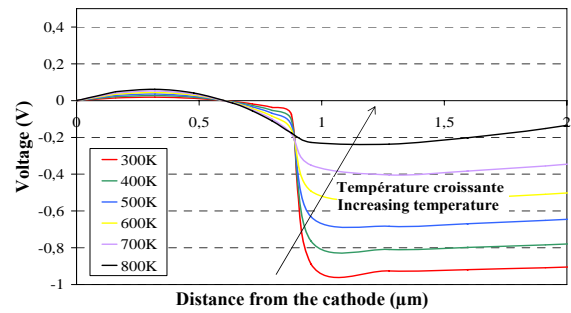


Figure 12 - 1D drop voltage evolution with temperature variation at the Pbase / N+ junction for zero current along a-a' cut line

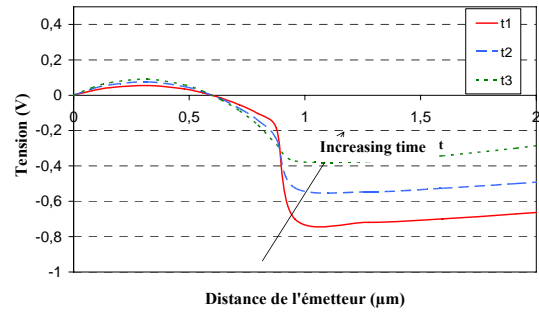


Figure 13 - 1D drop voltage evolution with temperature variation at the Pbase / N+ junction during the whole short circuit event along a-a' cut line

An analysis of the voltage drop along the P+ / N+ junction (base-emitter of the NPN parasitic bipolar component junction) indicates that the latch-up did not occur as highlighted in figure 14 (voltage drop lower than 0.7V) even if the NPN component lightly conducts. This information was also pointed out by figure 7(b) showing a current near the channel area.

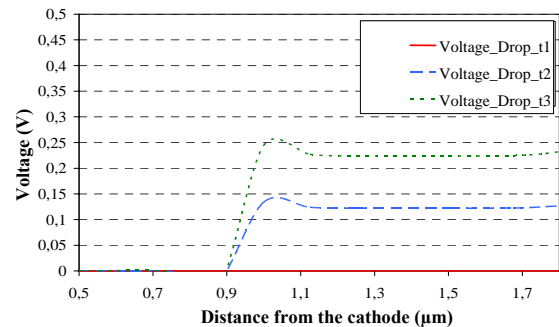


Figure 14 - Normalized 1D drop voltage evolution at the P+ / N+ junction during the whole short circuit event

The carriers concentration evolution is plotted in figure 15. When the device is turned-on, the drift region is under high level injection (carriers density upper than the total doping). Close to the Pbase region, the electrons focus mainly in the channel and the holes in the Pbase region. When the device has turned off, the current in the whole device is cut off and the drift region is under low level injection (carriers density lower than the background doping). However, in the Pbase region, the temperature increases leading to an increase of the carrier concentration (the intrinsic concentration increases with the temperature rise). Just before failure, the current increases drastically leading

to the N-drift region in high level injection again. Also, as it has been noticed before, the electrons do not focus only close to the channel but also in the Pbase region as well as the holes. Therefore the electrons and holes concentration are relatively high in the Pbase region.

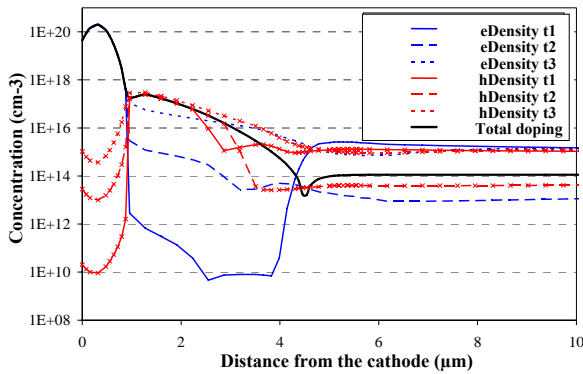


Figure 15 - Carriers concentration evolution during the whole short circuit event along a-a' cut line

As an additional feature, this is also highlighted by figure 16 illustrating the current density at the cathode contact which indicates that the whole current does not only flow through the NPN component but also in the P+ cathode contact.

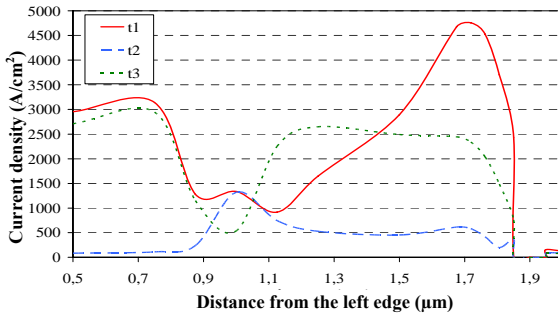


Figure 16 - 1D current density evolution during the whole short circuit event along b-b' cut line

In the channel region, it is possible to visualize the 2D physical distributions of electron and hole current density at  $t_1$ ,  $t_2$  and  $t_3$  (figure 17), which allows to observe an increase of the electron density in the Pbase region.

The electron and the hole contributions to the total current are also illustrated in figure 18 which clearly shows that whereas the saturation current was mainly composed by electron current during short circuit turn-on, just before failure the total current is composed in the same ratio of hole and electron currents.

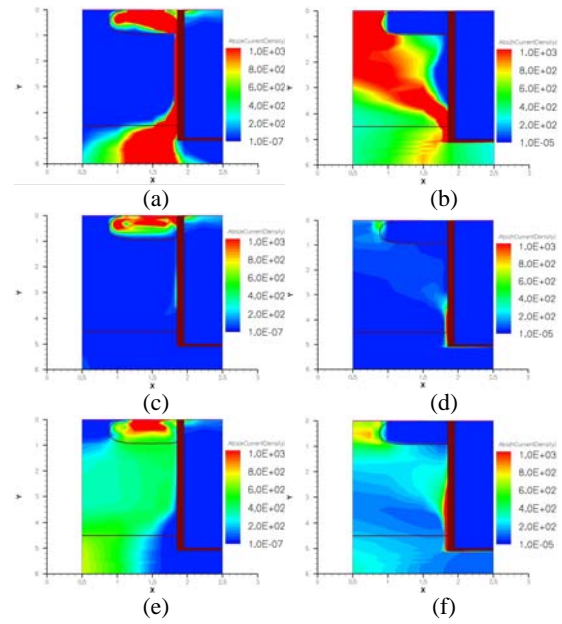


Figure 17 - Electron (a,c,e) and hole (b,d,f) current density at  $t_1$ ,  $t_2$  and  $t_3$  respectively

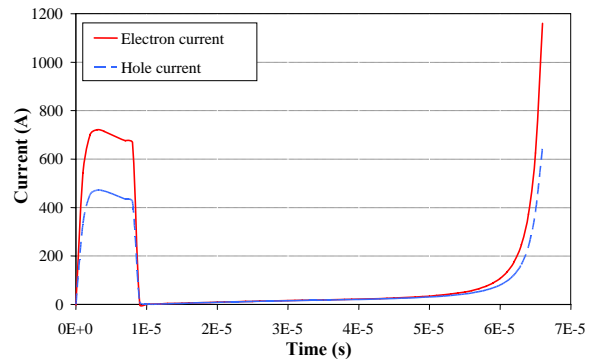


Figure 18 - Saturation current composition (part of hole and electron current)

Figure 19 is a key figure since it is possible to observe that the diffusion of this temperature between  $t_1$  and  $t_3$  (at times  $t_{21}$ ,  $t_{22}$  and  $t_{23}$  taken just after time  $t_2$ ,  $t_{23} > t_{22} > t_{21}$ ) leads to an increase of the cathode temperature after turn off. The inversion in the highest temperature value located first in the drift region and after in the Pbase area will accelerate the device failure by the activation of Pbase / N+ junction.

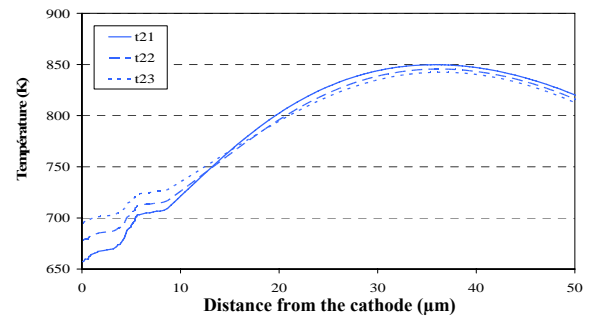


Figure 19 - 1D temperature evolution just after turn-off along a-a' cut line indicating an increase of the cathode temperature

## 6. Conclusion

The failure mechanism under short circuit just after turn-off has been investigated by considering the simulation of a finite elements 2D physically based Trench IGBT model. The information collected at various simulation times allow to focus on the device behaviour by considering the device physics.

It has been highlighted that the decrease of the cathode junction potential induced by increase of the cathode temperature indicates that an assisted thermal phenomenon occurs inducing the conduction enhancement of the parasitic NPN component. This leads to the so identified mode D failure few micro seconds after turn off under short-circuit.

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