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A step by step methodology to analyze the IGBT failure mechanisms under short circuit and turn-off inductive conditions using 2D physically based device simulation

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Abstract

A systematic methodology is developed in order to clarify the punch through Trench Insulated Gate Bipolar Transistor (T-IGBT) failure mechanisms which can occur under extreme operating conditions such as short circuit and clamped inductive switching. By considering a 2D dimensional physically based device simulation, and by analyzing some T-IGBT physical parameters, it is possible to identify if the failure mechanism is due to a breakdown, a latchup or a thermal runaway phenomenon.

1. Introduction

During high electrical and thermal stresses applied in many power module applications, different failures can occur, for example, under short circuit [1-7] and inductive switching conditions [8-10]. Those failures are often illustrated as drastic increasing of the total current in the power components, leading in many cases to the destruction of the device. It is not obvious to know which phenomenon occurred in the component and causes the failure. This is the reason why, it is necessary to investigate the internal behaviour of the component under such failure conditions, and a 2D or 3D physically based simulation is the best way to investigate the failure origins. In this paper, a systematic methodology is proposed to identify a destructive failure cause which can occur on a punch through trench gate IGBT. This is possible by simulating and analyzing some physical parameters.

2. Analysed device structure

The Trench IGBT investigated is a 1200V, 150A IGBT. The component is controlled by a trench gate and it is a punch through type. So, the PNP emitter and the base are separated by a heavily doped N+ layer (figure 1). Lifetime is controlled by ion implantation.

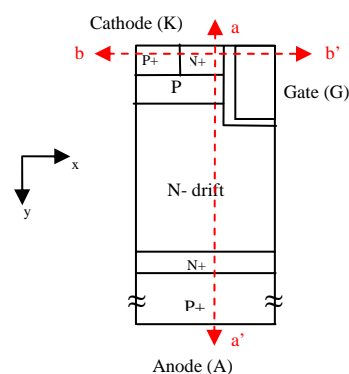


Fig. 1. The structure of the Trench IGBT

The simulation is performed with GENESISe ISE-TCAD software [11].

3. Methodology description

In order to identify the correct failure mechanism, it is necessary to simulate in a normal operating condition, the hole (I_p) and the electron (I_n) currents flows running through the cathode contacts P^+ and N^+ . The determination of these currents during the failure event will allow to clarify the failure origin. For each mode encountered, the failure origin identification is made thanks to the analysis of the related physical parameters. In order to confirm if the impact ionization phenomenon appends in the N drift region, we compute the integral of this physical value through the whole device area and then we compare the generated current to the global current.

As regarding the conduction enhancement of the base-emitter junction of the NPN parasitic bipolar transistor (N^+ / P base junction), the junction potential measurement compared to the extrapolated initial values will allow to confirm if a latchup phenomenon occurs or not. For $V_{be} > 0.7$, this junction is forward biased and a failure can occur due to the latchup phenomenon. In this case, a hole current I_p due to the latchup is generated and the ratio I_p/I_{P^+} is very high, whereas this ratio is about unity in normal operation.

Another cause of failure can be identified in the case of no latchup and no impact ionization, this phenomenon is the thermal runaway or second breakdown and is directly related to the temperature evolution in the IGBT.

Through the previous physical mechanism, we propose a systematic methodology to clarify the failure mechanism origin. This methodology is summed up in figure 2.

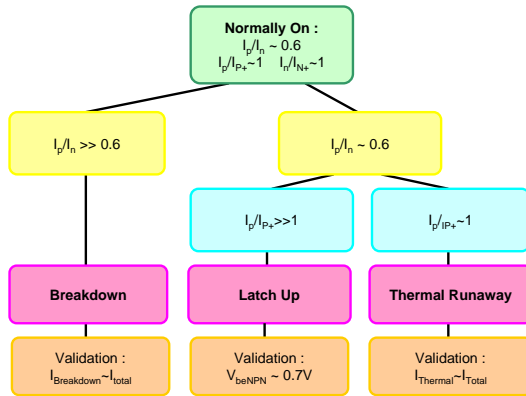


Fig. 2. Methodology chart

In a normal operation mode, the ratio I_p/I_n is about 0.6 and is defined by the structure irradiation for control the carriers lifetime. If this ratio increases during failure, this means that the impact ionization is mainly responsible for the device failure. In other case, it is necessary to evaluate the base-emitter junction voltage difference V_{be} of the NPN parasitic bipolar transistor (N^+ / P base junction), If $V_{be} > 0.7$, it means that there is a latch up phenomenon inducing a failure,

if $V_{be} < 0.7$ and I_p/I_n is always about 0.6, a one-dimensional temperature analysis can reveal that the failure is related to the high increase of temperature and we can conclude of a thermal runaway phenomenon responsible of the failure.

4. Application examples

Three different failure configurations are presented as examples of the methodology application to reveal the different failure origins. The first and the second one are failures occurring respectively during turn-on and few microseconds after turn-off [6] under short circuit conditions whereas the third example is a failure occurring several microseconds after inductive load turn-off [8].

4.1 Failure mechanism during turn-on under short circuit conditions : “mode A”

The mode A failure analysis of the trench IGBT is initiated under $V_{DD} = 1200V$ and $I_{csat} = 280A$ (abnormal case), [6] short circuit conditions at the temperature $T = 423K$. Figure 3 presents the simulation of the dynamic characteristic of short circuit. Three times t_1 , t_2 and t_3 are chosen to extract some internal physical parameters to analyze the structure of the component focusing on the active region. The time t_1 corresponds to the time of the beginning of the turn-on, at time t_2 , the current is about the saturation current and it corresponds to the beginning of the failure. Finally, at time t_3 , the current increases drastically and the component is under failure.

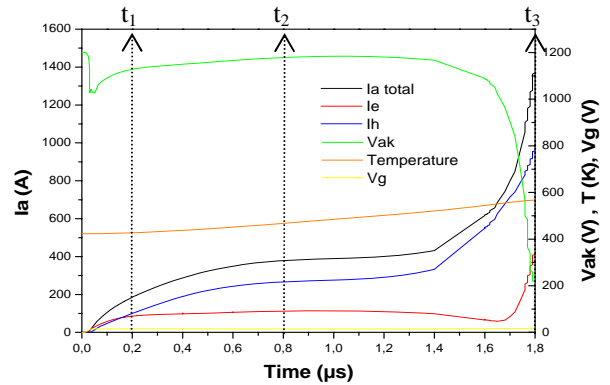


Fig. 3. Global waveforms for failure “mode A”

In the whole transient, the current is flowing within the IGBT as depicted in figure 3. The electron current runs through the channel of the MOSFET. The hole current is running through the P^+ / P base junction to reach directly the cathode contact of the IGBT. Note that the hole current seems to be higher than the electron current. When we consider the ratio between the hole current and the electron current (depicted in figure 4) during the whole transient, we notice that this ratio increases drastically as soon as the device has been turned-on. Figure 3 confirms this preliminary result. We can conclude from the methodology that there is an impact ionization mechanism leading to breakdown. We can now have a look on 1D and 2D device analysis.

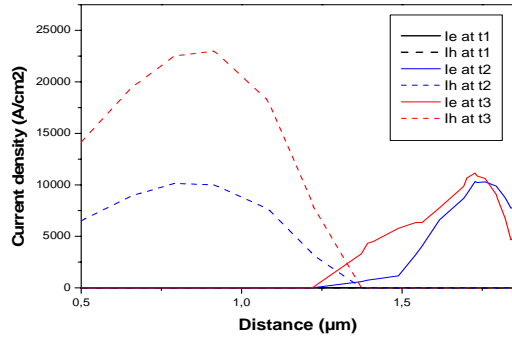


Fig.4. 1D current density evolution along b-b' cut line

Considering that a high collector voltage is applied (1200V), the electric field within the structure is maximum in the N drift region near the Pbase / N drift junction. At this location, the value of the electric field is strong enough to generate carrier by impact ionization as indicated in figure 5 showing a high impact ionization generation rate.

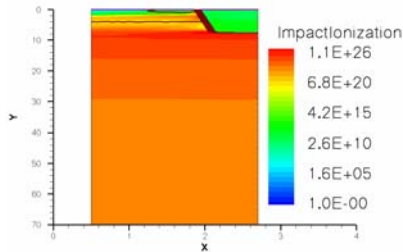


Fig.5. Impact ionization distribution at t_3

The generated current represents 1% of the total current at t_1 , 32.8% at t_2 and 28% at t_3 . This allows to conclude that impact ionization is responsible for the short circuit failure mode A. Furthermore, figure 4 confirms that the latchup did not occur since the hole current still concentrates in the P+ region. This observation is confirmed by figure 6 illustrating that the voltage applied to the base-emitter junction of the parasitic NPN bipolar component is lower than 0.7V.

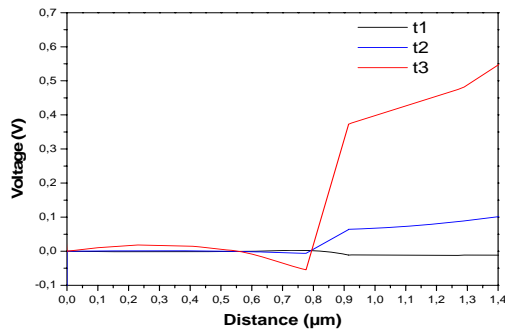


Fig.6. Normalized voltage applied to the base-emitter junction of the parasitic NPN bipolar component along a-a' cut line

Figure 7 illustrates that the maximum temperature reaches at cathode contact at t_2 is too low to be responsible for a thermal runaway failure. A consecutive elevation of temperature to breakdown phenomena is illustrated at t_3 .

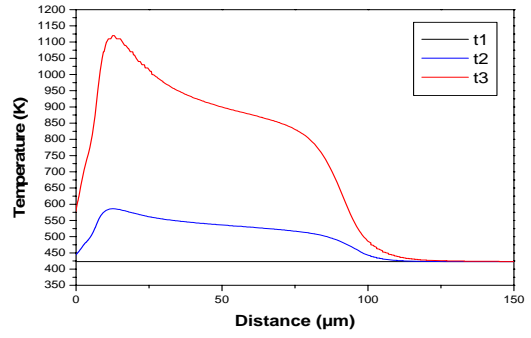


Fig. 7. 1D temperature distribution along a-a' cut line

4.2 Failure mechanism during turn-off under short circuit conditions : "mode D"

The failure "mode D" has been investigated for $V_{DD}=250V$ and $I_{csat}=300A$. The time t_1 is taken during on-state, the time t_2 is taken after the turn off and corresponds to the beginning of the failure. Finally, at the time t_3 , the current starts increasing drastically and the component turns under failure (figure 8).

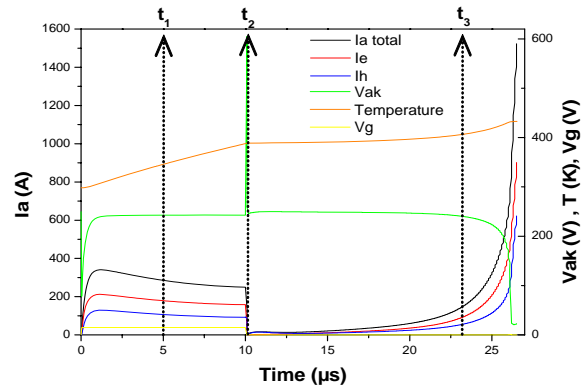


Fig. 8. Global waveforms for mode D

At time t_1 which corresponds to the time for a maximum current conduction under a high collector voltage, the main current (electron current) runs through the channel of the MOSFET. The hole current is running through the P+ region to reach directly the cathode contact of the IGBT. At time t_2 , the gate voltage has been reduced to zero and the channel of the MOSFET has been cut off. The device turned off and the whole current has been removed from the structure.

At time t_3 , without any control on the gate electrode, the current starts running again inside the structure as depicted in figure 8. However, we can observe that the current runs not only close to the channel area but also just under the P+ / Pbase region through the Pbase / N drift junction.

In that case, the temperature mapping illustrated in figure 9 shows an increase of the temperature within the device with the highest value close to 860K.

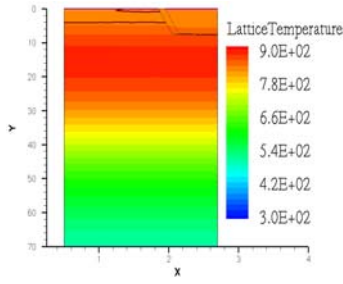


Fig.9. Temperature distribution at t_3

When we consider the ratio between the hole current and the electron current (depicted in figure 8) during the whole transient, we notice that this ratio keeps a constant value (about 0.6). Figure 10 confirms this preliminary result. We can conclude from the methodology that there is no impact ionization mechanism leading to breakdown. We can have an overview on 1D device analysis.

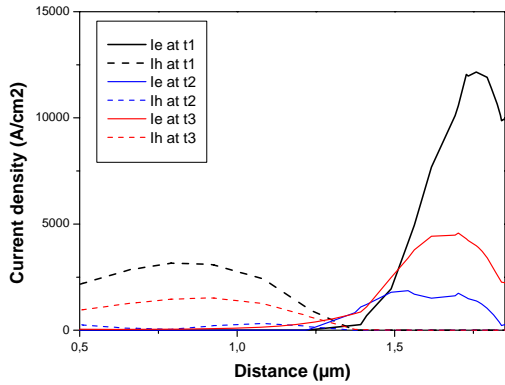


Fig.10. 1D current density evolution along b-b' cut line

Furthermore, figure 10 indicates that the latchup did not occur since the hole current still concentrates in the P+ region. This observation is confirmed by figure 11 illustrating that the voltage applied to the base-emitter junction of the parasitic NPN bipolar component is lower than 0.7V.

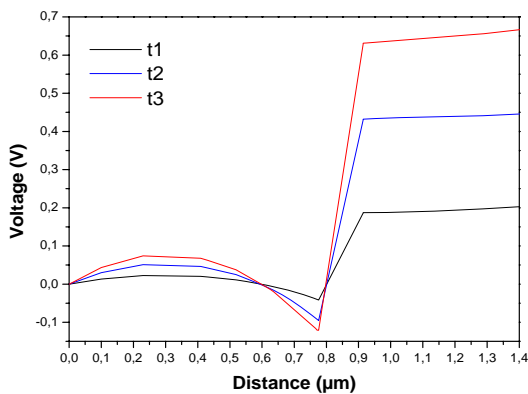


Fig.11. Normalized voltage applied to the base-emitter junction of the parasitic NPN bipolar component along a-a' cut line

Finally, when we observe the figure 8 and as confirmed by figure 12, the failure mechanism is linked to a thermal runaway.

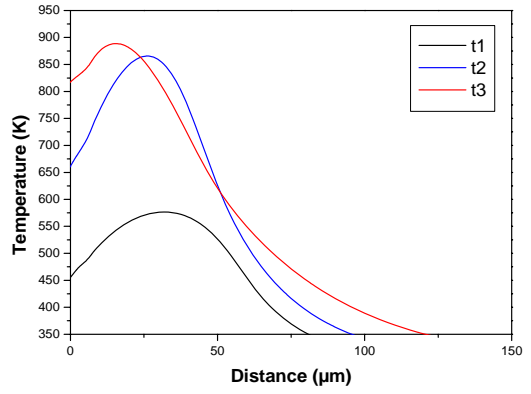


Fig. 12. 1D temperature distribution along a-a' cut line

Figure 13 is a key figure since it is possible to observe the inversion in the highest temperature value located first in the drift region and after in the Pbase area will accelerate the device failure by the conduction enhancement of the Pbase / N+ junction.

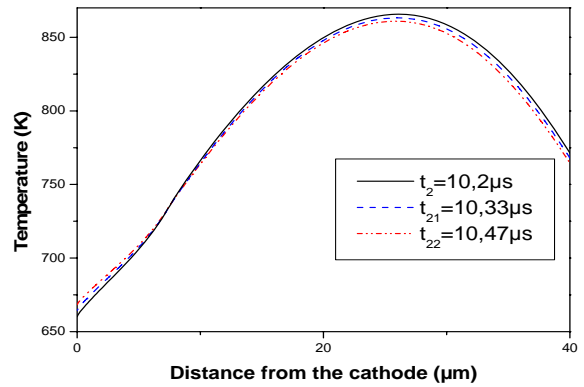


Figure 13. 1D temperature evolution just after turn-off along a-a' cut line

4.3 Failure analysis during inductive load turn-off

In this case, the trench IGBT is turned off under the conditions $V_{DD}=820V$, $I_{cmax}=400A$ gate resistance $R_g=1\Omega$ at the temperature $T=298K$.

Figure 14 gives a general overview of the simulated current, voltage and temperature waveforms at the cathode from internal side. It is evident that a failure occurs after t_3 , without any control on the gate, the current increases suddenly and drastically.

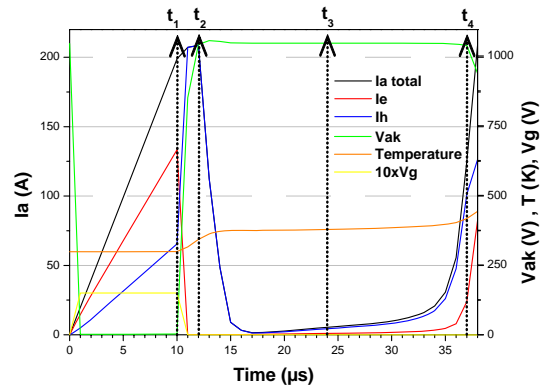


Fig.14. Global waveforms for inductive load switching

At time t_1 , the electron current runs through the channel of the MOSFET and the hole current under the influence of the electron flux flows laterally through the P+ / Pbase region to reach directly the cathode contact of the IGBT.

Concerning the ratio between the hole and the electron currents (depicted in figure 14) during the transient, we notice that this ratio of 0.6 is respected at t_1 , but it increases at t_2 . At this time the generated current due to impact generation is about 55% and is due to the high electrical stress during the switching. Figure 15 confirms this preliminary result. We can conclude from the methodology that there is an impact ionization mechanism but it is not leading to a direct failure. A 1D analysis of the device structure will provide useful information.

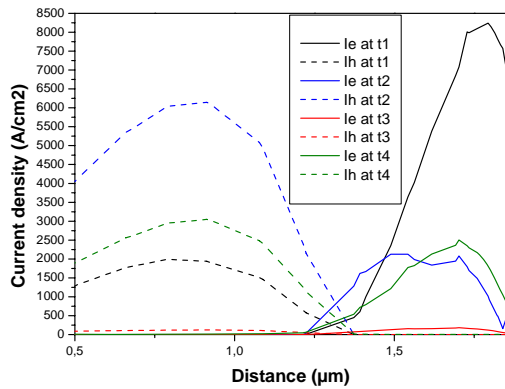


Fig.15. 1D current density evolution along b-b' cut line

The maximum value of the current density and electric field lead to the maximum value of the power density. In that case, the self heating generated within the structure leads to a temperature mapping showing an increase of the temperature within the device with a highest value close to 830K. This peak of temperature located in the Ndrift region at the vicinity of the Pbase / Ndrift junction (figure 16) is diffused into to the structure after t_2 .

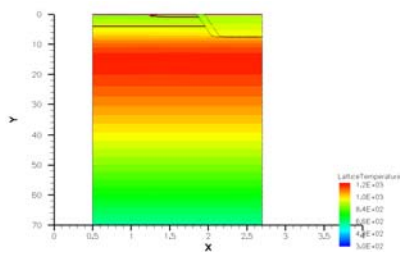


Fig. 16. Temperature distribution at 32µs

This is highlighted in figure 17 and illustrated by the temperature waveform at t_3 . When we observe the figure 17, it is possible to say that the failure mechanism is linked to a thermal runaway initiated by a strong impact ionization. A more complete analysis is given in detail in [8].

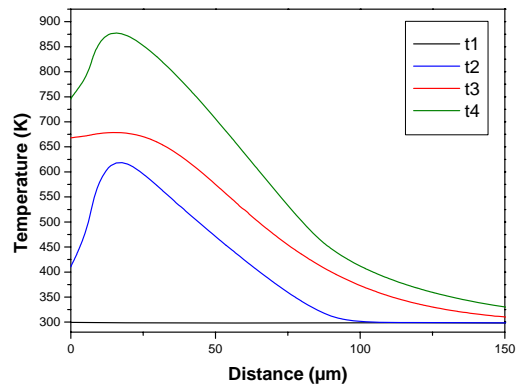


Fig. 17. 1D temperature distribution along a-a' cut line

Furthermore, figure 15 indicates that the latchup did not occur since the hole current still concentrates in the P+ region. This observation is confirmed by figure 18 illustrating that the voltage drop applied to the base-emitter junction of the parasitic NPN bipolar component is lower than 0.7V.

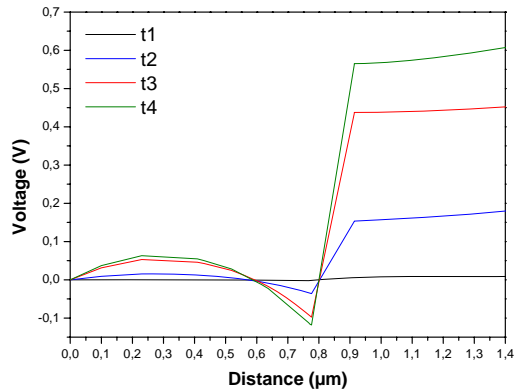


Fig. 18. Normalized voltage applied to the base-emitter junction of the parasitic NPN bipolar component along a-a' cut line

5. Conclusion

In this paper, a systematic methodology was developed in order to determine the failure mechanisms which can occur on a power component like IGBT and under extreme operating conditions. It was highlighted that the two main mechanisms (breakdown and thermal runaway) leading to a destructive failure can be pointed out by a specific simulation analysis.

The breakdown mechanism can be revealed by the study of the evolution during a transient of the ratio I_p/I_n which is fixed by the structure irradiation for control the carriers lifetime. If this ratio increases during failure, this means that the impact ionization is mainly responsible of the device failure. For the latchup mechanism, it is necessary to evaluate the base-emitter junction voltage difference V_{be} of the NPN parasitic bipolar transistor (N+ / Pbase junction). If $V_{be} > 0.7$, it means that there is a latch up phenomenon inducing a failure. Finally an appropriate temperature distribution analysis can reveal that the failure is related to the high increase and diffusion of temperature within the component and we can

conclude of a thermal runaway phenomenon is responsible for the failure. Three different switching configurations were useful to validate the proposed approach.

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