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Trench IGBT failure mechanisms evolution with temperature and gate resistance under various short-circuit conditions

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Abstract

Two extreme configurations under short circuit conditions leading to the punch through Trench IGBT failure under the effect of the temperature and the gate resistance have been studied. By analyzing internal physical parameters, it was highlighted that the elevation of the temperature causes an acceleration of the failure which is due to a thermal runaway phenomenon, whereas the influence of the gate resistance on the failure evolution is minimal.

1. Introduction

The short circuit capability is one of the figures of merit which defines the robustness of the power semiconductor components, especially the IGBT. Depending on the thermal and electrical conditions, during short circuit event, different types of failure can occur [1-8]. In the literature, some studies describe the various short circuit failure modes, but almost do not give internal device behaviour analysis. In fact, an internal 2D investigation seems to be necessary to have a good understanding of the failure mechanisms. This paper deals with the investigation of the temperature and gate resistance effects on the failure evolution under short circuit conditions.

2. Failure modes

It is common to distinguish four failure modes under short circuit operation [7] as represented in figure 1. The failure mode A occurs at the beginning of the short circuit during the turn on. The reason can be the high applied voltage leading to early breakdown or to the latch-up phenomenon [1-2]. The failure mode B

occurs during the on state of the device, between turn on and turn off. The main origin is the second breakdown associated to the rapid increase of the intrinsic temperature [3-4]. The failure mode C occurs during the turn off transient, and [2; 6] explains that this kind of failure can occur due to a dynamic latch-up. The failure mode D occurs several micro seconds after turn off and this mechanism is associated to the temperature [5-8].

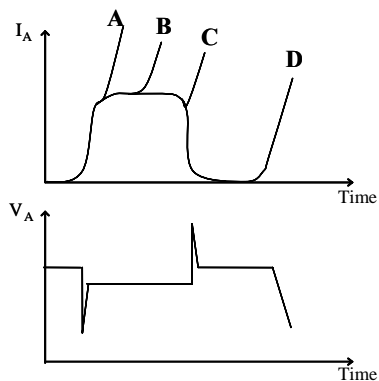


Fig. 1. Different failure modes under short circuit.

3. Device structure

The Trench IGBT investigated is controlled by a trench gate and it is a punch through type. So, the PNP emitter and the base are separated by a heavily doped N+ layer (figure 2). Lifetime is controlled by ion implantation. The maximum time during short circuit is about 10 μ s. The structure is 2 μ m width and 370 μ m long.

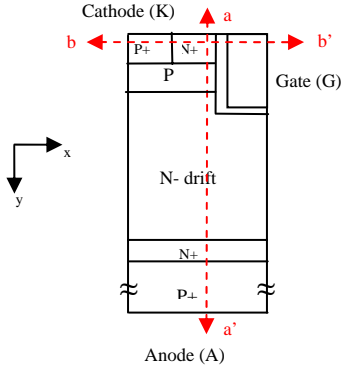


Fig.2. The structure of the Trench IGBT

4. Device model & simulation circuit

In order to perform a short circuit simulation model as realistic as possible, it is necessary to fit the static and dynamic characteristics for various temperatures, including the short circuit waveforms. In the simulator software, and by taking into account the main physical mechanisms like mobility degradation, recombination and impact ionization, always with temperature computation, it is possible to have a good matching between the measurements and the simulations. It is also important to consider electrical elements attached to the physical structure (figure 3). The physical simulation is performed with GENESISISE TCAD software [9].

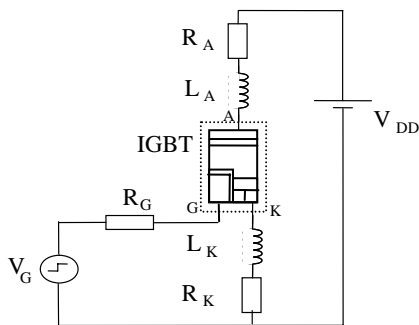


Fig.3. Short circuit simulation circuit

5. Results and discussion

Two electrical configurations under short circuit conditions has been chosen in order to investigate the

gate resistance and the temperature effects on the failure evolution : mode B and C.

5.1 Failure mechanism during on state : “mode B” and gate resistance variation effects

The failure under mode B of the trench IGBT is initiated under $V_{DD}=600V$ and $I_{csat}=300A$ at the temperature $T=298K$ under short circuit conditions. Figure 4 presents the simulation of the dynamic characteristic of the short circuit for different gate resistance R_g values (0 Ω , 1 Ω , 5 Ω , 50 Ω and 100 Ω).

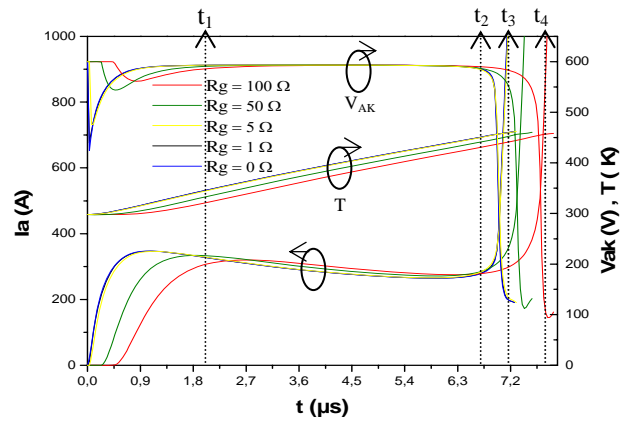


Fig.4. Global waveforms for mode B

It was highlighted that an increase of the gate resistance induces an increase of a delay at the turn on. Whereas, the gate resistance rise has a minor effect on the failure release, only the failure current slope is reduced with the gate resistance increase. A 2D analysis is presented for the gate resistance $R_g=1\Omega$ at three times t_1 , t_2 and t_3 and for $R_g=100\Omega$ at t_4 .

At time t_1 which corresponds to the time for a maximum current conduction under a high collector voltage, figure 5(a) depicts that the main current (electron current) runs through the channel of the MOSFET. The hole current is running through the P+ region to reach directly the cathode contact of the IGBT. At that time, since the collector voltage is high (600V), the electric field within the structure is maximum in the N drift region near to the Pbase / N drift junction. At this location, the value of the electric field is strong enough to generate carrier by impact ionization as indicated in figure 5(b) showing a moderate impact generation rate, the generated current represents 6.8% of the total current. The power density is maximum at the Pbase / N drift junction close to the channel where the current density is also high. As a consequence, the mapping of the temperature indicates that the temperature reaches a maximum value in the N drift region.

At time t_2 , the gate voltage is still applied. Figure 5(c) depicts that the electron current runs through the channel of the MOSFET and the hole current goes

through the P^+ region to reach directly the cathode contact of the IGBT. The electric field stays high along the reversed biased Pbase / N drift junction due to the high voltage continuously applied on the device. At the vicinity of this junction, the impact ionization (figure 5(d)) is higher and higher and reaches 13.2% of the total current. At this instant, the temperature mapping reaches a high value (but not the highest one during the short circuit).

At time t_3 , the gate voltage is still applied. The whole current is mainly composed by hole current running through the P^+ region. The electric field stays high along the reversed biased Pbase / N drift junction due to the high voltage continuously applied on the device (figure 5(e)). At the vicinity of this junction, the impact ionization distribution shown in figure 5(f) rises due to the rise of the current, the part of the generated current reaches 39.3% of total current. The power density still increases. At this instant, the temperature reaches its maximum value (about 450 K) due to the failure of the device (figure 4).

At time t_4 , which is taken during the failure as t_3 but for $R_g=100\Omega$, figure 5(g), represents the same current density distribution as in figure 5(e). Whereas in figure 5(h), the impact ionization repartition in the active region is less important for $R_g=100\Omega$.

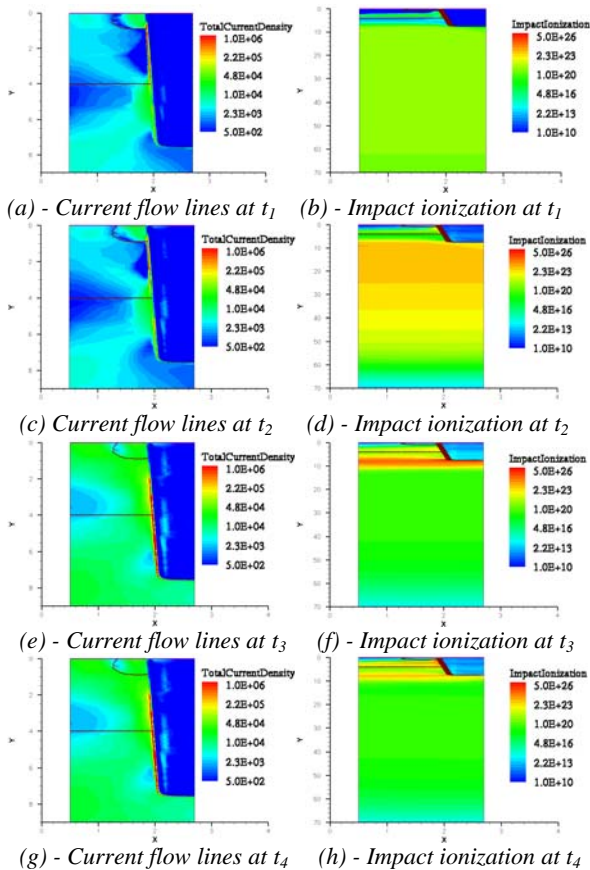


Fig.5. 2D physical distribution of some parameters during failure mode B.

When we consider the ratio between the hole and the electron current (depicted in figure 6) during the whole transient, we notice that this ratio keeps a constant value (about 0.6) before the failure. Figure 6 confirms this preliminary result. During the failure, the hole current becomes higher than electron current, we can conclude that there is no impact ionization mechanism leading to breakdown.

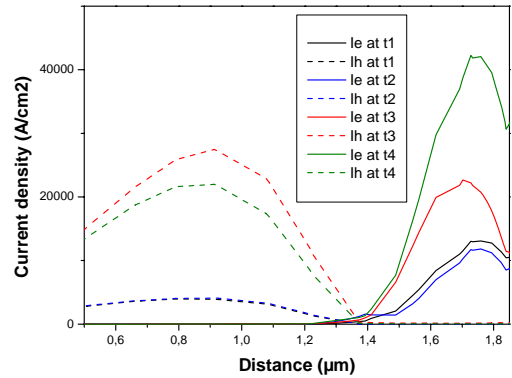


Fig.6. 1D current density evolution along b-b' cut line

5.2 Failure mechanism during turn off : “mode C” and temperature variation effects

The mode C failure analysis of the trench IGBT is initiated under $V_{DD}=250V$ and $I_{csat}=200A$ short circuit conditions with a gate resistance $R_g=1\Omega$. Figure 7 presents the simulation of the dynamic characteristic of short circuit for various temperature $T=298K$, $423K$ and $473K$. It was highlighted that an increase of the temperature seems to accelerate the destruction of the component. At $T=298K$, the failure occurs few microseconds after turn-off whereas at $T=473K$, the failure happens directly during turn-off. A 2D analysis is presented for the temperature $T=423K$ and three times t_1 , t_2 and t_3 are pointed out, whereas t_4 is an analysis time for the temperature $T=298K$.

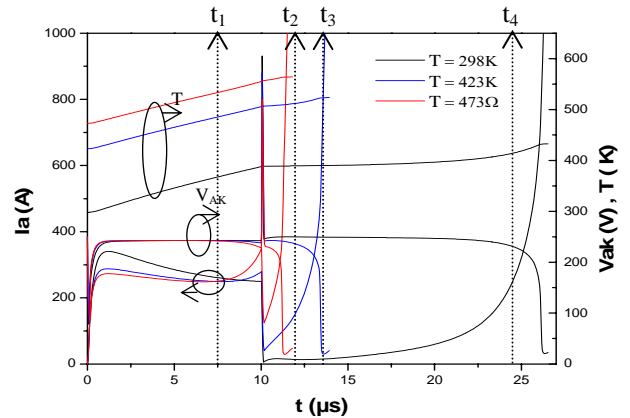


Fig.7. Global waveforms for mode C

At time t_1 which corresponds to the time for a maximum current conduction under a high collector

voltage, figure 8(a) depicts that the main current (electron current) runs through the channel of the MOSFET. The hole current is running through the P⁺ region to reach directly the cathode contact of the IGBT. At that time, since the collector voltage is high (200V), the electric field within the structure is maximum in the N drift region near the Pbase / N drift junction. At this location, the value of the electric field is not high enough to generate carriers by impact ionization. The power density is maximum at the Pbase / N drift junction close to the channel where the current density is also high. Then, the temperature mapping indicates that the highest value is maximum in the N drift region as shown in figure 8(b).

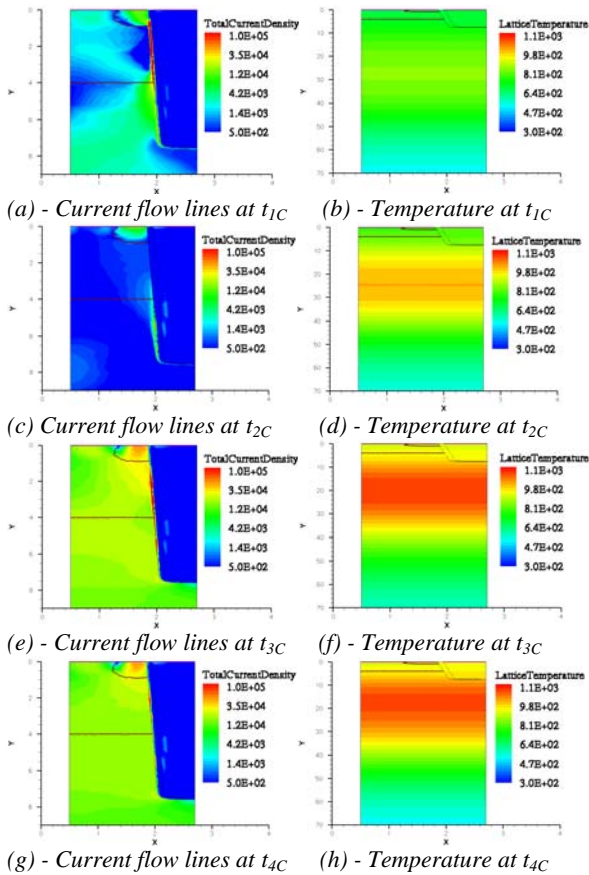


Fig.8. 2D physical distribution of some parameters during failure mode C.

At time t_2 , the gate voltage has been reduced to zero and the channel of the MOSFET has been cut off. The device did not turn off as expected and the whole current has been reduced but not removed completely from the structure (figure 8(c)). The electric field stays high along the reversed biased Pbase / N drift junction due to the high voltage continuously applied on the device. At the vicinity of this junction, the impact ionization is still low and the generated current only represents 0.2% of total collector current. The power density continues increasing. At this instant, the

temperature mapping (figure 8(d)) reaches a high value (but not the highest one during the short circuit).

At time t_3 , without any control on the gate electrode, the current starts running again inside the structure as depicted in figure 7. However, in figure 8(e), we can observe that the current runs not only through the P⁺ region but also through the base-emitter junction of the parasitic bipolar NPN component towards the N⁺ contact. The electric field is still high but the value starts decreasing with the decrease of the applied voltage and the increase of the current. The impact generation rate is low. The increase of the total current in the device induces an increase of the power density. This final stage corresponds to the device failure since the current can not be controlled anymore. In that case, the temperature mapping illustrated in figure 8(f) shows an increase of the temperature within the device with a highest value close to 1100K.

At time t_4 , which is taken to analyse the Trench IGBT at the temperature $T=298K$, we can observe on figure 8(g) that the current density distribution is the same as in figure 8(e); In fact, at t_3 for $T=423K$ and t_4 for $T=298K$, the component is failing, and the mechanism seems to be the same one for the two temperatures. The temperature distribution highlighted in figure 8(f) and 8(h) is similar at t_3 and t_4 . This observation is confirmed in figure 9.

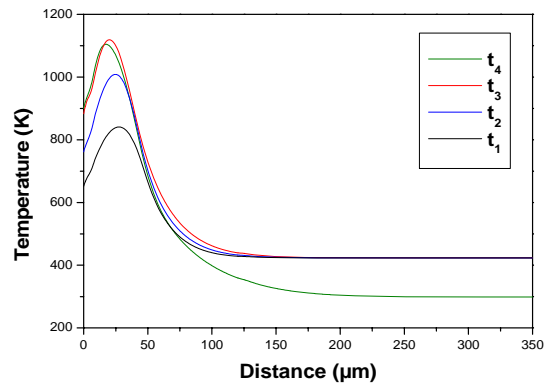


Fig.9. 1D temperature distribution along a-a' cut line

6. Summary

Table 1 gives a summary of the main phenomena which causes each failure mode on trench IGBT under short circuit conditions. Furthermore, it gives the tendencies of the influence of the applied gate resistances and of the temperature on the failure types.

Concerning the gate resistance and the temperature influence, for a fixed configuration of a failed short circuit simulation, an increase of the temperature will cause the failure earlier in time (from mode D to mode A). An increase of the gate resistance has more effect on the delay at turn-on and a low effect on the failure mode activation (from mode A to mode D).

Table 1
Sum up of the temperature and the gate resistance effects

	Gate voltage increasing	Temperature increasing	phenomena
Mode A	↓	↑	Impact Ionization
Mode B			Thermal runaway
Mode C			Thermal runaway
Mode D			Thermal runaway

7. Conclusion

The Trench IGBT physical internal behavior under various short circuit conditions has been investigated. For the failure mode occurring during the on-state and during turn-off, it was highlighted that a thermal runaway phenomenon is responsible on the spontaneous current increasing. The activation of the event leading to failure seems to be closely related to the dissipated energy within the structure. It was highlighted that the gate resistance variation has no significant effect on the short circuit capability, whereas it is improved by a temperature reduction in the chip.

References

- [1] L. Takata "Destruction mechanism of PT and NPT-IGBTs in the short circuit operation-an estimation from the quasi-stationary simulations", International Symposium on Power Semiconductor Devices Conference 2001, 4-7 June, pp: 327 – 330
- [2] T. Laska and al. "Short Circuit Properties of Trench-/Field-Stop IGBT's Design Aspects for a Superior Robustness", in Proc. International Symposium on Power Semiconductor Devices Conference., 2003, pp : 173-176.
- [3] M. Trivedi and al. "Investigation of the short-circuit performance of an IGBT", IEEE Transaction on Electron Device, vol.45, Issue: 1, Jan. 1998, pp: 313 - 320
- [4] M. Trivedi and al. "Failure mechanisms of IGBTs under short-circuit and clamped inductive switching stress", IEEE Transaction on Power Electronics, vol. 14, Issue: 1, Jan. 1999, pp: 108 – 116
- [5] S. Lefebvre and al. "Experimental Behavior of Single-Chip IGBT and COOLMOS Devices Under Repetitive Short-Circuit Conditions" IEEE Transaction on Electron Device, Vol. 52, No. 2, Feb. 2005
- [6] M. Ishiko and al. "Investigation of IGBT turn-on failure under high applied voltage operation", Microelectronics Reliability, Vol. 44, Iss. 9-11, Sept.-Nov. 2004, pp 1431-1436
- [7] A. Benmansour and al. "Failure mechanisms of Trench IGBT under various short-circuit conditions", accepted at Power Electronics Specialists Conference 2007, Orlando USA.
- [8] A. Benmansour and al. « Failure mechanism of trench IGBT under short-circuit after turn-off' Microelectronics and Reliability, vol.46, Iss. 9-11, Sept.-Nov. 2006, pp 1778-1783
- [9] ISE TCAD Software, V10