From Software-Defined to Software Radio: Analog Signal Processor Features

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***Abstract*— The RF transceivers architectures are to integrate the concept of Sotware Radio. But, in the case of mobile terminal, hard constraints are imposed by the factor of mobility. Low power and very complex circuits are claimed by the telecommunication industry. Classical architectures are no more sufficient to challenge this goal. New systems are thus proposed, and the concept of Software Defined Radio (SDR) is a step on the roadmap toward Software Radio (SR). This paper presents a state of the art of SDR circuits and explores the application of a Analog Signal Processor SR chip.**

***Index Terms*— analog signal processing, software-defined radio, cognitive radio, sampled analog signal processor.**

I. Introduction

THE concept of Sotware Radio as defined today was first introduced by the US Army. The first researches were developed during the 90's. Their main goal was to secure communications on hostile battlefield. The project "Speakeasy" was the first stone brought to that researches and opened all a new field in the telecommunication industry, military and civil ones. Mitola exposed a defined concept of Software Radio in 1999. It is described as a fully reconfigurable wireless device that adapts its communication variables in response to network and user demands.

Telecommunication industry has seen the opportunity to work on that principle. It is summed up by replacing several receiving chain in mobile phones, each one addressing a known standard, by a one-chip-solution. This unique chip is able to receive any telecommunication standards and can reconfigure itself using know communication standards. Industry targets

- a reduced cost of design (low cost technology like CMOS are required)
- a reduced cost of power consumption (less chips imply a power reduction)
- a reduced cost of human investment (all engineer works focused on one project)

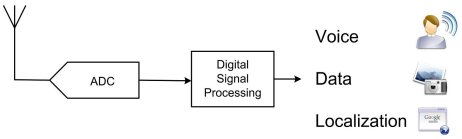

Fig. 1. Ideal Software Radio Receiving System

But nowadays, technological bottlenecks brake the development of a full SR receiving chain dedicated to mobile terminals (Fig. 1): RF signals coming from the antenna have to be converted into digital at least at twice RF frequencies (10GHz) with a high resolution (16 bits). Analog to Digital Convertors (ADC) responding to a low-power consumption adapted to a mobile terminal do not exist and are not expected to be realized before 15 years.

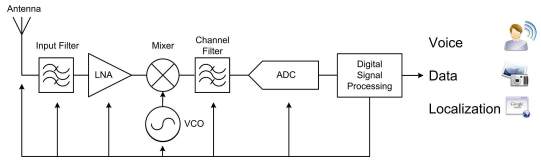

Fig. 2. Software Defined Radio Receiving System

Architectures are proposed to overcome this bottleneck. Traditional architectures are Software Defined Radio (SDR) architectures (Fig. 2). But, they limit their action to defined standards and can only operate in narrow band. Some offer windowed integrator to perform charge sampling. It plays on the anti-aliasing effect and enables to downconvert defined standards. These architectures are said to be multi-standards addressing the SDR concept (Fig. 3). They are still narrow band and are mainly analog [1], [2], [3], [4].

Other works on disruptive solution with an intensive research in analog Front End are proposed. Some explore

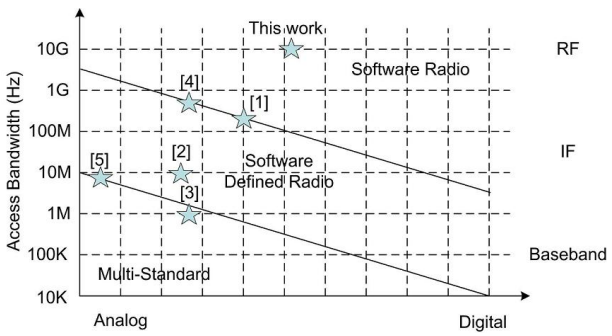

Fig. 3. State of the Art of SDR and SR systems

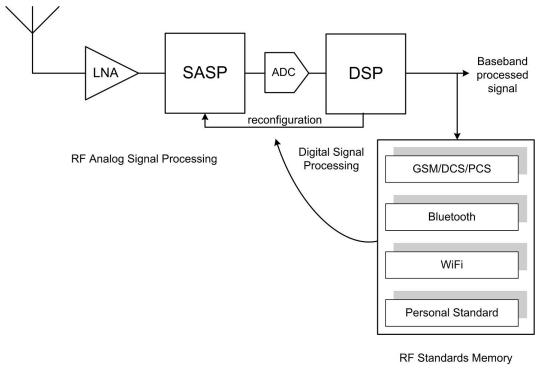

Fig. 4. Software Radio proposed system

discrete time analog signal processing in order to translate into analog domain the processing work usely done into digital [5] (Fig. 3). It enables better trade-off between reconfigurability and power consumption. This paper presents a Software Radio chip [6] that pre-process any RF signal directly after the antenna in order to reduce the ADC working frequency. It handles at the same time the good performance offered by discrete time analog signal processing and flexibility given by digital management ideally targeted by a SR device. The realization and the application of a Sampled Analog Signal Processor (SASP) [6] is exhibited. It is designed in 65nm CMOS technology from STMicrolectronics.

The SASP uses the principle of an analog discrete fourier tranform to translate into frequency domain the RF signal [6]. The calculation is based on voltage samples. Once the spectrum containing all information in a 0 to 5GHz range is processed, it is a matter to select the only one (or several) signal envelops to be demodulated. It is composed by few voltage samples among thousands. These samples are converted into digital for a digital signal processing. This system enables to treat any RF standards according to a low-power consumption given by analog signal processing and flexibility offered by a DSP. The DSP manages the use of stored standards and reconfigures as needed the parameters of the SASP. The standard memory can be updated and accepts news standards through old standards (Fig. 4).

II. The Sampled Analog Signal Processor

The SASP is designed in 65nm CMOS ST Microlelectronics technology. It aims at validating the concept of discrete time analog operations. Only 3 discrete time analog operations are required to perform a FFT: delay, add and weight. [7] describes every analog operation and its characteristics in the chosen technology. It enables to envisage a roadmap in the case of such analog processors dedicated to SR concept. Behavioral validation and processing applications are here proposed.

A. A Post Layout Simulation

The circuit considered here is a 64-point SASP (Fig. 5). It is a demonstrator sent to foundry to validate the feasibility

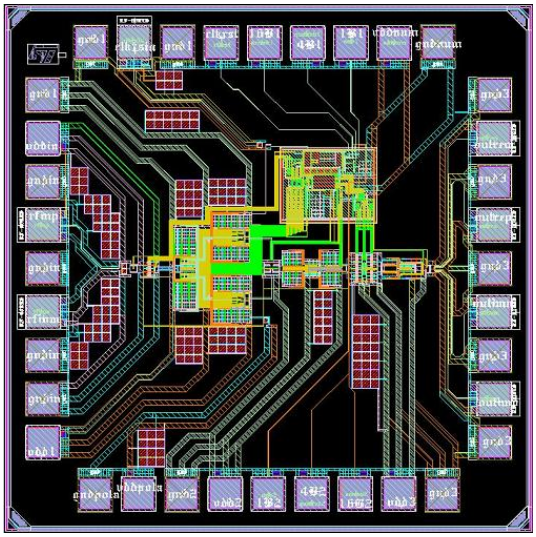

Fig. 5. 64-point SASP layout

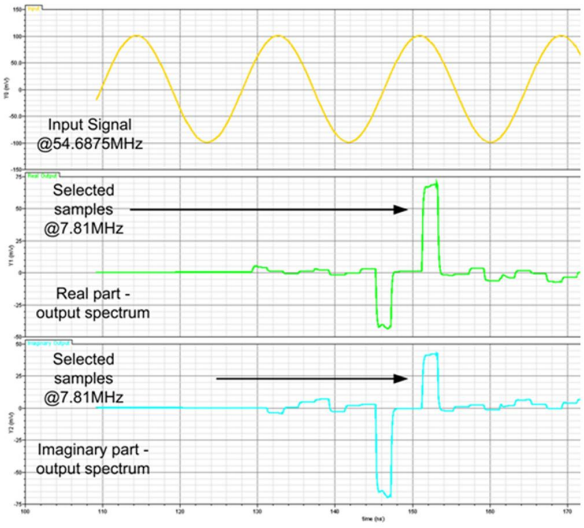

Fig. 6. 64-point SASP Post Layout Simulation

of the SASP. Its power consumption is 360mW with a 1.2V power supply. The input dynamic range is 200mV with a maximal functionnal sampling frequency of 1GHz. The die area is $1.44mm^2$.

A Post Layout Simulation (PLS) is done to validate the circuit behavior taking into account all the parasitic elements (Fig. 6). The SASP carries out analog operations on voltage samples of a sine wave with a frequency equal to $\frac{7*f_{sampling}}{64} = 54.6875MHz$. $f_{sampling}$ is equal to 500MHz. Only the 7th voltage sample processed by the processor on a FFT period is selected and displayed to an A/D convertor during all a FFT. It contains the phase and amplitude information of the input signal (Fig. 6). As expected, the spectrum is composed by 2 voltage samples per FFT processed. These samples are thus stored and displayed at the lowest frequency allowed equal to $\frac{500MHz}{64} = 7.8125MHz$. An A/D conversion is thus possible

TABLE I

RF STANDARDS ADDRESSED BY 65536-POINT SASP

System	Carrier Frequency	Channel Bandwidth	Modulation	Number of samples	$f_{sampling}$
GSM	925-960MHz	200kHz	GMSK	6	2.184GHz
DCS	1805-1880MHz	200kHz	GMSK	3	4.368GHz
UMTS	2110-2170MHz	5MHz	QPSK,HPSK	65	5.041GHz
Bluetooth	2402-2480MHz	1MHz	GFSK	12	5.461GHz
802.11g	2412-2472MHz	20MHz	OFDM	250	5.243GHz

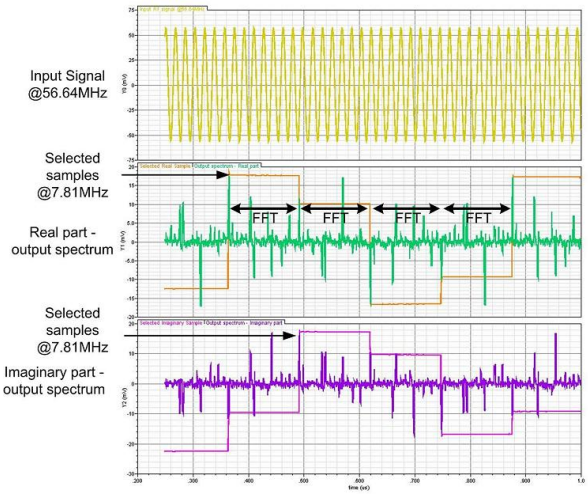

Fig. 7. A non-entire frequency sinewave processed by 64-point SASP

during that display time (128ns) at a lower frequency.

B. Frequency Demodulation Application

A sinewave equal $\frac{7.25*500MHz}{64}$ is sent (Fig. 7). The sampling frequency is still the same (500MHz). A dephasage is observed from FFT period to the next one. The sample selected in each processed spectrum exhibits the phase variation. As the sinewave input frequency is a quarter higher that an entire part of the sampling frequency, the spectrum is no more coherent between each FFT. The phase is shifted of $\frac{\pi}{2}$ at each processed FFT. It depicts that the sampling frequency $f_{sampling}$ can be one of the main parameter to configure the FFT processing. Phase and amplitude recovery can be done using directly the voltage samples. A demodulation is feasible into the frequency domain with optimized algorithm.

C. A Software Radio Chip

The chip is to be designed to process any RF standards. It must be able to handle enough voltage samples to display any signal envelope to the ADC. A study depicts the most used RF standards, their characteristics, and the SASP parameters to be applied to receive those standards (Tab. I). A 65536-point SASP is chosen to address any RF standards. It maximises the accuracy of signal processing and the covered frequency range. Tab. I exhibits the SASP configuration. The sampling frequency is the only parameter that enables an hardware reconfiguration. The selected voltage samples are to be processed digitally after their conversion into digital, which leads to re-invent the way of demodulating RF standards. This application is described as follows.

III. APPLICATIONS

Once the spectrum processed, an Inverse Fast Fourier Transform (IFFT) can be performed digitally to restore a baseband transient signal. A temporal demodulation can be done. This concept is not optimized in terms of performance and new applications can be explored by the use of the spectrum composed by the voltage samples. In fact, amplitude and phase information are directly caught by the spectrum. Modulations such as QPSK, QAM and by extension, OFDM car be treated by adapted algorithms in the frequency domain. The example of a QPSK modulation is here considered (Fig. 8). A 65536-point SASP is designed in VHDL-AMS language as defined in Tab. I. The sampling frequency is an entire number of times of the carrier frequency. QPSK encodes data by odd and even bits. 4 different phase shifting represents 4 pairs of bits. As the SASP is able to recover directly phase information at a given and stable frequency, it is easy to extract the 4 different phases. Once done, the demodulation is processed by the recognition of pairs of bits encoded in the phase information. If analog signal processing is enough accurate, a confident frequency demodulation is thus feasible.

This concept is well suited to OFDM modulation (Fig. 9). In fact, as the SASP performs a FFT, all the sub-carriers are directly demodulated and can be processed separately into digital. The A/D conversion and the digital processing speed are performed at a lower rate which implies a reduction of power consumption. Other applications can be imagined such as Frequency Hopping modulation types, easily demodulated by the mean of the spectrum.

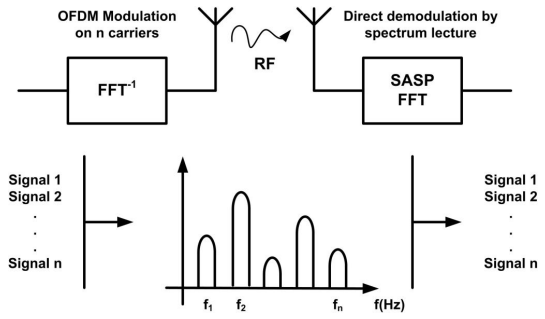

Fig. 9. A OFDM signal processed by the SASP

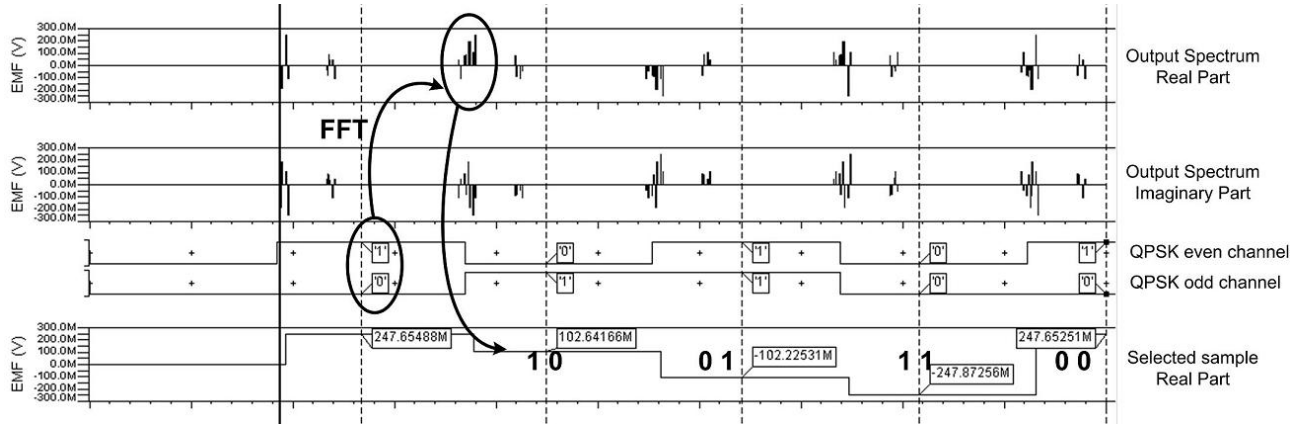

Fig. 8. A QPSK signal processed by 65536-point SASP

IV. Conclusion

This paper presents the applications of a Software Radio circuit that enables to receive any RF signals and displays phase and amplitude information into the frequency domain. It is dedicated to mobile terminals and answers to the constraints of power consumption and flexibility imposed by the Software Radio concept. Behavioral validation and layout design are performed. A technological roadmap is paved to a 65536-point SASP chip able to handle any RF standards. Frequency demodulation principle exhibits optimized signal processing using the performance of the SASP.

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