A 60GHz CMOS RMS Power Detector for Antenna Impedance Mismatch Detection

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***Abstract*— This paper presents a RMS power detector in 65nm CMOS for applications in WPAN 60GHz band. After presenting the context, the interest of power detection in RF transmitter chain is explained together with some 60GHz VSWR antenna measurements. Then, a state of the art of the detection techniques is given to justify our architecture choice and the operating principle is detailed. Finally, simulations results are presented which show a linear detection range of 25dB at 60GHz.**

I. INTRODUCTION

Millimeter-wave (mmW) frequencies, from 30GHz up to 300GHz, are historically the exclusive domain of III-V technologies. CMOS technology is now also able to support mmW applications with a significant gain of scale and cost. However, some limitations still occur for power amplifiers whose saturated output power can not go beyond 10dBm as detailed in [1], due to the very low breakdown voltage of standard CMOS devices. This low breakdown voltage implies a vulnerability of the PA due to the antenna impedance mismatch, which occurs when its close vicinity is obstructed.

Targeted application for this work is WPAN IEEE 802.15.3c [2], the next generation of short range telecommunication network using mmW signals between 57 and 64GHz which should provide data rates up to 3Gb/s.

Section II details the motivation to include a power detector in the mmW transmitter chain. A state of the art of existing detectors and couplers is then realized in section III. Finally, simulation results of the proposed solution are presented on section IV.

II. POWER DETECTOR ARCHITECTURE

As detailed in [3], there are three reasons for including an on-chip power detection circuit in a transmitter chain:

- A regulation loop with power detection allows Automatic Level Control (ALC) which can improve the linearity of the PA gain control, and which can also mitigate Process, Voltage and Temperature variations (PVT-variations).
- By reducing external test equipments in industrial production phase, a Build-In Seft Test (BIST) mechanism facilitates low-cost and high-volume test to detect failures in integrated circuits.
- By detecting antenna impedance variations, a regulation loop can limit the voltage standing wave ratio (VSWR) to improve the linearity of the PA-Antenna module. The regulation loop can also keep the PA well outside the breakdown region, therefore to enhance the device lifetime. For high VSWR, an emergency shutdown can be added to avoid the PA breakdown.

This work aims to underline the last point, the VSWR that occurs by variations of the antenna close vicinity.

A. VSWR Measurements

First of all, the VSWR variation range should be known before choosing an adapted solution to compensate this variation. Unfortunately, at mmW frequencies, the literature looks very poor on the subject, leaving us to realize our own measurements. Therefore, measurements were performed at mmW frequencies on reflection coefficient (S11) parameter of an antenna placed in two different conditions: in a free space to have a reference of the antenna; and in obstructed vicinity by placing a metal plane at various distances of the antenna.

The experiments were realized with a 4 elements circularly polarized patch antenna designed for 57GHz.

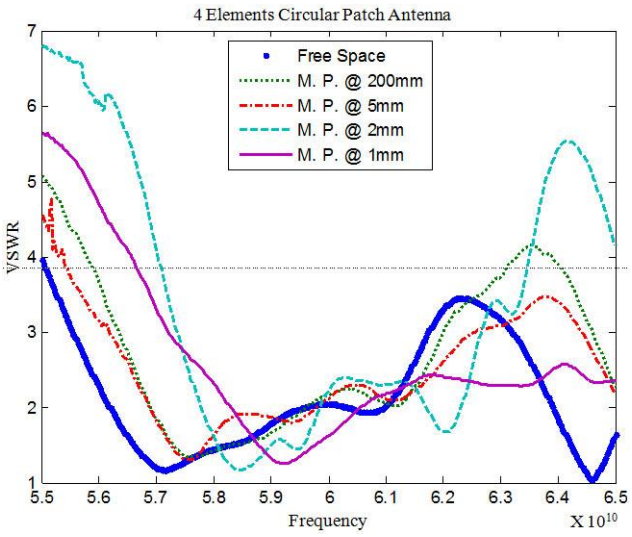

Figure 1. Measured results on the influence of a Metal Plane (M.P.) on Antenna VSWR.

Fig. 1 presents the Antenna VSWR versus the frequency for the different configurations of measurements (free space and different distances between the antenna and the metal plane MP).

The most important results are the increase of the center frequency of the antenna (detuning) and the increase of the VSWR at the antenna center frequency. Indeed, at 57GHz, Fig. 1 shows a peak of VSWR equal to 5:1 when the metal plane is placed at 2mm in its direction of radiation.

B. VSWR Effects on Power Amplifier

Impedance mismatch at PA output stage can have three kinds of effects. First, transistors can become saturated which results in a degradation of the PA linearity. Then, peak voltages can occur on the drain that can be higher that the transistor Breakdown Voltage and causes power transistor destruction. Finally, peak currents can be observed in the power transistor that implies too high power dissipation and results in the transistor destruction too.

In sub-micron CMOS technology, the main limitation is the low breakdown voltage [4]. Thus, using a CMOS technology, the output voltage is the parameter to be detected.

C. Architecture

Fig. 2 presents the architecture to be implemented. A detector unit is inserted between the power amplifier and the antenna. The detector output gives the information on the power of the signal at the antenna connector. This signal is then used by a feedback and decision loop to regulate the PA.

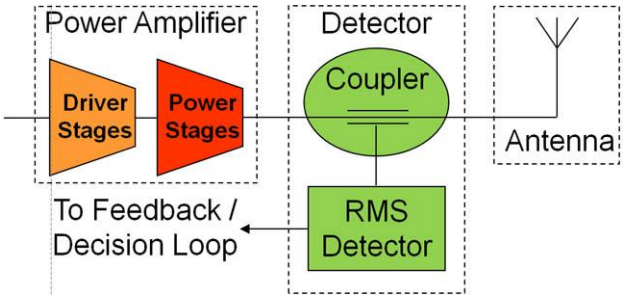

Figure 2. Architecture of the PA-Antenna module with a power detector.

The detector unit is formed by a coupler and a detector circuit. The coupler selects a part of the voltage at the PA output with minimal degradation of the RF signal. By using the detector circuit, the voltage coming from the coupler is converted into a power information (signal is squared and averaged).

III. POWER DETECTOR AND COUPLER DESIGN

A. Power Detector

There are two categories of detectors: peak and Root Mean Square (RMS). The first ones give information on the peak power whereas the second ones give information on the average power. A peak detector would have been used to realize a protection loop to avoid the PA breakdown. However, in order to regulate the average power at the PA output for Automatic Level Control and VSWR compensation as detailed in the previous section, a RMS detector will be preferred. Furthermore, workgroup IEEE 802.15.3c is working seriously towards the modulation standard OFDM [2], which implies a high Peak-to-Average Power Ratio (PAPR) – as high as 6dB – that means a waveform shape well-different from a sine wave. So the power detector should be a Root Mean Square (RMS) one, rather than a peak one which would not output the true average power of the transmitter.

There are several types of RMS power detectors mentioned in the literature which can be classified in two classes: thermal detectors and square law detectors. Thermal detectors [5, 6] like bolometers (e.g. thermistor or thermocoupler) convert the electrical power of the RF signal into thermal energy using a resistive component, and then measure the temperature variation with respect to the ambient temperature. Advantages of this method are a very wide bandwidth and a good accuracy between measured power and real power, but the main drawback is the chip implementation with coupling effects with adjacent circuits. For that reason, these detectors are principally used in instrumentation equipments.

Square law detectors use the characteristics of semiconductors components (diodes or transistors) to convert a voltage into a signal proportional to the RF power which is typically low-pass filtered to realize the average operation. A diode presents an exponential characteristics $I_D=f(V_{DS})$ which, near the threshold voltage V_T, can be assimilated to a square law versus the voltage, so linear versus the power [6, 7]. This kind of component is particularly useful for high frequency and low cost applications, but has the drawback of presenting a limited dynamic range as well as temperature dependence. They are used in instrumentation in complement of thermal detectors. Bipolar transistor characteristic is similarly exploited on a quite low working zone where exponential response can be assimilated to square law. This solution has been used by Pfeiffer in [3] and by Meyer in [7, 8]. The dynamic range is once again the limitation.

The dynamic range can be improved by using several detectors in ladder topology with attenuators and use the detector pair for whose output voltage ratio best approximates the gain of the attenuator, as explained in [7]. This results in an increase in the complexity, the size and the power consumption of the global detector.

Transistors can also be combined to provide the required square law transfer function as in Gilbert multiplier cells [9] or in translinear squarer-dividers [10], but this increases also the complexity and the consumption of the detector.

By using a standard CMOS technology, we can benefit from the naturally square-law characteristic of the MOS transistor in saturation. This can be done by using the simple single-ended Meyer cell as in [11], but, in order to facilitate the connection with the differential PA, we have chosen to implement the fundamentally differential circuit of Pfeiffer [3] using MOS transistors rather than bipolar transistors. Fig. 3 presents the schematic of this detector.

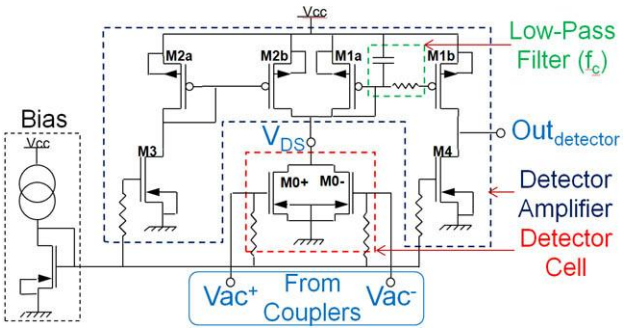

Figure 3. Schematic of the detector.

This application requires low transistor parasitic capacitances and also high f_T/f_{max} to address the mmW frequencies. That justifies the use of STMicroelectronics CMOS 65nm technology. Furthermore, all transistors are designed at L_{min}=65nm.

The power detector cell uses a pair of MOS transistors M_0^+ and M_0^- working in saturation to convert the differential voltage swing V_{ac} into a current that is proportional to the amplifier's output power. Each drain current is given by relation (1) where all constants have their usual meaning.

$$I_{DS} = \frac{kW}{2L}\left(V_{GS} - V_T\right)^2\left(1 + \lambda V_{DS}\right). \qquad (1)$$

V_{GS} is a sine-wave signal of V_{ac} amplitude at ω_0 around the biasing point V_{pol} (2).

$$\begin{cases} V_{GS}^{+} = V_{pol} + V_{ac}.\cos\left(\omega_0 t\right) \\ V_{GS}^{-} = V_{pol} - V_{ac}.\cos\left(\omega_0 t\right) \end{cases}. \qquad (2)$$

The sum I_{DS} of both drain currents is proportional to a sum of a biasing current and the squared input voltage (3).

$$I_{DS} \propto \left(2\left(V_{pol} - V_T\right)^2 + \left(V_{ac}\cos\left(\omega_0 t\right)\right)^2\right). \qquad (3)$$

The cosine squared produces mixing components that can be low-pass filtered to produce a DC current that is proportional to the true RMS power.

B. Power Couplers

A power coupler is needed to collect a part of the energy from the T-line to the detector circuit while having minimal effect on original RF signal. Literature presents two kinds of couplers: directional and capacitive couplers.

Directional couplers consist of two coupled transmission lines (coplanar), the main line linking the output of the PA to the antenna connector, and the second line linking the detector input to a matched load. They are often used as an external or on-board component in transmitter architectures.

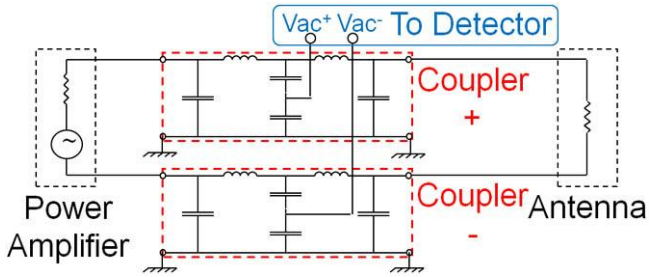

Figure 4. Equivalent schematic of the couplers.

The major drawback is the high insertion loss as high as -3dB in this e.g. CMOS directional coupler [12]. For that reason we choose to use a capacitive coupler. Fig. 4 presents an electrical equivalent model of the differential coupler (formed by two single ended couplers).

Capacitive couplers use capacitors to collect the energy from the T-line to the detector. In practice, a little metal rectangle is inserted under the T-line that creates two capacities: one in respect to the line and the second to the grounded substrate. That results in a capacitive divider. This king of coupler has been used by Pfeiffer in [3] where the insertion losses of the coupler region of the T-line look insignificant.

IV. Power Detector Simulations

A. SNR Limitations

To determine the dynamic range of the detector which is limited at low power by the noise of the detector cell (M_0^+ and M_0^-), the SNR (Signal to Noise Ratio) of this cell has been calculated. Starting from the characteristics of the desired NMOS obtained by a DC simulation with Cadence, the waveforms of the current output signal I_{DS}^+ and I_{DS}^- of transistors M_0^+ and M_0^- are computed by applying a 60GHz sine-wave voltage on the grid of each MOS transistor. In the same time, the noise current spectral density *Snid* can be calculated using the saturation MOS equation:

$$Snid = 8/3.kTgm \quad \left[in\ A^2 / Hz\right]; \qquad (4)$$

where the transconductance *gm* is derived from the initial MOS transistor characteristic ($gm = \Delta I_{DS}/\Delta V_{GS}$).

Considering a white noise low-pass filtered signal (cutoff frequency f_c), the SNR is given by the equation:

$$SNR = \left(\overline{Ids}\right)^2 \Big/ \left(\overline{Snid}.\frac{\pi}{2} f_c\right). \qquad (5)$$

By varying the biasing point via the bias circuitry, those SNR simulations show us a maximum of detection range (when *SNR>0dB*) presented on Fig. 5. P_{ac} is the power of the differential signal between the coupler and the detector; which is proportional to the power at the antenna connector with the ratio of coupler voltage attenuation squared.

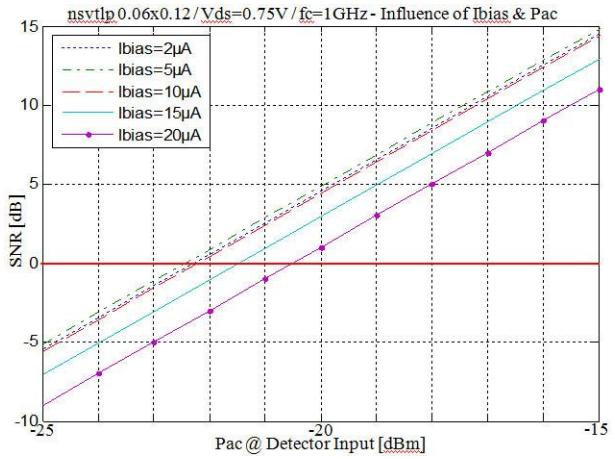

Figure 5. Influence of biasing on the SNR of the detector cell.

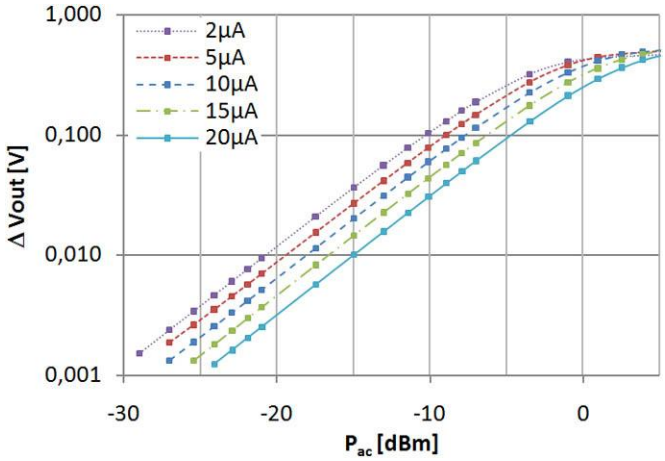

Figure 6. Transient simulations results of full detector working at 60GHz.

As can be seen from equation (5), the main parameter is the f_c frequency which has an influence of -10dB/dec on the detector SNR. Nevertheless, these simulations have shown that the drain-source voltage V_{DS} of the MOS has practically no influence on the dynamic range of the detector.

B. Transient Simulations

The detector cell is then associated to the detector amplifier and low-pass filter for the electrical transient simulation using Cadence. The design implementation is realized in STMicroelectronics CMOS 65nm technology. Fig. 6 presents the influence of the biasing on the output signal variation.

For high power levels, the detection range of the detector with its amplifier is reduced by the amplifier saturation, which occurs when the amplifier goes outside its linear range.

With a constant filter capacitance of 100fF, corresponding to a cutoff frequency between 37 and 140MHz depending of the biasing, which is a typical case when tuning an implemented device, the detection range is quite constant independently of the biasing, equal to 25dB. With a fixed cutoff frequency of 1GHz, the dynamic range of the detector is reduced to 20dB for low polarization levels and 23dB for high polarization levels.

V. CONCLUSION

A CMOS power detector has been designed and shows promising results in Cadence transient simulations, as summarized in Tab. 1. SNR limitations of detector cell have been studied. A circuit implementation of this detector including the coupler is under design in STMicroelectronics CMOS 65nm process.

TABLE I. COMPARISON OF POWER DETECTOR

	This Work	**Pfeiffer [3]**
Included Components	Detector	Coupler & Detector
Technology	65nm CMOS	0.13µm SiGe BiCMOS
Bandwidth	From 37 to 140MHz	13.8MHz
Linear Detection Range	25dB	8.5dB

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