

# Flyback Converter Surface Minimization: Design Procedure and Formulas

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**Abstract**—This paper gives generic formulas to account for power components surface in the design of a flyback converter. Starting from the converter requirements, key design parameters are defined, and their influence on converter surface studied. It is shown that some parameters have opposite actions, thus some trade-off must be found. On the other hand, additional constraints must be taken into account, especially losses. These ones are also evaluated using analytic formulas, and included in the design procedure. After design, the converter has been built, and compared to previous version, surface reduction is obvious.

## I. INTRODUCTION

Flyback converters are used in many low power applications. Very often, increasing power density is a key feature. For several applications, conventional PCB is used, and plugged into standardized racks. The power density increase corresponds then to a surface reduction (with often a maximum height requirement).

Designing a power converter with respect to a minimal surface means to set up an optimization strategy. The design variables must be chosen such as a minimum surface can be reached. However in the same time, other constraints must be fulfilled: external requirements obviously, but also other technological parameters, such as maximum losses in the components, or peak voltage on the semiconductors... Last, if a maximal height is required, component choice must account for this geometrical constraint.

This paper has thus the same goal as other design procedures explained in [1-2]. However, the proposed method does not rely on complex computer aided methods, as expert systems or heavy time simulation. For a dedicated application, such as the Flyback converters used in this paper, a fully analytical method is available, what allows simple use in any conventional software, as a Mathcad sheet for example.

In the first section of this paper, the topology to be designed will be presented. Then, design procedure will be detailed. First, the choice of the minimum number of design parameters will be presented. Then, all physical phenomena to be accounted for during the design will be listed. Analytical expressions will be given in section IV, and exploited in section V to propose some design trade off curves. The main difficulty is that the proposed expressions must be valid for any kind of design parameters value; this means that they must handle either continuous or discontinuous conduction mode. Validation of the proposed design will be proposed in section VI.

## II. CONVERTER REQUIREMENTS AND TOPOLOGY

The application illustrating our design method is a Switched Mode Power Supply (SMPS) with following requirements (for auxiliary feeding in railway applications):

- PCB size [mm\*mm\*mm] : 100 \* 160 \* 41.6
  - Output Power [W] : 70
  - Frequency [kHz] :  $20 < F < 45$
  - Input voltage [V] :  $43 < V_{in} < 137 \Rightarrow$  the design was achieved for 43 V (most constraint for the current), except for MOSFET voltage, taken from 137V
  - Output voltage [V] : 24 (0.6A), 12 (3A), 5 (0.5A), 3.3 (2.4A).  $\Rightarrow$  we defined a 12 V SMPS, and for the design, we have considered the total power on this output
- The converter topology has been chosen as a half Bridge Flyback structure (Figure 1. ), well adapted to this power range, with the advantage of recycling leakage energy, instead of dissipating it [3]. The behaviour of this converter is well known. For  $0 < t < \alpha.t$ , both switches are turned on: transformer is thus magnetized under voltage  $V_e$ . Output Diode is off and must handle reverse voltage ( $m.V_e + V_s$ ), where  $V_e$  and  $V_s$  are input and output voltage respectively, and  $m$  the transformer ratio. At  $t = \alpha.t$ , the two switches are turned off, demagnetization occurs first on the primary side, due to transformer leakage. This phase is neglected in the design phase, except for primary switch voltage constraint, which is imposed at  $V_e$ . Then, the conventional demagnetization on the secondary side occurs. The two switches must handle  $V_e + V_s/m$ . A reasonable assumption is that the two switches share this voltage equally. Therefore, each switch must blocks  $(V_e + V_s/m)/2$ .

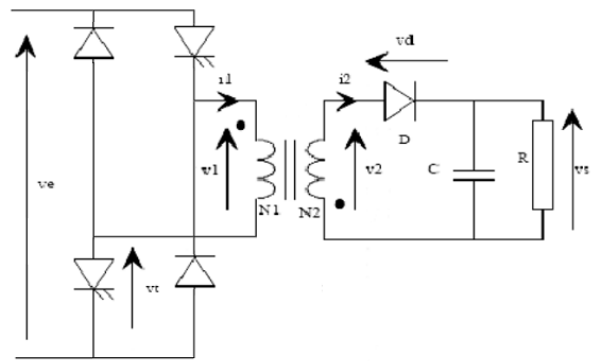


Figure 1. Half Bridge Flyback Structure.

### III. DESIGN PROCEDURE

As briefly mentioned in the introduction, the main goal of this paper is to optimize a Flyback converter. An optimization process consists in finding a correct set of design variable values that maximize or minimize a given objective function. In our application, the converter surface will be chosen as objective. However, several constraints must be fulfilled, what leads to a non obvious problem. Usually, the designer starts from his knowledge of the converter and focuses his attention on the most critical component. In the Flyback converter, it is obviously the transformer, which is bulky and the most complex component to be designed. Therefore, the converter optimization often results in a transformer optimization, and the other components are just considered using constraints. However, the converter optimum is not reached for every component optimum, and the best solution must account for all problems simultaneously. Therefore, we first modelled the complete Flyback behaviour, expressing all waveforms and associated results in a close form. Then, the objective function (surface) and all constraints could be expressed. Starting from external requirements only (input and output voltage  $-V_e$  and  $V_s$ - and power  $-P$ -), it is thus possible to carry on the surface minimization.

The components included in surface computation will be the transformer and the output capacitor (input capacitor is designed with respect to energy tank considerations, what is out of the scope of this paper). For simplification, we considered that for the power range of interest, semiconductor devices will be implemented in a TO-220 package associated with localized heatsinks. Therefore, whatever the converter design, it won't affect the surface minimization. Thus, heatsinks and semiconductors haven't been taken into account in the surface computation. However, losses have been computed, in order to guarantee a maximal temperature on the silicon dies.

#### A. Design parameters definition

The objective function and all constraints are deduced from converter waveforms, either directly (for instance semiconductor peak voltage) or after data processing. As illustrated in Figure 2., for both Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM), they depend on:

- switching frequency  $f$
- duty cycle  $\alpha$
- Magnetizing inductance  $L1$
- transformer ratio  $m = n1/n2$

However, due to fixed power, input and output voltages, duty cycle can be expressed as a function of the other parameters:

$$\alpha = \frac{V_s \cdot m}{V_s \cdot m + V_e} \text{ in CCM, and } \alpha = \sqrt{\frac{2 \cdot L1 \cdot f \cdot P}{V_e^2}} \text{ in DCM}$$

The design parameters are thus only  $f$ ,  $m$  and  $L1$ . To be noticed that due to the pre-regulation function of this converter, output voltage ripple is not really constraint, thus, output capacitor value is not a design parameter. After design, it just must be checked that the capacitance is not too small. In fact, the most important constraint for the capacitor is its rms current.

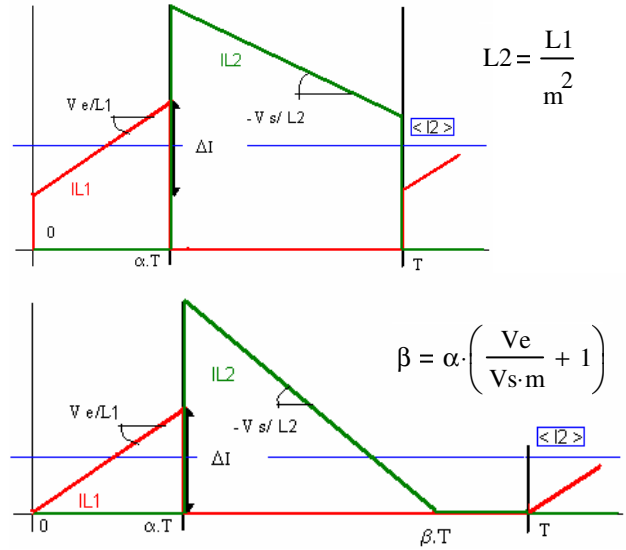


Figure 2. Flyback Waveforms for CCM and DCM.

#### B. Surface computation

The aim of this paper is to minimize the surface of the passive elements. Thus, they must be evaluated as a function of the design parameters. For a given technology, the surface of the output capacitor is linked to its rms current. Based on a 35V Electrolytic capacitor serie [4], the capacitor surface has been plotted as a function of its rms capability (Figure 3.). It is clear from this figure that a quadratic approximation can be made, what is not quite surprising since capacitor surface is linked to its ability to evacuate the losses, which depend on the quadratic value of the rms current.

The transformer surface is obviously linked to its design. A well known design method is the area product [5]. The transformer Area Product  $A_e \cdot S_f$  (winding area \* core area) can be expressed as a function of peak primary current and rms primary and secondary currents. Analytical expression can thus be derived as a function of the three design parameters, for both CCM and DCM. For a given core series, the surface occupied by the transformer can be linked to this area product using the same idea as the one proposed in [6]

$$S_{transf} = K \cdot \sqrt{A_e \cdot S_f}$$

$K$  has been computed to 14.5, according to ETD core series. Therefore, the transformer surface is linked to the three design parameters.

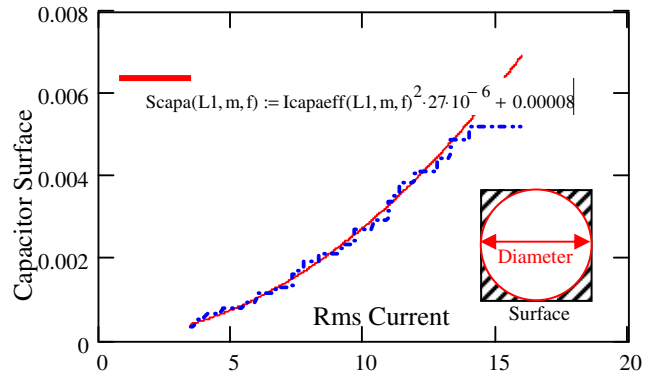


Figure 3. Capacitor surface vs rms current (blue dotted line), and the quadratic approximation (red line), for a 35V electrolytic serie.

### C. Losses and other constraints computation

Since all peak, average and rms currents can be expressed as a function of the design parameters, semiconductor losses can be computed, using well known losses models of semiconductors: voltage drop and resistance for diode, resistance for MOSFET. Switching losses can be estimated from switching times, peak currents and voltages applied to the semiconductors [7].

For transformer losses, if the peak induction and the magnetic material are fixed, losses may be estimated from manufacturer datasheet, even if accuracy is poor. It is important to account for this parameter, because it directly impacts the working of the Flyback: a high peak induction will allow reducing the area product and thus selecting a smaller core. On the other hand, it increases losses, which must be maintained under a given value. Copper losses cannot be precisely computed, due to the difficulty of considering proximity losses. However, a maximum current density is fixed, what allows maintaining reasonable losses. An estimate using DC resistor value can also be proposed.

Another key parameter for the transformer design is linked to the airgap: this one cannot be too large otherwise, leakage will increase. Even if leakage energy is recycled in this topology, a bad coupling is not desirable. Therefore, a maximum airgap is fixed. This one depends on the core size. In fact, the ratio Core\_width/Airgap is fixed. For instance, for ETD 39 [8] core, it corresponds to a 2 mm max airgap.

Capacitor losses can be computed from rms current and esr value, which may be interpolated from manufacturer datasheet, as for capacitor surface in Figure 4. However, this has not been accounted in this study, since most of the losses are generated in the semiconductor and the transformer.

Voltage overshoot on the MOSFETS and the secondary diode is linked to the normal behavior of the and to transformer ratio. It is a constraint for semiconductor choice (computed for 137V).

Duty cycle must stay within 0.1 (minimum technologically available) and 0.5, due to half bridge topology.

### D. Surface Minimization

Having expressed the passive component surface, the losses and the constraints as a function of the design parameters, a set of design parameters achieving the minimum surface, satisfying all constraints can be selected (see section V). Then, the core reference can be selected, as well as the actual capacitor.

### E. Parameter adjustment

After having selected the set of parameters corresponding to a minimum surface, and fulfilling all constraints, the core of the transformer is thus chosen. However, as illustrated in Figure 4, the actual surface is always bigger than the needed area product. Therefore, once the core has been selected, a second optimization can be carried out. Design parameters are then modified to exploit this core at the best. For this purpose, two compromises can be chosen. Either the design values may be changed to reduce capacitor size, then resulting in the best possible surface using this core. Another solution is to try to improve efficiency. In this case, frequency can be

reduced so that losses are reduced. This frequency decrease is achieved in conjunction with a change in magnetizing inductor L1, so that the final result still corresponds to the optimal total surface. The complete methodology is shown on Figure 5, and will be illustrated in section VI.

## IV. ANALYTICAL FORMULAS

All formulas have been implemented in a Mathcad sheet. In APPENDIX are only summarized the main equations. First is shown how to express the surface area product  $A_e.S_f$ , depending on the current conduction mode. The selection of the correct formula is achieved using the appropriate relationship that can be established at the limit between these two modes.

Rms current in output capacitor can also be computed from the knowledge of current waveforms. All other equations allowing constraints evaluation can be easily obtained, especially using some formal computations available in Mathcad.

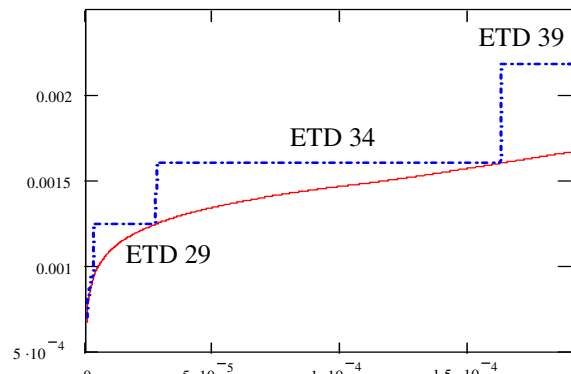


Figure 4. Surface computed from area product (vs magnetizing inductance), and the actual cores which must be chosen

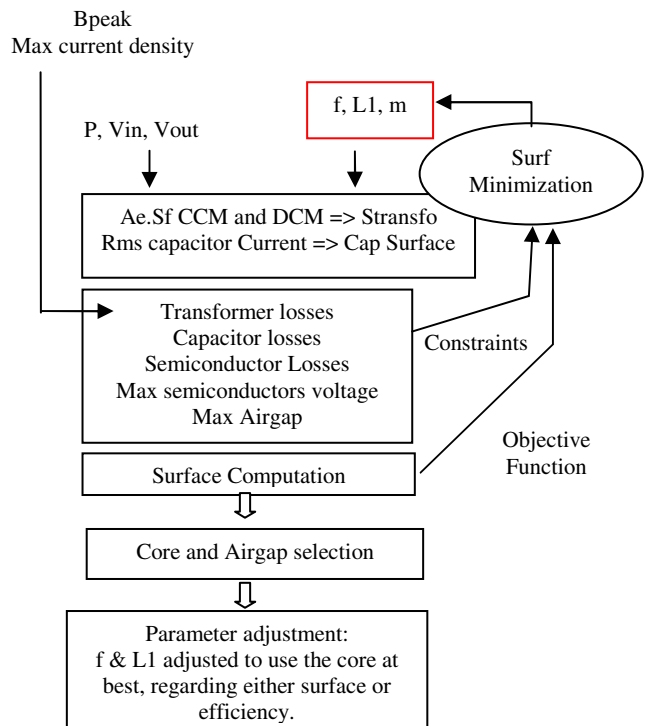


Figure 5. Surface minimization process.

## V. DESIGN TRADE-OFF

Before achieving the optimization, we first studied the influence of each parameter on the total surface, computed using analytical formula. Frequency increase results in a smaller surface, what is obvious (Figure 6. ). Other parameter variation exhibit more interesting behaviors: Optimum surface appears when varying transformer ratio  $m$  or magnetizing inductance  $L1$  (Figure 7. and Figure 8. ). It is a good illustration that the Flyback optimum does not results from the transformer optimum. Indeed, the transformer surface shows a monotonous variation as a function of all parameters: decreasing with frequency, increasing with magnetizing inductance, decreasing with transformer ratio  $m$ .

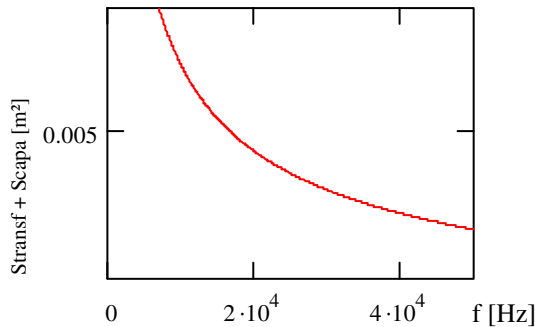


Figure 6. Influence of switching frequency on total surface (transformer + output capacitor). Curve obtained for  $L1 = 52\mu\text{H}$ ,  $m = 3$ ,  $B_{\text{peak}} = 0,22 \text{ T}$

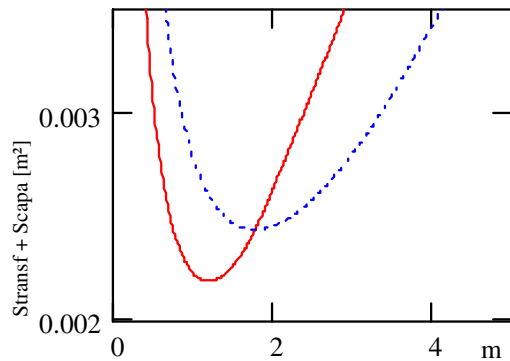


Figure 7. Influence of transformer ratio  $m$  on total surface (transformer + output capacitor). Curve obtained for  $f = 30\text{kHz}$ ,  $B_{\text{peak}} = 0,22 \text{ T}$ ,  $L1 = 52\mu\text{H}$  (solid) and  $L1 = 110\mu\text{H}$  (dotted)

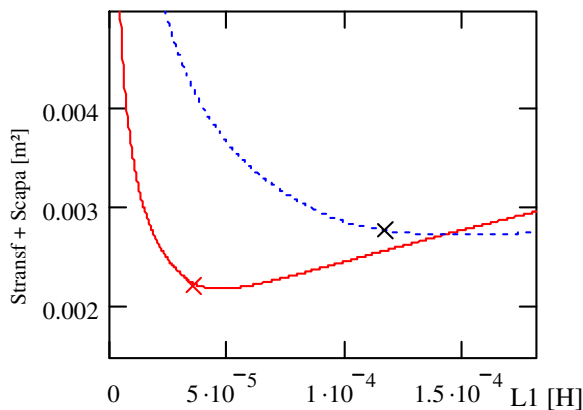


Figure 8. Influence of magnetizing inductance on total surface (transformer + output capacitor). Curve obtained for  $f = 30\text{kHz}$ ,  $B_{\text{peak}} = 0,22 \text{ T}$ ,  $m = 1,3$  (solid) and  $m = 3$  (dotted)

To help in selecting the good design parameters, the surface has been plotted as a function of magnetizing inductance  $L1$  and transformer ratio  $m$ , for different frequencies (Figure 9. ). It can be noticed that frequency does not modify the surface shape significantly. This can be explained by the monotonous variation of the surface versus frequency (Figure 6. ).

The optimization leads to the choice of  $m = 1,3$ ,  $L1 = 36\mu\text{H}$  and  $f = 40\text{kHz}$  for satisfying all constraints, and especially semiconductors and transformer losses. However, for this design, the selected core (ETD34) is not fully used, as illustrated Figure 11. Indeed, once the core has been chosen, the area product is fixed, and it is nonsense not to using it. Therefore, a first solution is to increase the magnetizing inductor  $L1$  until ETD34 is fully used. This  $L1$  increase results in a decrease of RMS current in the capacitors, and therefore a surface minimization. In Figure 10. this corresponds to  $L1 = 55\mu\text{H}$  with the same frequency (40kHz).

Another solution is to try to reduce losses by reducing the switching frequency. In this case, a new value of  $L1$  must be computed in order to keep the surface minimum. The  $f$  &  $L1$  parameters must be determined conjointly, checking that ETD34 is still used optimally. In the treated example, the solution has been found to be  $30\text{kHz} - 44\mu\text{H}$  (Figure 10 & Figure 11. ). This lower frequency allows reducing the thermal constraints and increasing the converter efficiency.

## VI. CONVERTER REALIZATION AND TESTS

The final choice has been  $L1 = 44\mu\text{H}$ ,  $m = 1,3$ ,  $f = 30\text{kHz}$ . The transformer is built with an ETD 34 core,  $n1 = 23$ ,  $n2 = 17$ , air gap has been computed at  $1,5 \text{ mm}$  and peak induction has been imposed at  $220\text{mT}$ . This optimized design is not far from discontinuous conduction mode, what is quite reassuring since this corresponds to the minimum stored energy in the transformer.

Global efficiency has been measured to validate losses models and achieve a sensibility study (Figure 13. ). Obviously, accuracy is not very good with these design models, but the error is not so big (88% expected, 83% obtained; Remember that capacitor losses were neglected).

Compared to the initial design, a significant surface reduction has been achieved. Indeed, on the same surface as the initial power supply, keeping the same height (because the PCB was inserted in a rack), 70W has been reached, compared to 35W initially. The power density was thus doubled thanks to an optimal design.

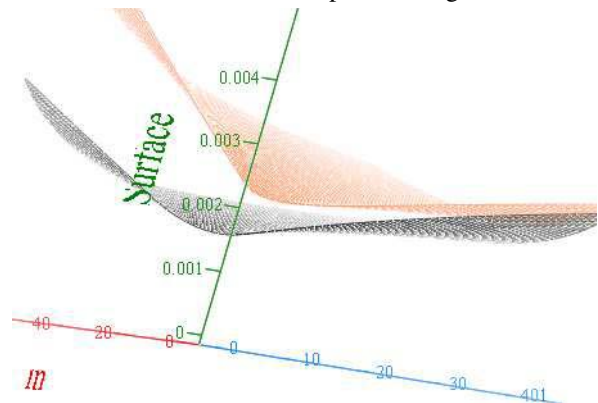


Figure 9. Surface vs magn. inductance  $L1$  and transformer ratio  $m$  (illustration purpose only – scale not available for  $m$  and  $L1$  axis).

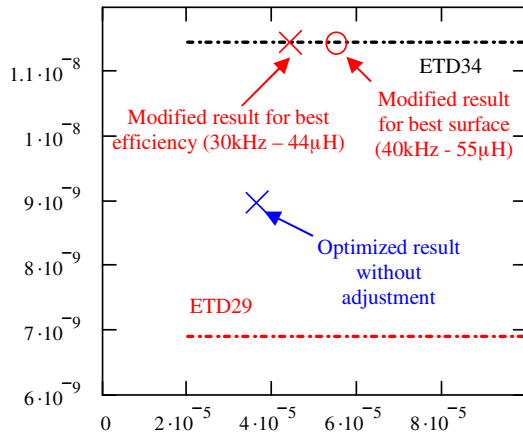


Figure 10. Use of Core ETD34. Comparison between optimized result (without accounting for core reference discretization), adjustment for better surface, adjustment for better efficiency.

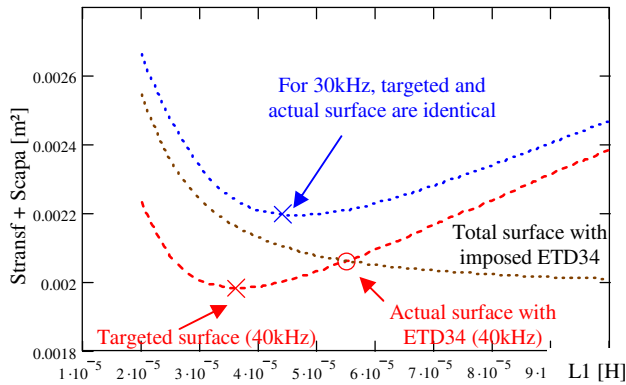


Figure 11. Parameter adjustment once the core has been selected. The set of design parameters ( $m = 1.3$ ,  $L_m = 36\mu\text{H}$ ,  $f = 40\text{kHz}$ ) is no more optimal when selecting the core ETD34

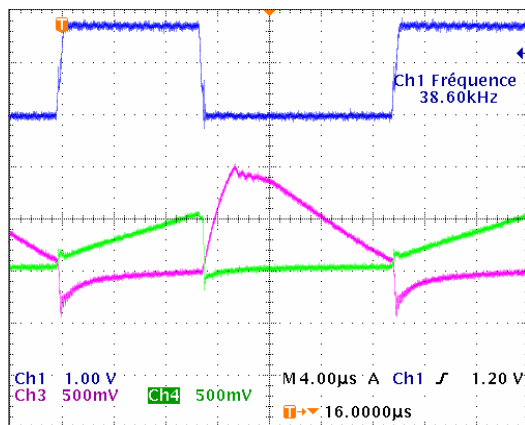
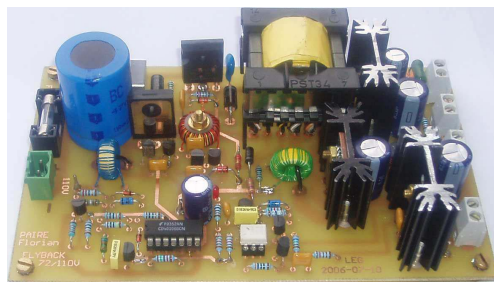


Figure 12. The realized converter and nominal load experimental wave forms at 45V input voltage.

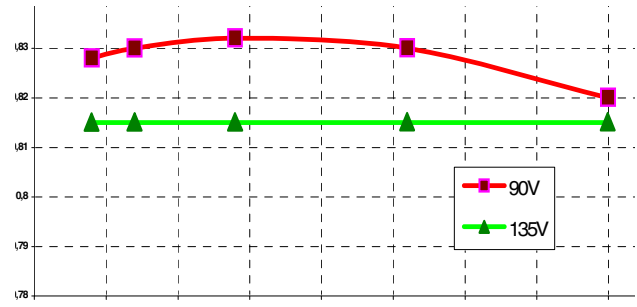


Figure 13. Efficiency vs Frequency for two input voltages.

## VII. CONCLUSION

In this paper, a fully analytical modeling of a Flyback converter has been proposed and implemented in a simple Mathcad sheet. This analytical description accounts for both continuous and discontinuous conduction mode and is therefore general. Thanks to some approximations, the area of passive components (transformer and output capacitor) can be computed. Transformer surface is linked to the well known area product, whereas output capacitor surface is correlated to rms current. The global surface (transformer + capacitor) depends on 3 parameters only, and exploring the space of solutions has allowed minimizing the surface, respecting all constraints on the components. After optimization, some adjustments have to be done, in order to account for the discrete nature of core references. Several options are possible: either pure surface minimization, or improving efficiency. Therefore, the power density has been doubled compared to initial power supply. Thanks to the analytical formulas, any other compromise or optimization goal may be easily reached. For instance a new design with the best efficiency on a given surface would only take a few minutes.

## ACKNOWLEDGMENT

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### CCM-DCM limit determination

$$L1lin(m, f) := \frac{1}{2} \cdot V_e^2 \cdot \left( V_s \cdot \frac{m}{V_s \cdot m + V_e} \right)^2 \cdot \frac{1}{P \cdot f}$$

### Area Product

$$AeSf(L1, m, f, B) := \begin{cases} SferScuCC(L1, m, f, B) & \text{if } L1 > L1lin(m, f) \\ SferScuCD(L1, m, f, B) & \text{otherwise} \end{cases}$$

$$AeSfCC(L1, m, f, B) := \begin{cases} L2 \leftarrow \frac{L1}{m^2} \\ \alpha \leftarrow V_s \cdot \frac{m}{V_s \cdot m + V_e} \\ T \leftarrow \frac{1}{f} \\ \Delta i \leftarrow \frac{V_e}{L1} \cdot \alpha \cdot T \\ IL2max \leftarrow m \cdot \left( \frac{P}{V_e \alpha} + \frac{1}{2} \cdot \Delta i \right) \\ \frac{L1 \cdot IL1max(L1, m, f)}{B} \cdot \left( \frac{kb1}{J1} \cdot IT1effCC(L1, m, f) + \frac{kb2}{J2 \cdot m} \cdot IdeffCC(L1, m, f) \right) \end{cases}$$

$$AeSfCD(L1, m, f, B) := \begin{cases} L2 \leftarrow \frac{L1}{m^2} \\ \alpha \leftarrow \sqrt{\frac{2 \cdot L1 \cdot f \cdot V_s \cdot L2}{V_e^2}} \\ T \leftarrow \frac{1}{f} \\ IL1max \leftarrow \left( \frac{V_e}{L1} \cdot \alpha \cdot T \right) \\ \frac{L1 \cdot IL1max(L1, m, f)}{B} \cdot \left( \frac{kb1}{J1} \cdot IT1effCD(L1, m, f) + \frac{kb2}{J2 \cdot m} \cdot IdeffCD(L1, m, f) \right) \end{cases}$$

### Capacitor Current

$$Icapaeff(L1, m, f) := \begin{cases} IcapaeffCC(L1, m, f) & \text{if } L1 > L1lin(m, f) \\ IcapaeffCD(L1, m, f) & \text{otherwise} \end{cases}$$

$$IcapaeffCC(L1, m, f) := \begin{cases} L2 \leftarrow \frac{L1}{m^2} \\ \alpha \leftarrow \sqrt{\frac{2 \cdot L1 \cdot f \cdot V_s \cdot L2}{V_e^2}} \\ T \leftarrow \frac{1}{f} \\ IL2max \leftarrow m \cdot \left( \frac{V_e}{L1} \cdot \alpha \cdot T \right) \\ \beta \leftarrow \alpha \cdot \left( \frac{V_e}{V_{sm}} + 1 \right) \\ \frac{1}{3} \cdot \left( \frac{6 \beta^2 T V_s \alpha IL2max L2 + 3 \beta^2 IL2max L2^2 - V_s^2 \alpha^3 T^2 + \beta^3 T^2 V_s^2 - 3 \beta^2 T V_s IL2max L2 + 3 \beta^2 T^2 V_s^2 \alpha^2 - 3 \beta^2 T^2 V_s^2 \alpha - 6 \beta IL2max L2^2 I2 + 3 \beta^2 T V_s IL2 L2 - 6 \beta T V_s \alpha IL2 L2 + 3 IL2^2 L2^2 + 6 \alpha IL2max L2^2 I2 - 3 \alpha IL2max L2^2 + 3 V_s \alpha^2 T IL2 L2 - 3 V_s \alpha^2 T IL2max L2}{L2^2} \right)^{\frac{1}{2}} \end{cases}$$

$$IcapaeffCD(L1, m, f) := \begin{cases} L2 \leftarrow \frac{L1}{m^2} \\ \alpha \leftarrow \frac{V_{sm}}{V_{sm} + V_e} \\ T \leftarrow \frac{1}{f} \\ \Delta i \leftarrow \frac{V_e}{L1} \cdot \alpha \cdot T \\ IL2max \leftarrow m \cdot \left( \frac{P}{V_e \alpha} + \frac{1}{2} \cdot \Delta i \right) \\ IL2min \leftarrow \left( \frac{P}{V_e \alpha} - \frac{1}{2} \cdot \Delta i \right) \cdot m \\ \frac{1}{3} \cdot \left( \frac{-[V_s^2 \alpha^3 T^2 - 3 V_s^2 \alpha^2 T^2 - 3 T V_s IL2 L2 + 3 T V_s IL2max L2 - 3 IL2^2 L2^2 - 3 IL2max L2^2 + 6 IL2max L2^2 I2 + 6 V_s \alpha T IL2 L2 - T^2 V_s^2 + 3 T^2 V_s^2 \alpha - 6 \alpha IL2max L2^2 I2 + 3 \alpha IL2max L2^2 - 3 V_s \alpha^2 T IL2 L2 + 3 V_s \alpha^2 T IL2max L2 - 6 V_s \alpha T IL2max L2]}{L2^2} \right)^{\frac{1}{2}} \end{cases}$$

## Diode Current

$$\text{Ieff}(L1, m, f) := \begin{cases} \text{IeffCC}(L1, m, f) & \text{if } L1 > L1_{\text{lin}}(m, f) \\ \text{IeffCD}(L1, m, f) & \text{otherwise} \end{cases}$$

$$\begin{aligned} \text{IeffCC}(L1, m, f) &:= \begin{aligned} &L2 \leftarrow \frac{L1}{m^2} \\ &\alpha \leftarrow V_s \cdot \frac{m}{V_s \cdot m + V_e} \\ &T \leftarrow \frac{1}{f} \\ &\Delta i \leftarrow \frac{V_e}{L1} \cdot \alpha \cdot T \\ &IL2_{\text{max}} \leftarrow m \left( \frac{P}{V_e \cdot \alpha} + \frac{1}{2} \cdot \Delta i \right) \\ &IL2_{\text{min}} \leftarrow \left( \frac{P}{V_e \cdot \alpha} - \frac{1}{2} \cdot \Delta i \right) \cdot m \\ &\frac{1}{3} \cdot 3^2 \cdot \left[ \frac{(-1 + \alpha) \cdot \frac{V_s^2 \cdot \alpha^2 \cdot T^2 - 2 \cdot T^2 \cdot V_s^2 \cdot \alpha + 3 \cdot V_s \cdot \alpha \cdot T \cdot IL2_{\text{max}} L2 - 3 \cdot T \cdot V_s \cdot IL2_{\text{max}} L2 + T^2 \cdot V_s^2 + 3 \cdot IL2_{\text{max}}^2 \cdot L2^2}{L2^2}} \right]^2 \end{aligned} \\ \text{IeffCD}(L1, m, f) &:= \begin{aligned} &L2 \leftarrow \frac{L1}{m^2} \\ &\alpha \leftarrow \sqrt{\frac{2 \cdot L1 \cdot f \cdot V_s \cdot IL2}{V_e^2}} \\ &T \leftarrow \frac{1}{f} \\ &IL2_{\text{max}} \leftarrow m \left( \frac{V_e}{L1} \cdot \alpha \cdot T \right) \\ &\beta \leftarrow \alpha \cdot \left( \frac{V_e}{V_s \cdot m} + 1 \right) \\ &\frac{1}{3} \cdot 3^2 \cdot \left( \frac{\beta^3 \cdot T^2 \cdot V_s^2 - 3 \cdot \beta^2 \cdot T^2 \cdot V_s^2 \cdot \alpha - 3 \cdot \beta^2 \cdot T \cdot V_s \cdot IL2_{\text{max}} L2 + 3 \cdot \beta \cdot T^2 \cdot V_s^2 \cdot \alpha^2 + 6 \cdot \beta \cdot T \cdot V_s \cdot \alpha \cdot IL2_{\text{max}} L2 + 3 \cdot \beta \cdot IL2_{\text{max}}^2 \cdot L2^2 - V_s^2 \cdot \alpha^3 \cdot T^2 - 3 \cdot V_s \cdot \alpha^2 \cdot T \cdot IL2_{\text{max}} L2 - 3 \cdot \alpha \cdot IL2_{\text{max}}^2 \cdot L2^2}{L2^2} \right)^2 \end{aligned} \end{aligned}$$

## MOSFET Current

$$\text{IT1eff}(L1, m, f) := \begin{cases} \text{IT1effCC}(L1, m, f) & \text{if } L1 > L1_{\text{lin}}(m, f) \\ \text{IT1effCD}(L1, m, f) & \text{otherwise} \end{cases}$$

$$\begin{aligned} \text{IT1effCC}(L1, m, f) &:= \begin{aligned} &L2 \leftarrow \frac{L1}{m^2} \\ &\alpha \leftarrow V_s \cdot \frac{m}{(V_s \cdot m) + V_e} \\ &T \leftarrow \frac{1}{f} \\ &\Delta i \leftarrow \frac{V_e}{L1} \cdot \alpha \cdot T \\ &IL1_{\text{min}} \leftarrow \frac{P}{V_e \cdot \alpha} - \frac{1}{2} \cdot \Delta i \\ &\frac{1}{3} \cdot 3^2 \cdot \left( \alpha \cdot \frac{T^2 \cdot \alpha^2 \cdot V_e^2 + 3 \cdot T \cdot \alpha \cdot V_e \cdot IL1_{\text{min}} L1 + 3 \cdot IL1_{\text{min}}^2 \cdot L1^2}{L1^2} \right)^{\frac{1}{2}} \end{aligned} \\ \text{IT1effCD}(L1, m, f) &:= \begin{aligned} &L2 \leftarrow \frac{L1}{m^2} \\ &\alpha \leftarrow \sqrt{\frac{2 \cdot L1 \cdot f \cdot V_s \cdot IL2}{V_e^2}} \\ &T \leftarrow \frac{1}{f} \\ &IL2_{\text{max}} \leftarrow m \left( \frac{V_e}{L1} \cdot \alpha \cdot T \right) \\ &\frac{1}{3} \cdot 3^2 \cdot \left( T^2 \cdot \alpha^3 \cdot \frac{V_e^2}{L1^2} \right)^{\frac{1}{2}} \end{aligned} \end{aligned}$$