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Low frequency noise in InAlAs/InGaAs modulation doped field effect transistors with 50-nm gate length

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We report on the low frequency [$1/f$ and generation-recombination (GR)] noise in InAlAs/InGaAs modulation doped field effect transistors with a 50-nm gate length. The characteristic capture and emission times of the GR noise depended on the gate voltage. Measurements of the noise as a function of the gate voltage showed that the gate leakage current, contacts, and ungated sections of the channel did not contribute to the $1/f$ noise. The gate voltage dependence of the $1/f$ noise agreed well with the model of number of carriers fluctuations as a source of the $1/f$ noise. An effective density of traps responsible for the $1/f$ noise was found to be $D_{\text{eff}} \approx 2.7 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$. © 2007 American Institute of Physics. [DOI: [10.1063/1.2781087](https://doi.org/10.1063/1.2781087)]

I. INTRODUCTION

InAlAs/InGaAs high electron mobility field effect transistors (HEMTs) or modulation doped field effect transistors (MODFETs) have demonstrated superior performance as high frequency oscillators, mixers, and amplifiers. InAlAs/InGaAs HEMTs with the gate length L_g of $\sim 50 \text{ nm}$ can be used as submillimeter low noise amplifiers and generators with the cutoff frequencies well above 200 GHz.^{1,2} In the regime of the plasma waves excitation, InAlAs/InGaAs HEMTs with deep submicron gates can be used as oscillators and tunable detectors in the terahertz frequency range.³⁻⁵ One of the key parameters for such microwave and terahertz devices is the level of the low-frequency noise.

In nonlinear circuits, the low frequency fluctuations are up-converted into microwave noise close to the carrier frequency and determine the phase noise characteristics of oscillators, mixers, and amplifiers. Low frequency noise measurements are also a powerful tool to study impurities and defects in semiconductor structures and to diagnose quality and reliability of semiconductor devices. That is the reason why the low frequency noise in InGaAs-based MODFETs has been extensively studied.⁶⁻¹⁴ Nevertheless, the understanding of the noise mechanisms is incomplete.

Both $1/f$ and generation-recombination (GR) noise¹²⁻¹⁴ were observed in InGaAs-based MODFETs. Measurements of the temperature dependence of the GR noise allowed finding the activation energy of traps responsible for the GR noise.^{11,12} Gate leakage current was found to contribute to the output low frequency drain current noise in some cases.¹⁰

In certain devices, the gate voltage dependence of the $1/f$ noise is well described by the model suggested in Ref. 15 and based on empirical Hooge relation¹⁶

$$\frac{S_R}{R^2} = \frac{\alpha}{fN}, \quad (1)$$

where S_R/R^2 is the relative spectral density of the $1/f$ noise in “semiconductor resistor,” N is the total number of the carriers in the resistor, R is the resistance, f is the frequency, and α is the Hooge parameter, which varies for different semiconductor objects within the range $10^{-7} - 10^{-1}$.

However, experiments reported in Refs. 7, 9, and 11 revealed essential deviations from the predictions of the model developed in Ref. 15. Attempts to improve the agreement between the experiments and the theory by accounting for the dependence of the mobility on the gate voltage in the gated HEMT channel^{9,17} did not lead to the satisfactory agreement in the framework of the model.¹⁵

In many cases, the $1/f$ noise originates from GR noise sources with characteristic times τ distributed in a very wide frequency range (see, for example, Refs. 17–19, and references therein). In these cases, the relative spectral density of noise is inversely proportional to $1/N^2$ rather than to $1/N$, as in Eq. (1).

In this article, we report on experimental studies of the low frequency ($1/f$ and GR) noise in InAlAs/InGaAs HEMTs with 50-nm gate length. The obtained results are interpreted using the model linking the observed noise with fluctuations of carriers number in the channel.

II. EXPERIMENTAL DETAILS

Schematic of cross-sectional view of a structure under study is shown in Fig. 1. The InAlAs/InGaAs heterostructure

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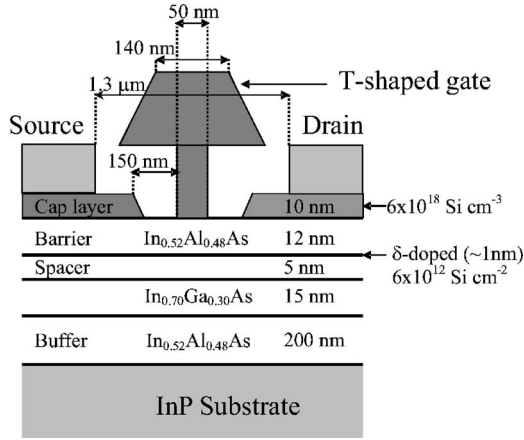


FIG. 1. Cross-sectional view of the structure under study.

was grown by molecular beam epitaxy on a semi-insulating InP substrate. The structure consists of a 200-nm-thick In_{0.52}Al_{0.48}As buffer layer, 15-nm-thick undoped In_{0.7}Ga_{0.3}As pseudomorphic channel layer, followed by 5-nm-thick In_{0.52}Al_{0.48}As spacer, δ -doped layer (Si, $6 \times 10^{12} \text{ cm}^{-2}$), 12-nm-thick In_{0.52}Al_{0.48}As barrier layer, and 10-nm-thick In_{0.52}Al_{0.48}As cap layer doped to $6 \times 10^{18} \text{ cm}^{-3}$ (Si).

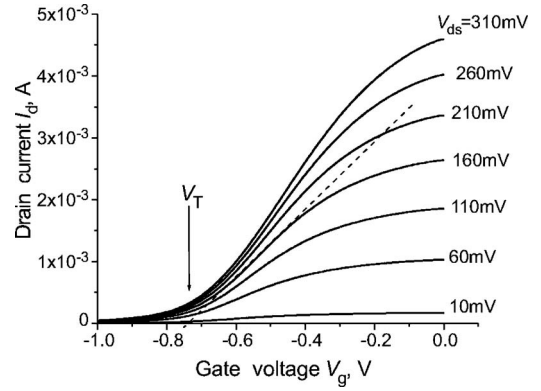
The main steps of the devices fabrication process were as follows. First, the ohmic contacts metallization (Ni/Ge/Au/Ni/Au) was evaporated and annealed. Then the devices were isolated by wet mesa etching using phosphoric acid solution. A thin 60-nm silicon nitride (Si₃N₄) layer was deposited at low temperature to preserve the quality of ohmic contacts. This layer was used both to form the gate footprint and to passivate the devices. The gate footprint was fabricated using the high resolution poly(methylmethacrylate) resist insulated by LEICA EBP5000+ lithography machine followed by dry CHF₃/CF₄ plasma etching of silicon nitride to form the footprint of the gate. Then the top of the T gate was defined by electron-beam lithography. The final step was a wet recess with selective succinic acid solution and Ti/Pt/Au gate metallization. The gate length L_g is 50 nm (see Fig. 1). For our measurements we used devices with the gate width $W=20 \text{ } \mu\text{m}$. The devices were mounted in the ceramic packages.

The Hall measurements yielded the electron concentrations under the cap layer of approximately $\sim 5.5 \times 10^{12} \text{ cm}^{-2}$ and in the part of the channel which is not covered by the cap layer (Fig. 1) of about $3.5 \times 10^{12} \text{ cm}^{-2}$. Electron Hall mobility in large samples was within the range 11 000–12 200 $\text{cm}^2/\text{V s}$.

The low-frequency noise was measured on the packaged transistors in the frequency range from 1 Hz to 50 kHz at 300 K with the source grounded. The voltage fluctuations S_V from the load resistor $R_L=100 \text{ } \Omega$ connected in series with the drain were analyzed by a SR770 network analyzer. The spectral noise density of the short circuit drain current fluctuations, S_I , was calculated as $S_I = S_V[(R_L + R_d)/(R_L R_d)]^2$, where R_d is the drain-to-source differential resistance.

III. RESULTS AND DISCUSSION

The threshold voltage V_T found from the transfer current-voltage characteristics $I_d(V_g)$ measured in linear re-

FIG. 2. Transfer drain current-gate voltage, $I_d(V_g)$, characteristics.

gime was within the range -0.55 to -0.8 V for different devices. Figure 2 shows an example of the transfer characteristics for the transistor with $V_T \approx -0.78 \text{ V}$. Below the threshold voltage, the $I_d(V_g)$ dependences followed a conventional law $I_d \sim \exp(qV_g/\eta kT)$ with ideality factor $\eta=3.8-5.2$ (k is the Boltzmann constant, T is the temperature, and q is the elemental charge).

The electron concentration under the gate, n_s , can be approximated by the relation

$$n_s \approx \frac{(V_g - V_T)C_g}{q}, \quad (2)$$

where $C_g = \epsilon\epsilon_0/(d + \Delta d)$ is the gate capacitance per unit area ($C_g \approx 5.1 \times 10^{-3} \text{ F/m}^2$), d is the distance from gate to channel, Δd is the effective half-thickness of the two-dimensional electron gas ($\sim 4 \text{ nm}$),²⁰ ϵ is the dielectric constant of In_{0.52}Al_{0.48}As [$\epsilon=12.7$ is a linear approximation between $\epsilon=15.15$ (InAs) and $\epsilon=10.06$ (AlAs)],²¹ and ϵ_0 is the permittivity of free space. For the transistor with $V_T \approx -0.78 \text{ V}$ and $d=18 \text{ nm}$ (see Fig. 1), the concentration n_s at zero gate bias was found to be $n_s(V_g=0) \approx 2.5 \times 10^{12} \text{ cm}^{-2}$. Thus, the electron concentration under the gate at zero bias is smaller than the concentration obtained from the Hall measurements on the wafer for the ungated part of the channel which is not covered by cap layer ($3.5 \times 10^{12} \text{ cm}^{-2}$).

In order to find the access resistance, which is the sum of the contact resistance and resistance of the ungated parts of the channel, we plotted the total source-drain resistance R_{ds} as a function of the $(V_g - V_T)^{-1}$. This crude estimate yielded values of the access resistance within the range from 46 to 90 Ω for different devices. The resistance of the gated part of the channel was $R_c < 10-20 \text{ } \Omega$.

The estimate for the mobility from the channel resistance yields $\mu = L_g/(WR_c q n_s) \geq 650 \text{ cm}^2/\text{V s}$, which is at least one order of magnitude smaller than the Hall mobility. In short channel devices the electron mobility is limited by the electron transit time due to ballistic effects.²² In a degenerate case this time is L_g/v_F , where $v_F = (2E_F/m^*)^{1/2}$ is the Fermi velocity, E_F is the Fermi energy, and m^* is the electron effective mass. As shown in Ref. 22, a ballistic transistor mobility is given by $\mu = (2qL_g)/(\pi m^* v_F)$. Taking for Fermi energy in two-dimensional degenerate case $E_F = \pi \hbar^2 n_s / m^*$ we

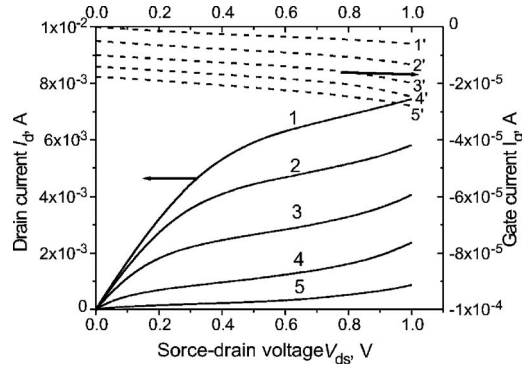


FIG. 3. Output current-voltage characteristics $I_d(V_{ds})$ (solid lines) and dependencies of the gate leakage current on source-drain voltage (dashed lines) at different gate voltages V_g (V): 1, 1'=0; 2, 3'=-0.2; 3, 3'=-0.4; 4, 4'=-0.6; 5, 5'=-0.8.

obtained $\mu \approx 1000 \text{ cm}^2/\text{V s}$, which is of the same order of magnitude as the mobility estimated from the resistance value.

Figure 3 represents static current-voltage characteristics for one of the devices. Solid lines represent the output current-voltage characteristics $I_d(V_{ds})$ at different values of V_g . Dashed lines show the dependences of gate leakage current, I_g , on source-drain voltage V_{ds} at different gate voltages V_g . An increase of the drain current at high drain voltage $>0.8\text{--}0.9 \text{ V}$ might be related to the electron impact ionization in the channel. As known, this effect leads to the increase of the high frequency noise at corresponding voltages.²³ However, this mode of operation and the high frequency noise were out of the scope of our study.

As seen, at low drain voltage $V_{ds} \leq 0.1 \text{ V}$ and at large negative gate bias (curves 4, 4' and 5, 5'), the I_g/I_d ratio is relatively high, approximately $10^{-2}\text{--}10^{-1}$. This high gate leakage current can potentially contribute to the low frequency drain current noise (see, for example, Refs. 10, 24, and 25). However, as it will be shown later, in the structures under study, the contribution of the gate leakage current noise to the total noise is negligible.

Figure 4 shows the noise spectra of short circuit drain current fluctuations, S_I , measured on linear part of output current-voltage characteristics $I_d(V_{ds})$ ($V_{ds}=50 \text{ mV}$) at differ-

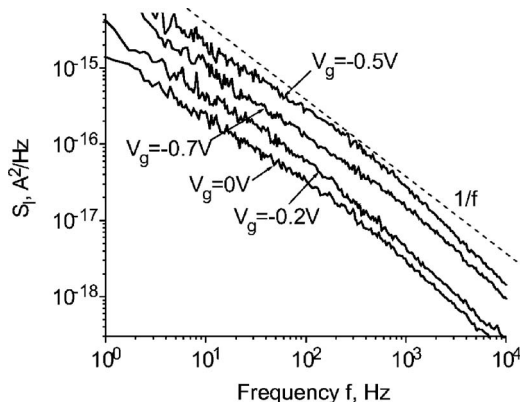


FIG. 4. Frequency dependencies of short circuit drain current fluctuations, S_I , in linear regime ($V_{ds}=50 \text{ mV}$) at different gate voltages V_g . The dashed line shows the $1/f$ slope.

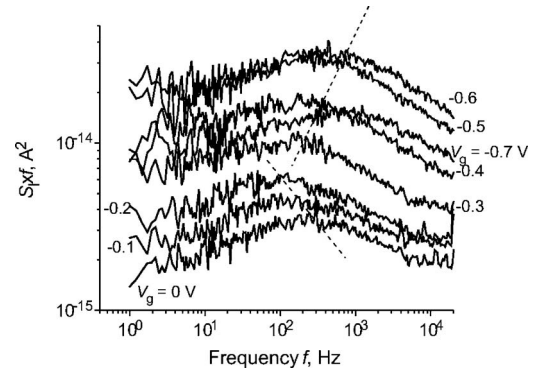


FIG. 5. Frequency dependencies of $S(f)f$ measured in linear regime ($V_{ds}=50 \text{ mV}$) at different gate voltages V_g . The dashed lines show the direction of the shift of maxima with V_g changing.

ent gate voltages, V_g . At $V_{ds}=50 \text{ mV}$, the $I_d(V_{ds})$ characteristics are linear even at large negative (subthreshold) V_g values $|V_g| > |V_T|$ (see Ref. 26, for example, for the subthreshold characteristics of the transistors).

As seen, S_I depends on V_g nonmonotonically, with the gate voltage decrease S_I grows at first, reaches its maximum, and decreases with further decrease in V_g . The shape of the noise spectra can be characterized as “ $1/f$ -like” with deviations, which can be attributed to the GR noise. (GR noise has been observed in InGaAs,^{12–14} AlGaAs,^{27,28} and AlGaN-based²⁹ HEMTs.)

The procedure of GR noise extraction from $1/f$ -like noise spectra can be simplified by plotting $S(f)f$ versus frequency dependences. In these coordinates, the GR noise reveals itself as maxima on the flat background of the $1/f$ noise. Figure 5 shows the frequency dependencies of $S(f)f$ measured in linear regime ($V_{ds}=50 \text{ mV}$) at different gate voltages V_g .

The contribution from GR noise is clearly seen in Fig. 5 on all spectra at any values of V_g . Similar dependences were observed for all other transistors measured. The characteristic time constant of the GR noise associated with return to equilibrium of the occupancy of noisy level is $\tau = 1/2\pi f_{\text{max}}$, where f_{max} is frequency of the maxima in Fig. 5. The time constant τ is determined by the capture $\tau_c = 1/\sigma v_F N_c$ and emission $\tau_e = \exp[E_a/kT]/\sigma v_F N_c$ times as $\tau^{-1} = \tau_c^{-1} + \tau_e^{-1}$ (see Ref. 30, for example). Here E_a is the activation energy, σ is the electron capture cross section, and N_c is the effective density of states in the conduction band. As seen in Fig. 5, f_{max} , and therefore τ , depend nonmonotonically on the gate voltage. While transistors differed in the amplitude of the GR noise and absolute values of τ , all of them demonstrated similar dependences of the time constant τ on the gate voltage.

An increase of τ with the gate voltage increase at small V_g values can be explained by the dominance of the emission time and dependence of the activation energy E_a on the gate voltage. Further decrease of τ at high V_g indicates predominance of the capture time and its decrease with increase of the concentration in the channel. Similar dependences of the emission and capture times as the functions of the gate volt-

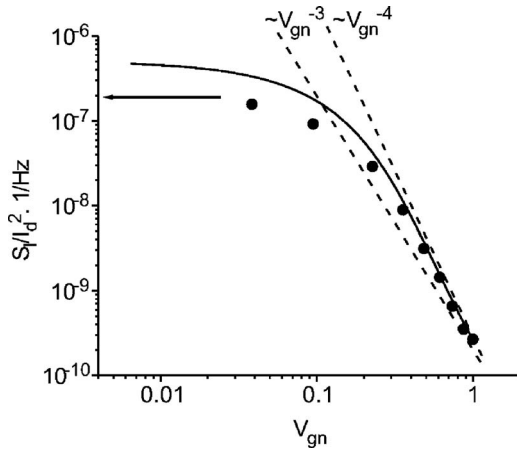


FIG. 6. The relative spectral noise density on the normalized gate voltage $V_{gn} = (V_g - V_T)/|V_T|$ in linear regime ($V_{ds} = 50$ mV). Frequency of analysis $f = 10$ Hz. An arrow shows the noise level measured below the threshold voltage. The dashed lines show the slopes $S_I/I_d^2 \propto V_{gn}^{-3}$ and $S_I/I_d^2 \propto V_{gn}^{-4}$. The solid line is calculated according to Eqs. (4) and (5) using experimental V_T , R_c , R_{ac} values. D_{eff} has been used as fitting parameter.

age were observed while studying random telegraph noise in Si metal–oxide–semiconductor field effect transistors (MOSFETs).³¹

Experimental points in Fig. 6 represent the dependence of the current relative spectral noise density S_I/I_d^2 versus normalized gate voltage $V_{gn} = (V_g - V_T)/|V_T|$ for one of the structures in question at frequency of analysis $f = 10$ Hz. Such dependencies are used very often to discuss and analyze the peculiarities of the $1/f$ noise in MODFETs.^{9,11,15,32}

In short channel HEMTs with the high ratio L_c/L_g , (L_c is the channel length), the spectral noise density S_I/I_d^2 is often independent or weakly dependent on the gate voltage at voltages close to zero gate bias.^{9,15,32} That is because the resistance of the gated part of the channel at $V_g \approx 0$ ($V_{gn} \approx 1$) is only a small fraction of the total drain to source resistance and noise is mainly determined by the ungated part of the channel and the contacts. However, in the transistors under investigation ($R_{ds}/R_c \approx 5$ at $V_g = 0$) the flat part of the noise versus gate voltage dependence was absent for the gate voltage close zero (see Fig. 6). Therefore, in spite of the large access resistance, its contribution to the noise is small in comparison to the noise originated from the gated part of the channel.

Let us estimate the Hooge parameter for the gated part of the channel at $V_g = 0$. Neglecting the contribution to noise from the access resistance and feedback due to the source part of the access resistance (transconductance is very small at small V_{ds}) the spectral noise density of the R_c resistance fluctuations can be written as

$$\frac{S_{R_c}}{R_c^2} = \frac{\alpha_{g0}}{fN_g} = \frac{S_I(R_c + R_{ac})^2}{I_d^2 R_c^2}. \quad (3)$$

With $L_g = 50$ nm, gate width $W = 20$ μm , and $n_s(V_g = 0) \approx 2.5 \times 10^{12}$ cm^{-2} , the total number of electrons in the gated part of the structure is $N_g \approx 2.5 \times 10^4$. Taking $S_I/I_d^2 \approx 2 \times 10^{-10}$ at $f = 10$ Hz, $R_{ac} \approx 46$ Ω , and $R_c \approx 10$ Ω , we have $\alpha_{g0} \approx 1.3 \times 10^{-3}$. The values of the Hooge parameter of the same order of magnitude or smaller have been reported for

many different kinds of HEMTs, (see Refs. 6 and 13 for InAlAs/InGaAs, Ref. 33 for GaAs/AlGaAs, and Ref. 34 for GaN/AlGaN HFETs).

With the gate voltage decrease, the S_I/I_d^2 increases approximately as $S_I/I_d^2 \propto V_{gn}^{-4}$ (Fig. 6). Meantime, the steepest decrease of S_I/I_d^2 predicted by Eq. (3) in the framework of the model,¹⁵ i.e., assuming α_g independent on the gate voltage is only $S_I/I_d^2 \propto V_{gn}^{-3}$.

On the other hand, in accordance with the McWhorter model (see, for example, Ref. 17)

$$\frac{S_{R_c}}{R_c^2} = \frac{kTD_{eff}}{fL_g W n_s^2 \ln(\tau_{max}/\tau_{min})}, \quad (4)$$

where D_{eff} is the effective trap density on the Fermi level, $n_s(V_g)$ is the electron concentration in the gated part of the channel, and τ_{max} and τ_{min} are the maximum and minimum tunneling times.

Electron concentration in the channel is given as (see Ref. 26, for example)

$$n(V_g) = \frac{C_g \eta k T}{q^2} \ln \left\{ 1 + \exp \left[\frac{q(V_g - V_T)}{\eta k T} \right] \right\}. \quad (5)$$

Equation (5) describes the gate voltage dependence of concentration both below and above the threshold voltage V_T . Well above the threshold voltage it reduces to Eq. (2).

Solid line in Fig. 6 was calculated using Eqs. (4) and (5) with $\ln(\tau_{max}/\tau_{min}) = 4$ and $D_{eff} = 2.7 \times 10^{12}$ cm^{-2} eV^{-1} . The influence of the access resistance was taken into account as

$$\frac{S_I}{I_d^2} = \frac{S_{R_c}}{R_c^2} \frac{R_c^2}{(R_c + R_{ac})^2}. \quad (6)$$

As seen, the calculated curve describes well experimental results over the entire range of V_{gn} . In particular, the experimentally found slope $S_I/I_d^2 \propto V_{gn}^{-4}$ at large V_{gn} values is well reproduced in the framework of this approach.

Equation (4) is often used to analyze the $1/f$ noise in Si MOSFETs. In that case D_{eff} is the effective density of the traps into SiO_2 under the gate. In case of the InGaAs MODFETs, traps can be located either on the quantum well interface¹⁰ or in adjacent InAlAs layers (see Fig. 1).^{19,34} The D_{eff} taken for the calculations is directly affected by the $\ln(\tau_{max}/\tau_{min})$ value. For crude estimate we assumed $\ln(\tau_{max}/\tau_{min}) = 4$ as suggested in Ref. 36. The obtained D_{eff} value ($2.7 \times 10^{12} - 1 \times 10^{13}$) cm^{-2} eV^{-1} is about one order of magnitude higher than those reported for InAlAs/InGaAs MODFETs with the very long gates of $L_g = (10 - 100)$ μm .¹⁰ The effective trap density usually increases with gate length decrease for $L_g < 1$ μm (see Refs. 10 for InAlAs/InGaAs MODFETs and Ref. 36 for Si MOSFETs). A crude extrapolation of the data from Refs. 10 and 35 to the gate length of 50 nm yields the value of D_{eff} of the same order of magnitude as obtained here or even higher.

Close to the threshold voltage, the experimental and calculated curves tend to saturate. This saturation indicates that the gate leakage current does not contribute much to the total output noise. Indeed, with the gate voltage decrease the drain current also decreases but the gate current increases. Therefore, if the gate current contribution to the output noise were

dominant the spectral noise density S_I/I_d^2 should have gone up with decrease of V_{gn} . Since this trend is not observed, we conclude that the gate current contribution to the drain current noise is negligible.

Using Eq. (4) one assumes that the fluctuation in number of trapped electrons, δN_t , and the fluctuation of the number of free electrons in the channel δN are equal, i.e., $|\delta N/\delta N_t| = 1$. However, as shown in Ref. 37, this assumption is correct only in a strong inversion regime (large n_s values). Close to the threshold voltage and below, the ratio $\delta N/\delta N_t$ is reduced. That might be the reason why experimentally measured noise is smaller at $V_{gn} \ll 1$ in Fig. 6, than those calculated using Eq. (4).

IV. CONCLUSION

The low frequency $1/f$ and generation-recombination noise were studied in InAlAs/InGaAs MODFETs with 50-nm gate length. The characteristic time of the GR noise nonmonotonically depends on the gate voltage. This behavior indicates that emission and capture times are dominant at different gate voltages.

Even at high negative gate voltage and small drain bias (under condition when gate leakage and drain currents are comparable) the gate current does not contribute much to the output drain current noise. In spite of the high access resistance in comparison with the resistance of the gated part of the channel, the access resistance also does not contribute to the overall noise. Hence, the contact noise and the noise originated from the ungated parts of the channel are small. Both, well above the threshold voltage and close to the threshold, the gate voltage dependence of noise complies very well with the model of number of carriers fluctuations as a source of the $1/f$ noise.

An effective density of trap $D_{eff} \approx 2.7 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ estimated from the $1/f$ noise amplitude is relatively high in comparison with the longer gate Si MOSFETs.

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