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# Wafer Level Package for Image Sensor Module

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***Abstract-*** **A new ISM (image sensor module) WLP (wafer level package) for reflow process is designed, fabricated and tested. The ISM WLP is composed of polymer bonding layer, glass cap wafer for particle free process and CIS (CMOS Image Sensor) chip wafer which has micro via hole interconnection. During the last decades, WLP is highlighted as the next generation ISM Package method for many advantages like high yield (particle free process), small form factor (3D interconnection), low assembly cost and so on. Nevertheless these benefits, there are some problems like micro via hole fabrication, low temperature insulation process (inside hole), bottom side oxide etching, warpage control according to wafer level bonding using different material, and whole process temperature limitation for micro lens damage. Among various fabrication methods for ISM package, COB (Chip on board), COF (Chip on film), and L, T contact WLP from ShellCase are generally used. In case of COB and COF package, it has difficulty in particle control during assembly process. In case of ShellCase type WLP has very complicated fabrication process. Additionally, most of above package has disadvantage in size point of view. Through suggested ISM WLP using through interconnection via, wafer level fabrication & packaging technology is realized. It can not only solve problems of conventional packaging structures but also tremendously reduce the manufacturing & assembly cost (include time) of ISM package and realize real chip scale package. Based on sensor size, 3.67 X 3.42 X 0.39 (H) mm3 WLP is designed. During the parametric study using commercial 3-D simulation programs, silicon thickness, polymer bonding layer thickness, and glass thickness were chose the effective factor. And considering the optical and electrical analysis, we decide the parameter: silicon thickness is 0.1mm, polymer bonding layer thickness is 0.04mm, and glass thickness is 0.25mm. The fabrication process is composed bonding layer patterning, wafer bonding, thinning, via etching, passivation layer deposition, bottom oxide opening, metal plating, bottom electrode patterning, solder ball formation, and dicing. A new concept of ISM WLP has been founded to be suitable structure for low cost, small form factor application.**

## I. INTRODUCTION

Many researcher forecast mobile phone market will be increase 10 % annual average growth between 2007 to 2010. These predictions are based on two fundamental trends. First, the growth of BRICs (BRICs means Brazil, Russia, Indonesia, and China) market has been most visible, in worldwide phone sales growing. This trend requests cost effective mobile phone, including ISM (low-end market). Second, the move to 3G will be make new high end market. This trend requests additional low grade ISM. According to these reasons, there were needs which is low cost, small size, low grade (like VGA) ISM. To satisfy these needs, there were many packages are developed. These include COB (Chip on board), COF (chip on film), and WLCSP (like shallcase type). [1-3] In spite of these efforts, there are many limitations in cost and size point of view. In this paper we have developed a fabrication technology of WLP for ISM, using the polymer based wafer bonding, through via hole interconnections from the backside of the Si substrate to the electrical pad. This package consists of a glass cap wafer for protecting an image sensing area from particle during fabrication process, adhesive bonding layer for low temperature wafer bonding, 3-D interconnections for real chip scale package, metal re-routing and solder bumps on the backside for reflow process. All processes of the packaging were done at wafer level. This paper describes the optimal package design, fabrication process, and evaluation results for ISM. Using this package, we can satisfy most of market requirements like user assembly cost reduction (reflowable package), chip scale package (through via interconnection method), increasing manufacturing efficiency (particle free process).

## II. DESIGN

### A. *Basic Concept of Package.*

Fig. 1 shows the basic concept of WLP for ISM. The package is consisted of glass cap wafer, polymer bonding layer, and CIS wafer which has through interconnection via.

The glass cap wafer has a function which is not only window for image processing, but also protection layer contamination during fabrication process. Adhesive polymer bonding layer is chosen for low temperature bonding. Because micro lens on active area are maintained under 200℃ in all fabrication steps. WLP must be cost effective and ultra small package. Under these constructions, we chose proper methods and optimized each process steps to achieve a low-cost and high-density WLP. Through via interconnection is chosen for chip scale package, ultra small package, and solder ball is attached for reflowable package. This reflowable package can eliminate additional interconnection cost between chips to board.

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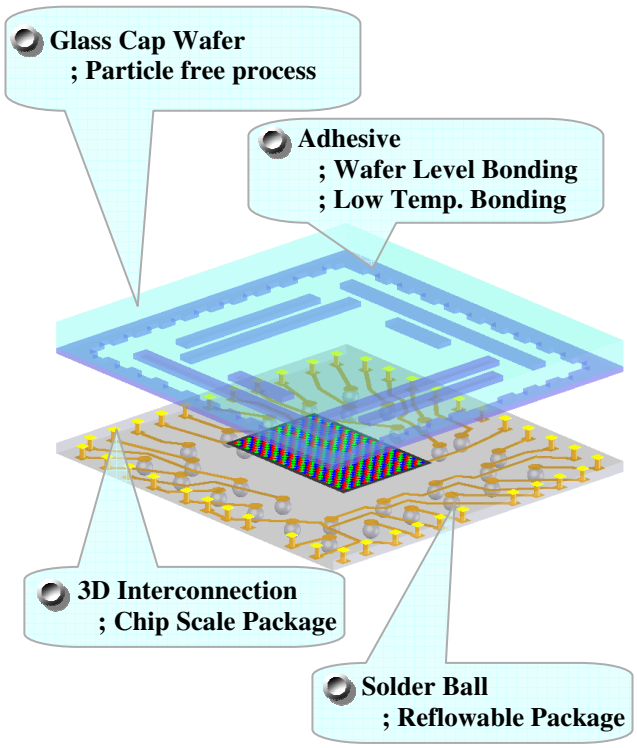



Fig. 1. Schematic Diagram of WLP for ISM.

*B. Simulation.*

We predict warpage, stress distribution and shear stress on the proposed package structure to figure out critical area on the package where can cause failure.

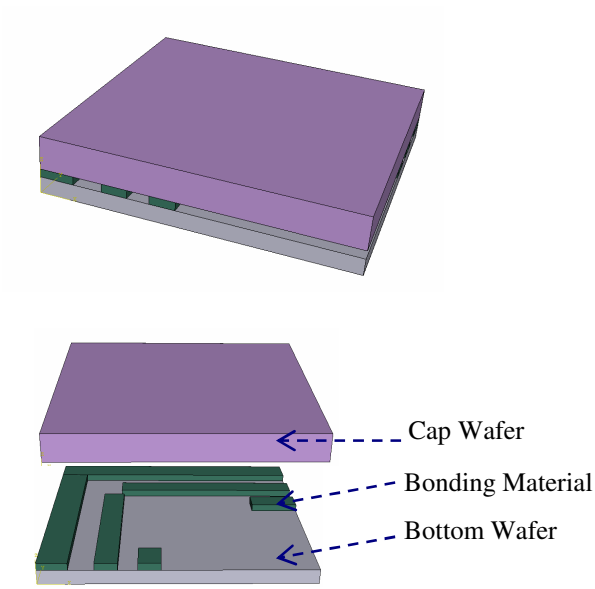



Fig. 2. Geometry structures of the Reflowable ISM WLP.

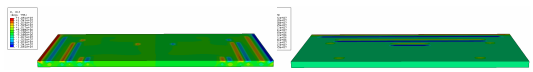
TABLE I
Material property

| Material Name | Young's Modulus (GPa) | CTE (ppm/K) | Poisson's ratio | Tg (ºC) |
|---|---|---|---|---|
| Pyrex.7740 | 63 | 3.25 | 0.2 | |
| Adhesive film | 3.3 (25 ºC) | 69<br>88 | 0.34 | 74 |
| Silicon | 130 | 2.6 | 0.27 | |

Warpage of package closes zero due to the similar CTE values between top wafer and bottom wafer. Bonding material is more critical factor due to the high CTE. CTE mismatch can be source of failure as delamination on the bonded area. Device wafer thickness slightly affects warpage and stresses on WLP ISM. Shear stress increase by bits due to the increase of device wafer thickness. We can fine these results in figure 3 & table 2.

(a) Warpage results at device wafer thickness 100um case

(b) Stress distribution at device wafer thickness 100um case



(c) Shear stress at device wafer thickness 100um case

Fig. 3. Simulation results at device wafer thickness 100um case.

TABLE II
Parametric study results.

| Device Wafer Thickness | Warpage | Max. Mises Stress | Max. Shear Stress |
|---|---|---|---|
| 75um | 2.49 um | 111.8 Mpa | 111.8 Mpa |
| 100um | 2.84 um | 112.2 Mpa | 112.2 Mpa |
| 125um | 2.58 um | 112.2 Mpa | 112.2 Mpa |
| 150um | 2.3 um | 112.1Mpa | 112.1Mpa |

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## III. FABRICATION

### A. *Process Overview*

The schematic fabrication process of the Reflowable ISM WLP is shown in Fig. 2. A 4-inch sized CMOS Image Sensor wafer was prepared with thickness of 525um. And a 4-inch pyrex glass wafer with thickness of 250um was used as the protective cap wafer for the package.

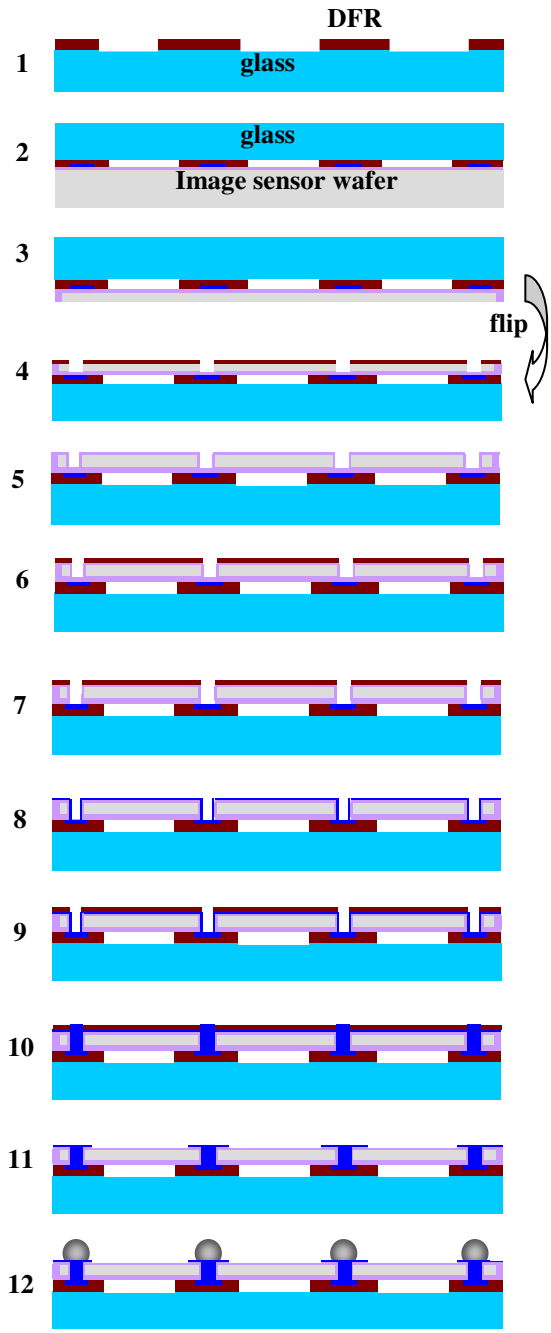


Fig. 4. Schematic fabrication process of the Reflowable ISM WLP.
1. DFR patterning. 2. Adhesive bonding. 3. Wafer thinning.
4. via etching. 5. passivation layer deposition. 6. DFR lamination.
7. passivation layer etch. 8. Seed layer deposition.
9. Mold for electroplating. 10. via filling by electroplating.
11. Seed layer etch. 12. Solder ball formation

The cap glass wafer was bonded with the image sensor wafer by adhesive bonding process. This adhesive bonding process is chosen because of low bonding temperature. A DFR (Dry Film Resist) layer was used as bonding material because of low cost and convenience of use. After the bonded wafer was thinned to the required thickness by conventional CMP process, backside vias were formed through the silicon wafer towards the Al pads of the image sensor. And an insulation film of SiO2 was deposited as the passivation layer on the wafer surface, as well as inside the vias. The passivation layer on surface of the Al pads was removed by etching process, and then electrical connection was established by forming conductive leads from Al pads to the backside of the wafer through the backside vias. Finally solder balls were formed on the backside of the wafer for reflow process.

## IV. PROCESS CONDITION AND EXPERIMENT RESULTS

For the packaging technology of image sensor, low-temperature processes are preferred for the protection of the sensor device and micro-lens. In this paper, all the process steps were performed at temperature lower than 150℃ except the solder ball reflow process. Key processes and experiment results are explained below in detail.

### A. *Bonding Process*

For the application of ISM WLP, choosing the cover layer whose role is protection of the image sensing area may be restricted to the glass wafer because of several requirements like transparency and durability. In this fabrication, polymer bonding method is adopted as the suitable technique to bond the glass wafer to the top side of the CIS wafer. The Vacrel, dry film resister (DFR) of DuPont, photosensitive adhesive material, is used as polymer bonding material.

A brief description of bonding process is followed. First of all, the DFR is laminated and patterned on the glass wafer, and then glass wafer with DFR pattern is bonded to CIS wafer through the high pressure and temperature. Due to the weakness in high temperature of CIS wafer which contain temperature sensitive material, the maximum bonding temperature is decided inherently as shown in figure 3 about 165℃. Figure 4 represents the result of polymer bonding. In case of bonding process, the strength of bonded area can be the indicator whether the quality of bonding is good or not. In this project, the shear strength is adopted as the index for deciding the quality of bonding results and 'Dage series 4000' equipment is used. As shown in Table 1, the shear strength of

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center portion and edge portion are different because of the non uniformity of bonding equipment. Even though there is differentiation in shear strength between center portion and edge portion, the shear strength of the weakest area, center portion, is around 26 MPa.

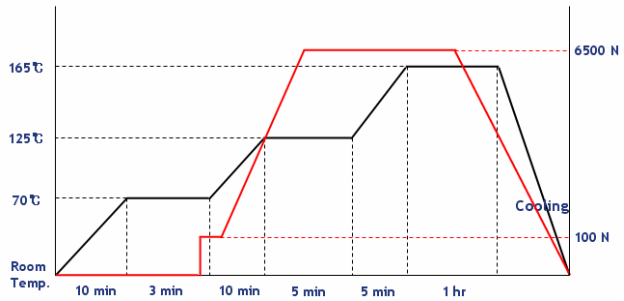



Fig. 5 the pressure and temperature profiles for polymer bonding in the ISM WLP process.

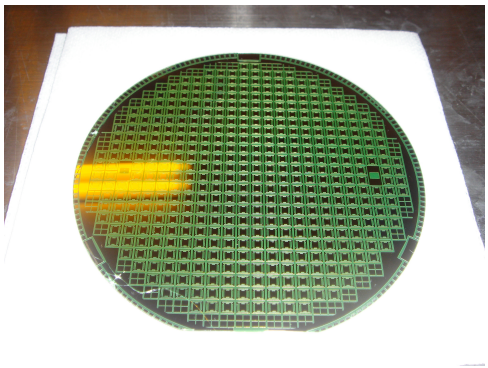


Fig. 6 the photograph of the result of polymer bonding

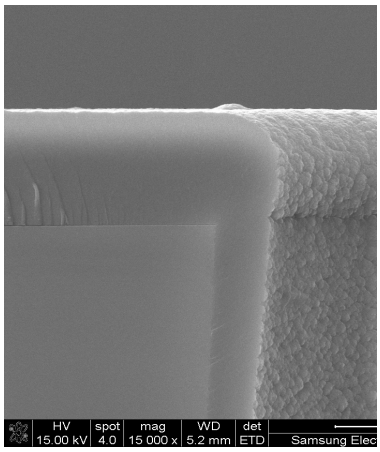
TABLE III
the shear strength of polymer bonding

| | Edge portion | | Center portion | |
|---|---|---|---|---|
| | Kgf | MPa | Kgf | MPa |
| Sum | 273.0 | 579.96 | 222.64 | 478.22 |
| Average | 17.06 | 36.25 | 12.37 | 26.57 |
| Standard Deviation | 1.64 | 3.84 | 1.28 | 2.76 |

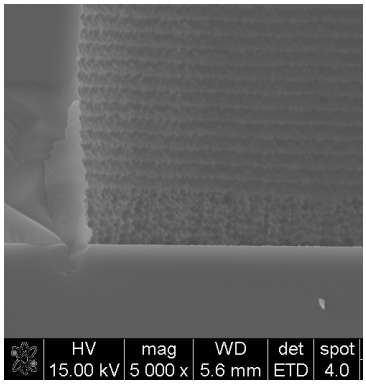
*B. Backside via etching.*

DRIE process was used to form vertical vias from the wafer backside surface to the insulation layer at the bottom of Al pads. Via diameter was 50um and aspect ratio was optimized as ~2.0 for an optimum balance of process capability requirement between via etch process and passivation layer deposition process. Process result is shown in figure 5.

In the DRIE process for the backside via, small scallop and notch were needed for sequent passivation process. So The DRIE process was optimized to get good sidewall surface smoothness, i.e. scallop, small notch effect on via bottom corner, and acceptable etch rate as well. Both HF(high frequency) and LF(low frequency) processes were used in the via etch step to get benefit of both good etch rate and notch-free process. Optimized scallop (<200nm) and notch (<1um) were achieved in this step to meet the process requirement of the passivation layer deposition process.




(a) Cross-sectional view of via




(b) Bottom cross-sectional view of via

Fig.7. SEM inspection of the cross-sectional view of via.

*C. Backside via passivation.*

A SiO2 passivation layer was deposited on wafer backside and inside via holes by low-temperature PEVCD process at 100℃. The process was optimized for good step coverage, sufficient passivation thickness and acceptable deposition rate. Process result is shown in figure 6. A 1um-thick passivation layer at via bottom and sidewall was achieved to provide sufficient passivation effect.

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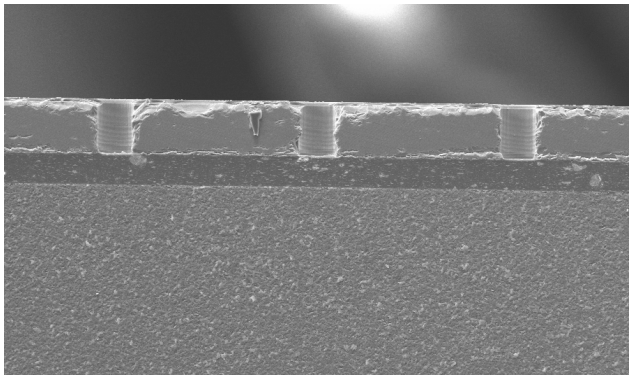
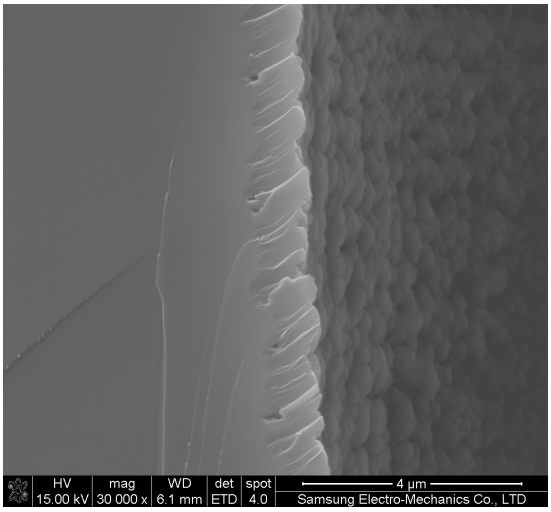


(a) passivation layer on backside surface.




(b) passivation layer on bottom sidewall

Fig. 8. SEM inspection of passivation layer deposition

### D. *Bottom electrical connection process*

Among various interconnection methods, via interconnection technology is selected to get diverse advantages like reducing the chip size. Generally in case of via interconnection method, metal filling by copper electroplating and copper polishing for planarization are used. It is very difficult to control the quantity of overburden of copper electroplating. Therefore for the subsequent fabrication process, removing the risen part of copper column is widely accepted method. However, during the copper polishing, it is possible to attack the passivation layer around the via hole and surface and then leakage current may be happened through the damaged passivation area. In this project, that possibility is basically eliminated by deleting the polishing process. The peculiarities of fabrication compared to the previous fabrication are first, deposited metal layer can not be used only seed layer but also redistributed line layer. Second, by using dry film resister for redistributed line patterning, copper polishing process can be eliminated. There are several advantages by using this fabrication process like the reducing the second metal deposition process, removing the possibility of happening of leakage current and so on. Figure 7 shows the schematic view of the patterning process of redistributed line with the overburden of copper filling. Figure 8 represents the SEM image of the result of copper filling process.

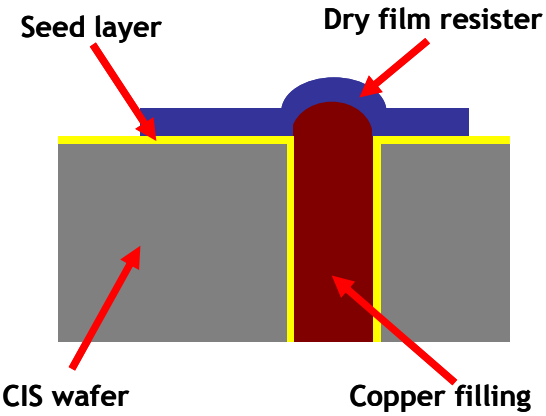



Fig.9 Schematic view of the patterning process of redistributed line with the overburden of copper filling.

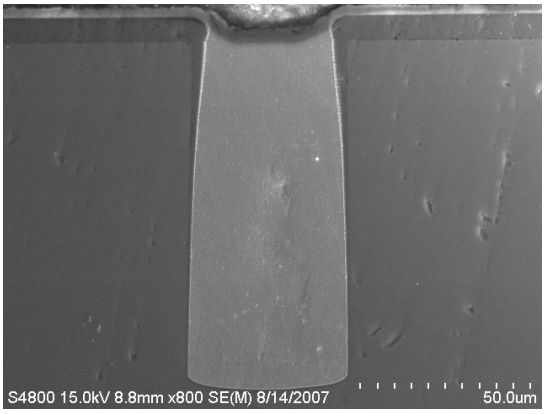



Fig. 10. SEM image of metal filling using copper electroplating method.

## V. CONCLUSION

A new concept, wafer level package for image sensor module which is composed Pyrex glass, polymer bonding layer and CIS wafer have been found to be suitable structure for the low cost reflowable package. We obtained optimal process parameter under constraint, like temperature. This package is realized with simple wafer level process technology. It is fabricated with small size (chip scale, 3.67 X 3.42 $mm^2$), thickness (400um), and low cost. It is suitable for mass production. The presented package can find applications where a compact overall device size is needed while keeping low temperature process, such as a image

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sensor module, bio chips, micro valve, optical switch and display.

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