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65nm CMOS Circuit Design of a Sampled Analog Signal Processor dedicated to RF Applications

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Abstract—The Software-Defined Radio (SDR) concept aims at designing a re-configurable radio architecture accepting all cellular or non-cellular standards working in the 0-5 GHz frequency range. Some technical challenges have to be solved in order to address this concept. A fully digital SDR system implying an A/D conversion close to the antenna is not feasible in the case of mobile terminal. This paper presents the design of an Analog Processor which process RF signal in order to select and convert into digital only the desired RF signal envelope. It uses the principle of a Fast Fourier Transform (FFT) to carry out basic analog functions with high accuracy at a low power consumption. Schematic and Post Layout Simulations are exhibited. Estimated die area and power consumption are numbered.

Index Terms—analog signal processing, software-defined radio, cognitive radio, sampled analog signal processor.

I. INTRODUCTION

THE telecommunication industry claims for multifunctional mobile terminals. All kind of applications such as audio, graphic or video data are told to be integrated in a same wireless device. But they have to accommodate different wireless standards with different carrier frequencies, channel bandwidths, modulation schemes or data rates [1], [2].

The concept of Software-Defined Radio (SDR) can solve the problem of the wireless convergence. Reconfigurable circuits and systems are part of the solution as they can be tuned to any frequency band, select any reasonable channel bandwidth, and detect any known modulation. This paper exhibits the architecture and the schematic of a SDR RF Front-End dedicated to mobile terminals.

An ideal receiving SDR architecture is only software. It is composed of a Low Noise Amplifier (LNA), an Analog to Digital Converter (ADC) and a Digital Signal Processor (DSP). But, the resolution required for the Analog to Digital conversion is not feasible at a 10GHz frequency and a low power consumption required in the case of a mobile terminal [3], [4]. A mixed analog architecture was thus proposed to overcome the A/D-conversion bottleneck. A component called Sampled Analog Signal Processor (SASP) located between the LNA and the ADC processes the RF input signal (Fig. 2). It carries out operations on discrete-time analog voltage samples. The signal is processed analogically and its data rate is decreased to be converted into digital at a lower frequency,

claiming a less-powerful ADC. Whereas the digital conversion technological bottleneck is avoided, new challenges appear in the analog domain.

The SASP is an analog processor performing an analog Discrete Fourier Transform (DFT). It is ruled by :

- Two parameters inherited from the DFT equation (Eq. 1) to master the SDR requirements such as reprogrammability and flexibility: the sampling frequency $f_{sampling}$ and the number of voltage samples N are taken into account to determine the spectral accuracy ($\frac{f_{sampling}}{N}$).
- Two basic analog operations: one operation was to delay the voltage samples. This is mathematically translated by z^{-1} in the z -domain. The second was to weight and calculate the samples. The combination of both operations gives the DFT calculation.

$$X(k) = \frac{1}{N} \sum_{n=0}^{N-1} x(n)W_N^{nk}, \quad k = 0, 1, \dots, N-1 \quad (1)$$

$$W_N = e^{-j(2\pi/N)}$$

where N is the number of samples and $x(n)$ is the input voltage sample value.

Once the spectrum processed and displayed by analog voltage samples, only the samples representing the desired RF signal envelope are converted into digital. The digital process is just a matter of recovering the modulated signal into baseband. This is compared to a frequency translation as the RF signal envelope is translated into baseband.

II. THE SAMPLED ANALOG SIGNAL PROCESSOR

The SASP is composed by 3 parts to calculate the FFT:

- The continuous-time signal pre-conditioning [5],
- The sampler and the FFT,

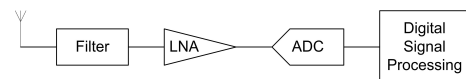


Fig. 1. Ideal SDR architecture

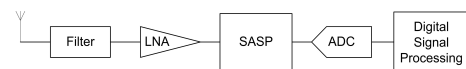


Fig. 2. Proposed SDR architecture

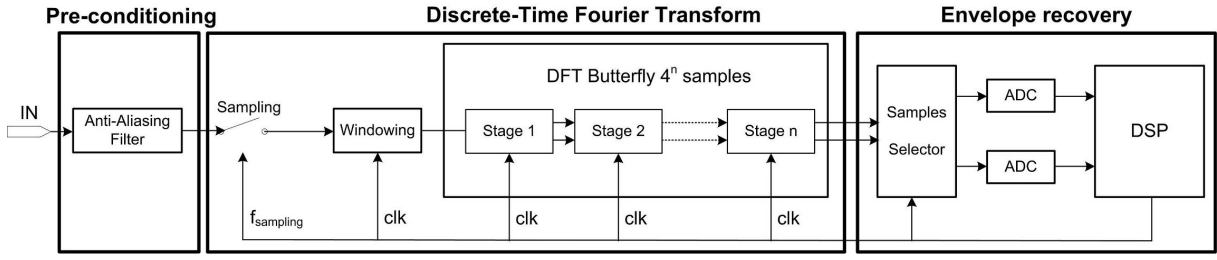


Fig. 3. SASP Architecture

- The envelope selection and conversion.

The SASP implements a pipeline FFT algorithm [6]. A radix-4 FFT using $\log_4(N)$ stages was chosen in order to improve the speed efficiency [7], [8]. All stages of a radix-4 FFT use a basic module with 4 weighted inputs (twiddle factors) and 4 outputs.

A pipeline implementation consists in using one basic module per stage which runs with two processing phases [7], [8]:

- 1) Summation/substraction and weighting factor [10].
- 2) Feedback storage.

The basic stage architecture is composed by a delay line, two "switching boxes", and a processing unit [11] to process the basic analog operations on voltage samples. The only difference between each stage is the frequency clock of the "switching box" and the length of the delay line equal to 3.4^{n-k-1} samples, $k \in [0; \log_4(N) - 1]$ [8].

The technology used to design the circuit is 65nm CMOS technology from STMicroelectronics. The analog implementation of the basic stage is composed by (Fig. 4):

- an input delay line (one for the real samples, and one for the imaginary samples),
- a weighting unit,
- a adding/substracting unit,
- a "feedback" delay line to serialize the samples at the stage output.

A. The Delay Line

The delay line processes a delay equivalent as a z -transformation to z^{-1} . It was carried out by an accumulation delay line that stores the voltage sample during a given time (Fig. 5). Three operating states of the delay line are performed. For example, at a given time:

- 1) One sample is loaded in a capacitor (S_1 is closed).
- 2) One sample is stored during the delay time (S_2 is open).
- 3) One sample is either carried out on the processing unit or on the output stage (S_6 is closed).

A delay line is composed by 3.4^{n-k-1} delay cells, $k \in [0; \log_4(N) - 1]$ (Fig. 7) [8]. A delay cell is composed by:

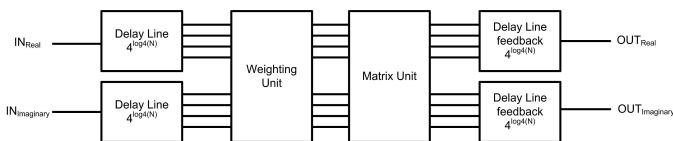


Fig. 4. Analog implementation of a Radix-4 FFT stage

- an input switch to load the voltage sample,
- a capacitor to store the voltage sample,
- an output switch to display the voltage sample.

Because the circuit runs mainly with charge transfers, DC offset errors are the main drawbacks induced (Eq. 2). Thus, a differential structure is chosen with both positive and negative signals centered on a DC voltage of 800mV with a linearity range of 200mV. Only the transistors non linearities and the parasitic capacitors matters remain. These specifications rule the all specifications of the circuit.

$$V_{out} = V_{in} \underbrace{\left(1 + \frac{W.L.C_{ox}}{C_{hold}}\right)}_{\text{non unity gain}} - \underbrace{\frac{W.L.C_{ox}}{C_{hold}}(V_{DD} - V_{TH})}_{\text{pedestal error}} \quad (2)$$

Each delay cell has a positive and a negative part to store the samples coming from the positive and the negative signals. An inside buffer protects the voltage samples against the output voltage variations and improves the charge transfer. It is implemented with a single transistor $M_{1,2}$ and a resistor $R_{1,2}$ (Fig. 6). It has a gain slightly superior to 1 to guarantee a gain of 2 along all the charge transfers to compensate the division by 2 provided by the FFT calculation. It has a linearity range of 200mV centered on the DC voltage of 800mV.

A trade off is done on the capacitor value. It has to enable a fast load of the voltage sample without loosing charge during the delay time. As the basic structure of a delay cell is based on capacitor, the die area occupied by the capacitor in the

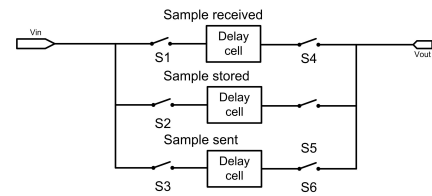


Fig. 5. Accumulation Delay Line

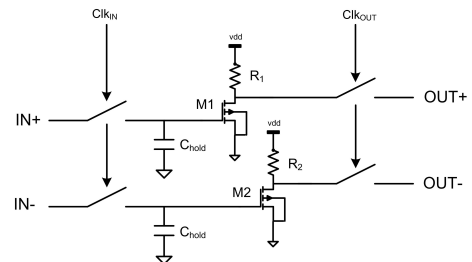


Fig. 6. Simplified schematic of a delay cell

circuit is also a factor to take into account. The all SASP counts $4^{\log_4 N} + 4^{\log_4 N - 1} - 2$ capacitors [8]. Thus, the trade off implies to choose a capacitor value as low as possible. The storage capacitor C_{hold} was 50fF (Fig. 6).

Fig. 8 presented the simulation of a charge transfer. The acquisition time is 491ps at a sampling frequency of 500MHz. The pedestal error is 0.11mV for a 30mV voltage sample. The inside buffer has a gain of 1.14 which leads to a total amplification of 2 during the charge transfer.

B. The Matrix Unit (MU)

MU adds and subtracts voltage samples 4 by 4 as described in the algorithm matrix in [9]. It is composed by basic adders. Each adder is designed with 4 transistors connected to a common resistor (Fig. 9). Each transistor has a size of $\frac{W}{L} = 20$. The current crossing each transistor is proportionnal to the input voltage equal to V_{gs} . The current crossing the resistor is the sum of the 4 currents coming from each transistors. Thus, the voltage seen at the drain of the transistors is proportionnal to the sum of the input voltages. As the circuit is differential, the structure subtracts voltage samples by inverting some of the positive signal input with the negative ones. In Fig. 9, IN3 et IN4 are inverted. Voltage samples on IN3 and IN4 are thus subtracted to those on IN1 and IN2. The Matrix contains adders et mixed adders/subtractors to carry out the FFT calculation.

C. The Weighting Unit (WU)

WU weights each sample with a coefficient $W_n^k = \cos(2\pi.nk) + i.\sin(2\pi.nk)$ (Eq. 1). The real part of the signal is weighted by $\cos(2\pi.nk)$ and the imaginary by $\sin(2\pi.nk)$ (Fig. 4). Every discrete sample is consequently weighted by a factor within the interval $[0, 1]$. The principle of the voltage/current/voltage conversion

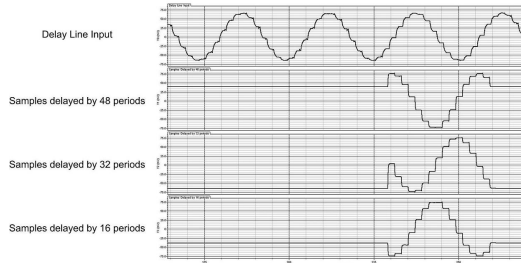


Fig. 7. Simulation of a delay line

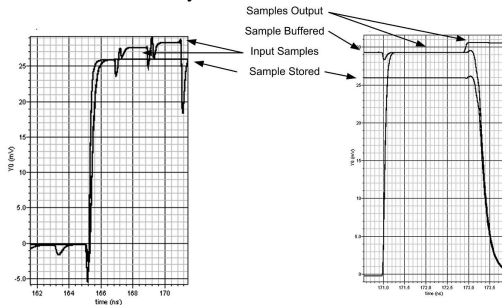


Fig. 8. Charge Transfer. Load and Display of a voltage sample

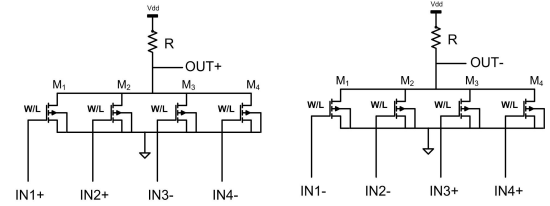


Fig. 9. Simplified schematic of a 4-voltage sample adder

coming from the matrix is used to carry out this analog operation. A switch network (S_x) selects the input voltage of each transistor gate (Fig. 10). The input voltage can be either a voltage sample to be weighted or the DC reference voltage (800mV). Tab. I depicts the possible configuration of the switch network. Every transistor (M_x) has a different size. It implies that the current crossing each transistor is no more proportionnal to the input voltage but to the width of the transistor.

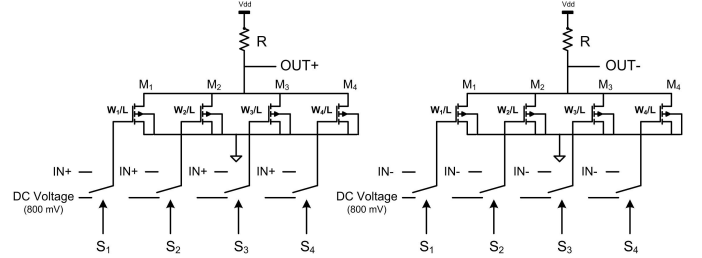


Fig. 10. Simplified schematic of the Weighting Unit

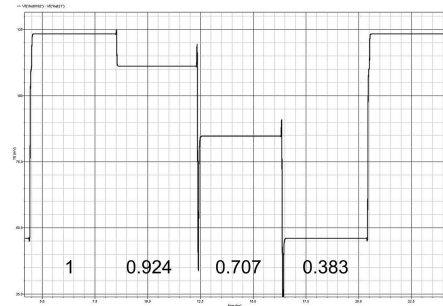


Fig. 11. A 100mV voltage sample weighted by 4 factors

Fig. 11 exhibits the weighting a 100mV voltage sample as shown in Tab. I. For instance, if M_3 and M_4 are switched on the input signal and M_1 and M_2 on the 800mV DC voltage reference, the voltage sample is weighted by 0.707.

D. The Feedback Delay Line

The Feedback delay line had the same structure of the input delay line. It receives 4 by 4 the voltage samples through 4 inputs and serializes all of them on a single output.

III. RESULTS

The circuit considered here is a 64-point radix-4 FFT processor. There are $\log_4(64) = 3$ stages. It carried out an Analog FFT working at 500MHz to target the processing of RF signals in the 0-250MHz frequency range. A Post Layout Simulation

TABLE I
WEIGHTING UNIT COEFFICIENTS APPLICATION

Switch Network Configuration				Coefficients			
S_1	S_2	S_3	S_4	For a 100mV input voltage sample simulation			
Transistor Characteristics							
$M_1 \frac{W_1}{L} = 2.1$	$M_2 \frac{W_2}{L} = 5.3$	$M_3 \frac{W_3}{L} = 7.8$	$M_4 \frac{W_4}{L} = 9.3$	$\cos(2\pi.nk)$	Output	Effective Coefficient	Error
DC	DC	DC	DC	0	0	0	0%
DC	DC	DC	IN	0.383	45.9mV	0.372	2.87%
DC	DC	IN	IN	0.707	84.5mV	0.686	2.97 %
DC	IN	IN	IN	0.924	111mV	0.901	2.48%
IN	IN	IN	IN	1	123.1mV	1	0%

(PLS) exhibited the FFT delivered by the SASP (Fig. 12). The input signal is a sinusoid at 39MHz ($\frac{5 * f_{sampling}}{64}$). The spectrum processed can be identified as pulses of the Fourier Transform of a sinewave. The characteristics of the 64-point circuit is shown in Tab. reftab:charac with a 1.2V supply voltage. A layout view of the first stage is presented in Fig 13. Three parts of the stage schematic can be recognized: the input delay line, the matrix unit, the feedback delay lines. The perspectives are to display a SASP dedicated to a RF Front-End processor. It intends to carry out at least a 4096-point analog FFT, working at 5GHz. Technological and design improvements will lead to a power consumption under 500mW to design this circuit.

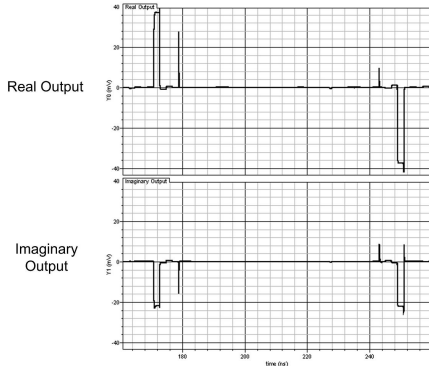


Fig. 12. Simulation of a 64-point SASP

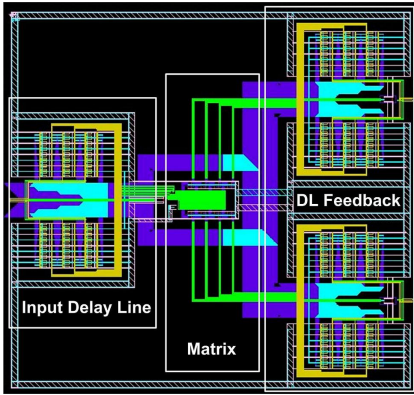


Fig. 13. Layout view of the first stage

IV. CONCLUSION

The SASP is an Analog Processor dedicated to RF applications. It aims at lowering the RF signal frequencies by

TABLE II
64-POINT SASP CONSUMPTION AND DIE AREA

Building Block	Power Consumption		Die Area (mm^2)
	@ 500MHz	@ 1GHz	
4-sample delay line	2,80mW	3,08mW	0.0126 mm^2
16-sample delay line	11,22mW	12,35mW	0.0338 mm^2
64-sample delay line	44,88mW	49,42mW	0.0481 mm^2
4-sample Weighting Unit	9,24mW	9,24mW	0.0120 mm^2
16-sample Weighting Unit	75,90mW	75,90mW	0.0523 mm^2
Matrix Unit	23,08mW	23,08mW	0.0060 mm^2
Stage 1	162,36mW	167,4mW	0.385 mm^2
Stage 2	81,34mW	83,21mW	0.208 mm^2
Stage 3	113,1mW	114mW	0.301 mm^2
64-point SASP	372mW	378mW	3.1 mm^2

selecting the RF signal envelope. Only the desired signal envelope is converted into digital. Hence, the ADC worked at a dramatically reduced frequency and the A/D conversion technological bottleneck is avoided. This paper exhibited the circuit design of the SASP in a 65nm CMOS technology. It draws the way to a Processor able to handle telecommunication signals, compatible with the SDR concept.

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