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D. Fernandez, J. Madrenas, M. Dominguez, J. Pons, J. Ricart. Pulse-Drive and Capacitance Measurement Circuit for MEMS Electrostatic Actuators. DTIP 2007, Apr 2007, Stresa, Iago Maggiore, Italy. pp.28-32. <hal-00257656>

HAL Id: hal-00257656

<https://hal.science/hal-00257656v1>

Submitted on 20 Feb 2008

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PULSE-DRIVE AND CAPACITIVE MEASUREMENT CIRCUIT FOR MEMS ELECTROSTATIC ACTUATORS

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ABSTRACT

In this paper we present an electronic circuit for position or capacitance estimation of MEMS electrostatic actuators based on a switched capacitor technique. The circuit uses a capacitive divider configuration composed by a fixed capacitor and the variable capacitance of the electrostatic actuator for generating a signal that is a function of the input voltage and capacitive ratio. The proposed circuit can be used to actuate and to sense position of an electrostatic MEMS actuator without extra sensing elements. This approach is compatible with the requirements of most analog feedback systems and the circuit topology of pulsed digital oscillators (PDO).

Keywords: Capacitance, distance, estimation, capacitive divider, pulsed digital oscillators, PDO.

1. INTRODUCTION

Capacitance estimation of electrostatic actuators is the first step in developing complex control systems which includes some kind of feedback loop of the capacitance or distance between plates of the actuator [1]–[4]. Usually, those systems rely on complex optical measurements [5] or anchored capacitive sensors to obtain its value [6]; however, the actuator capacitance can be estimated by processing only the driving signal applied to the actuator. Two main approaches have been proposed in the literature. First one is the integration of the current drained by the actuator with a digital PWM driving signal [7] or with an arbitrary waveform signal [4]. Both exploit the relation $C(t) = Q(t)/V(t)$ and need to perform an integration of the actuator current, which leads to severe problems in sensitivity, due to its small magnitude and drift, phenomena inherent to analog integrators. Second one is the capacitive-divider architecture with current excitation [8], but it has limitations in both switching speed and leakage. Despite the apparent simplicity of both architectures, important problems arise when those circuits are intended to be used in a fast-varying, small capacitance and high voltage environment characteristic of electrostatic actuators.

In this paper we present a capacitive-divider circuit for estimating the actuator capacitance with a pulsed or

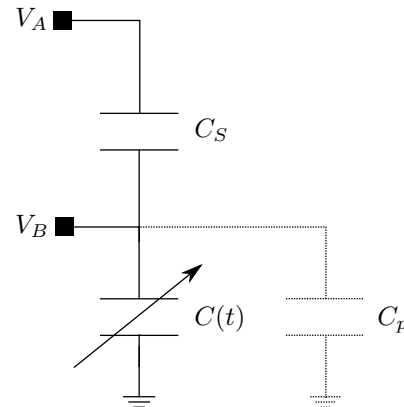


Fig. 1. Architecture of a capacitive divider based estimation circuit.

PWM driving signal. The proposed circuit can measure the electrostatic actuator position, without needing charge-discharge cycles to update the actuator position estimation. This reduces the injection of mechanical noise in the moving plate position, making the approach well suited for analog position feedback systems, like tunable lasers [9] or optical filters [10], as well as the circuit topology of pulsed digital oscillators (PDO) [11], where sparse, small-width excitation reset pulses are required as excitation signals and high-bandwidth, low phase shift is required in the estimated position. The simplicity of the approach, which is based only in MOS switches and voltage followers, make it suitable for high-voltage operation and easy design and calibration.

2. THE CAPACITIVE-DIVIDER ESTIMATOR

2.1. Working principle

The circuit architecture is based on a capacitive-divider configuration, shown in figure 1. Applying classic circuit analysis we have:

$$V_A - V_B = V_A \left(1 - \frac{C_S}{C_S + C(t) + C_P} \right) \quad (1)$$

where V_A is the input voltage, V_B is the output voltage, C_S is a fixed capacitor, $C(t)$ is the capacitance of the actuator and C_P is the main parasitic capacitance. It is necessary that $C_S \gg C(t)$ for a proper operation of the circuit. Note that the high value of the series capacitor does

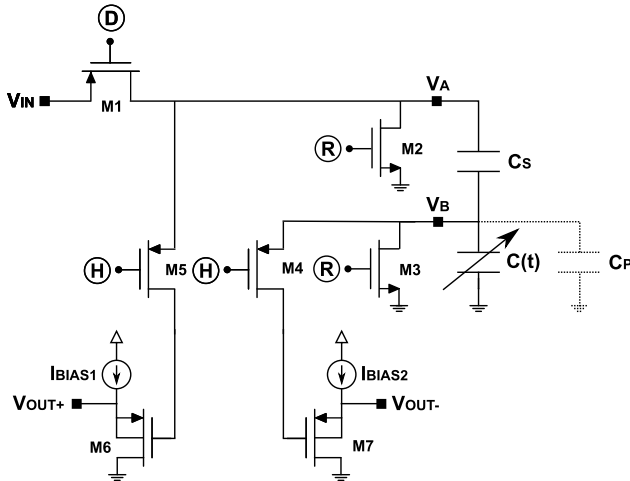


Fig. 2. Schematic of the capacitance estimation circuit. C_S is a fixed capacitor, $C(t)$ is the capacitance of the actuator, V_{IN} is a constant input voltage and the outputs are V_{OUT+} and V_{OUT-} . The capacitance C_S is much higher than the actuator capacitance.

not have any effect on the actuator stability, nor implies a significant pull-in voltage increase, as reported in [12]. With this condition, the only relevant parasitic capacitance is C_P , and previous expression can be approximated to:

$$V_A - V_B \approx C(t) \frac{V_A}{C_S} + C_P \frac{V_A}{C_S} \quad (2)$$

If the input voltage V_A is a pulse-width modulated (PWM) signal, changing between a high voltage V_{IN} and 0 V , the parasitic capacitance represents only a constant voltage offset easy to compensate at electronic level. The mean electric force generated by the input voltage determines the equivalent continuous-time actuation voltage. Note, however, that the measurement can only be done when V_A is at its high state. This could lead to measuring problems if the frequency and duty cycle of the PWM signal are both too low, because the actuator position could change and the estimation circuit might not notice. This can only happen if the PWM frequency is near or below the mechanical resonance: simplest solution is to increase the PWM frequency, but if the application cannot tolerate it, the actuation voltage should be reduced so the duty cycle can be increased to have the same electrostatic force.

Also, it is important to notice that the output node V_B has an infinite DC output impedance, so, no long-term stability of the measure can be guaranteed with this simplified architecture, as was shown in [8], due to leakage.

2.2. Driving and sensing circuit

The proposed circuit schematic is shown in figure 2. Transistors M_1 , M_2 , M_3 , M_4 and M_5 are MOS switches controlled by signals R (Reset), D (Disconnect) and H (Hold). M_6 and M_7 are PMOS voltage followers that track the capacitor voltages and provide electrical isolation to those nodes, so a circuit of finite input impedance or

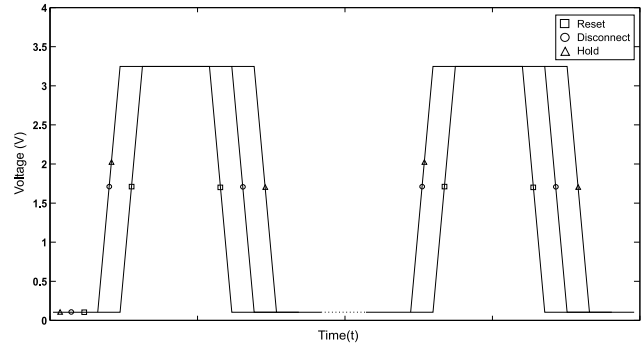


Fig. 3. Temporal evolution of the Reset (R), Disconnect (D) and Hold (H) control signals.

a measuring instrument can be connected to sense the capacitance of the actuator without increasing the leakage at V_B node. PMOS followers require a supply voltage higher than the input voltage V_{IN} , but they are able to buffer the signal even when the input voltage approaches ground. If this is not required, NMOS buffers could be used instead. It is recommended that those followers have their bulk connected to the source so no body-effect related distortion exists.

Note that the output voltage is taken as a difference of the signals V_A and V_B . Even though V_A is a constant voltage at the sampling time, it is sampled too. This is done because that way, any noise or charge injection that affect both lines (common-mode noise) compensates with a differential measurement.

To generate the three control signals, a standard-cell digital circuit and a chain of starving inverters were designed so only one external clock signal is needed to control the switches. This clock signal performs both the reset operation, so the DC impedance at the V_B node can be kept small and hereby the leakage does not have an effect, and the PWM modulation of the input voltage V_{IN} , so the actuation voltage can be easily modulated without any additional high-voltage circuitry. The generated sequence runs as depicted in figure 3. Initially, all signals are reset to 0. V_{IN} is being applied to the capacitor structure, and V_A and V_B are being tracked by the voltage followers and transmitted to V_{OUT+} and V_{OUT-} , respectively. Then, signals Disconnect and Hold are turned on. The capacitors are disconnected from V_{IN} and V_A and V_B are stored in the gate capacitance of the voltage followers, so the outputs V_{OUT+} and V_{OUT-} are kept constant regardless of the capacitor voltages. Next, a Reset pulse is generated, discharging both capacitors. Then, signal Disconnect is set to zero, so the capacitors are charged again. Finally, when the capacitors are charged, signal Hold is deactivated and the outputs track again the capacitors' voltages and the cycle starts again.

The timing of the sequence cannot be arbitrarily fast. The Reset pulse width has to be long enough to discharge both capacitors through the ON resistance of transistors

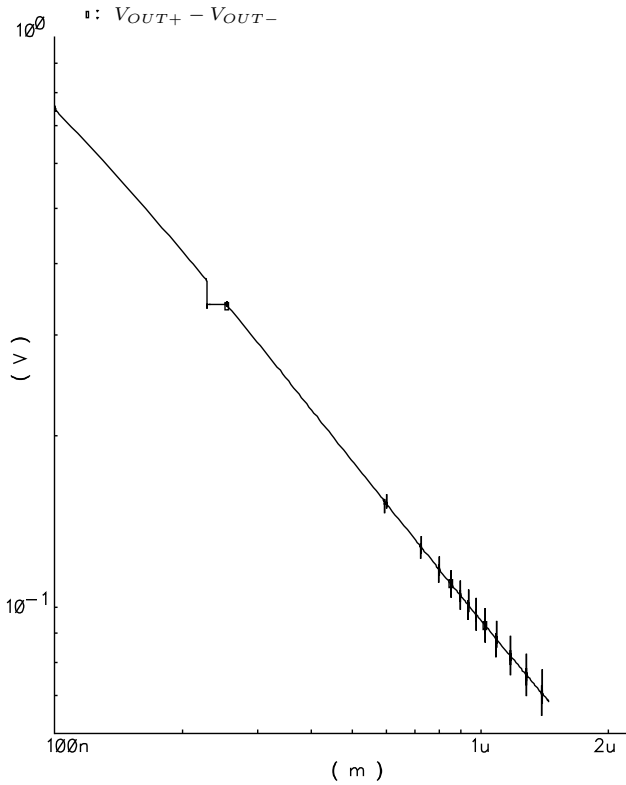


Fig. 4. Plot of the output voltage vs. distance between plates. Both axes are in logarithmic scale so the ideal response becomes a straight line. The steps are caused by the Hold signal.

M_2 and M_3 . Otherwise, the circuit would have a memory effect that could produce a long-time effect in the circuit response. Besides, the delay between signals Disconnect and Hold falling edges must be long enough for the ON resistance of M_1 to charge the capacitors to avoid a glitch to be propagated to the output nodes. Also, the switch leakage currents limit the maximum time between different sequences. Prior works [8] show that leakage will require at least a reset sequence every few seconds or less.

Note that the compensation of the parasitic capacitance can be done by adjusting the current source I_{BIAS2} , so the output voltage is tuned to cancel the parasitic effect.

2.3. Simulations and layout

The simulations were performed with the Spectre simulator at post-layout transistor-level. A verilog-A model of an electrostatic actuator was developed to allow co-simulation between the electrical and mechanical domains. Special care was taken to correctly adjust the simulator tolerances and the minimum conductance or anomalous results can be obtained, since electrostatic actuator charge, current and position are usually below the default precision of electronic simulators and this causes long-term anomalies in the result.

The electrostatic actuator parameters are shown in table I. They were taken directly from the data reported in [13], with the exception of the mass and damping, which

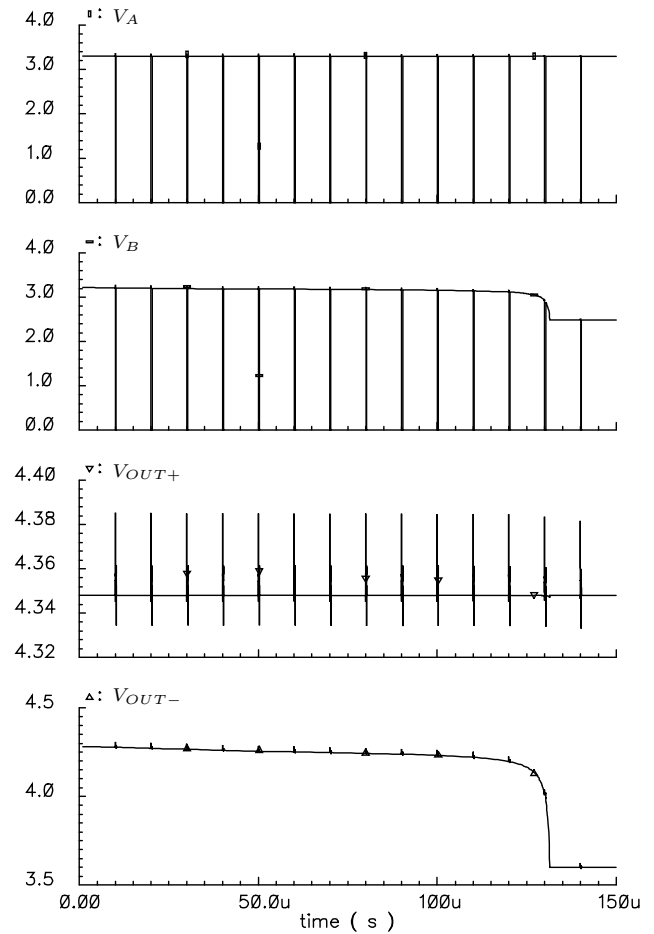


Fig. 5. Transient simulation: The actuator begins moving from the on-rest position at $t = 0$ and stops when it reaches the mechanical stoppers (located at $100nm$ of the bottom plate) at $t = 130\mu s$. Plot shows V_A , which is the voltage applied to the upper node of the serial capacitance, V_B , which is the actuator voltage, and the output voltages V_{OUT+} and V_{OUT-} . The actuation voltage is $3.3V$, serial capacitor $C_S = 100pF$, pulse width is $250ns$ and pulse frequency $50kHz$.

were not directly available. Mass was deduced from the frequency of the mechanical resonance of the actuator, and damping was adjusted to have a quality factor near unity. With those parameters, a batch of extensive simulations was performed to validate the electrostatic actuator model and circuit behaviour.

TABLE I
ELECTROSTATIC ACTUATOR PARAMETERS

Parameter	Value
k (N/m)	32
g_0 (m)	1.45×10^{-6}
A (m^2)	3.6×10^{-7}
m (Kg)	5.11×10^{-9}
b (Ns/m)	8.08×10^{-4}

A plot of the differential output voltage versus distance between plates is shown in figure 4. The plot was drawn by performing a transient simulation of the distance between

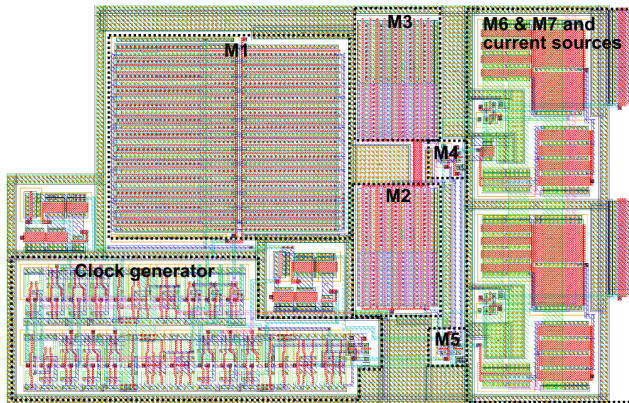


Fig. 6. Layout of the complete capacitance estimator circuit. Main parts are pointed out. Total area is 0.011mm^2 .

the plates of the actuator and the output voltage of the circuit and plotting them one against each other so the time variable is cancelled. The frequency of the pulses has been set to 50kHz with a 250ns pulse width, so the effect in the output signal during the actuator displacement over the full gap can be seen as steps or glitches on the output voltage in Fig. 4 and 5.

In figure 5 the transient response of the output nodes of the circuit is represented. Note that signals V_{OUT+} and V_{OUT-} have a noticeable charge transfer effect, but the output taken as difference of both signals has much reduced effect thanks to the cancellation when the difference is computed.

The layout of the complete circuit, including the clock generator, is shown in figure 6. It has an area of 0.011mm^2 and is designed for a 3.3V , $0.35\mu\text{m}$ CMOS 2P5M technology. At the time of writing this manuscript the testchip is being manufactured. Future work will develop a high voltage version of this circuit ($\approx 70\text{V}$), after this low voltage prototype has been experimentally verified. Note that, besides the clock generator, most of the area is occupied by the transistors $M1$, $M2$ and $M3$ due to the necessity to have a reduced ON resistance in those switches. That way, the circuit can operate with a very small Reset pulse width, if necessary.

3. CONCLUSIONS

A new circuit able to continuously measure the capacitance, position or distance between plates of an electrostatic actuator has been proposed. Its working principle allows an estimation of the position with only processing two voltage signals, and does not require anchored capacitive sensors or optical measurements to obtain its value. The main advantages are its simplicity, design and easy integration in high or low-voltage CMOS fabrication process. Its capability of measuring with only sparse clock or reset signals and the small width of those signals make it suitable for environments where the position of the electro-

static actuator cannot be affected by spurious signals, for example, pulsed digital oscillators, micromirrors, tunable lasers, optical filters, etc. Its main limitation is related to leakage, which limits the maximum time between clock or reset signals.

The first step of the future work will include the development of a high-voltage version of the proposed circuit and simulations of the circuit in a complete application, for example, pulsed digital oscillators and analog feedback positioning for electrostatic actuators. Second step will include experimental verification of previous work.

4. ACKNOWLEDGMENTS

This work was supported in part by the Spanish Ministry of Education and Science under Projects TEC2004-03940 and TEC2004-00236/MIC. Daniel Fernández holds a research fellowship supported by the Catalan Department of Universities, Research and Information Society (DURSI) and the European Social Fund (ESF).

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