



HAL
open science

Selective etching of Pt with respect to PtSi using a sacrificial low temperature germanidation process

Nicolas Breil, Aomar Halimaoui, Thomas Skotnicki, Emmanuel Dubois, Guilhem Larrieu, Adam Łaszcz, J. Ratajczak, G. Rolland, Arnaud Pouydebasque

► To cite this version:

Nicolas Breil, Aomar Halimaoui, Thomas Skotnicki, Emmanuel Dubois, Guilhem Larrieu, et al.. Selective etching of Pt with respect to PtSi using a sacrificial low temperature germanidation process. Applied Physics Letters, 2007, 91, pp.232112-1-3. <10.1063/1.2821143>. <hal-00255853>

HAL Id: hal-00255853

<https://hal.science/hal-00255853v1>

Submitted on 18 Sep 2024

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire HAL, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



HAL Authorization

Selective etching of Pt with respect to PtSi using a sacrificial low temperature germanidation process

N. Breil,^{a)} A. Halimaoui, and T. Skotnicki
STMicroelectronics, 850 rue Jean Monnet, 38926 Crolles Cedex, France

E. Dubois and G. Larrieu
IEMN, UMR CNRS 8520, Avenue Poincaré, Cité Scientifique, 59652 Villeneuve d'Ascq Cedex, France

A. Łaszcz and J. Ratajczak
Institute of Electron Technology, Al. Lotników 32/46, 02-668, Warsaw, Poland

G. Rolland and A. Pouydebasque
CEA-LETI, 17 rue des Martyrs, 38054 Grenoble Cedex, France

A soft and scalable etching procedure that selectively eliminates Pt without altering PtSi is proposed. The selective etch is based on the low temperature transformation of the excess Pt into a more reactive Pt_xGe_y phase that is easily etched in a sulfuric peroxide mixture. The mechanism of Pt_xGe_y alloying is detailed based on x-ray diffraction analysis. The innocuousness of the germanidation-based selective etch on the integrity of the PtSi/Si junction is consolidated by Schottky barrier measurements. This process is expected to facilitate the integration and the scalability of PtSi on ultrathin silicon layers. © 2007 American Institute of Physics.

[DOI: [10.1063/1.2821143](https://doi.org/10.1063/1.2821143)]

PtSi is very attractive for future very large scale integration technologies as a band-edge source/drain (S/D) material for submicron *p*-type metal-oxide-semiconductor field-effect transistors (*p*-MOSFET) that could alleviate hard constraints placed on the specific contact resistivity. Moreover, as an attempt to circumvent the difficult challenges associated to the formation of shallow doped extensions,^{1,2} the integration of low Schottky barrier metallic junctions also deserves a particular attention because the absence of dopants inherently suppresses the need for high temperature annealing required for their activation. In that context, PtSi appears as the candidate of choice for both flavors of *p*-MOSFET S/D junctions, either degenerately doped Ohmic or undoped Schottky, because it offers a reduced Schottky barrier that promotes efficient carrier injection. Moreover, PtSi also features a low temperature of formation^{3,4} as well as a reduced consumption of silicon during the silicidation reaction. From a practical standpoint, silicided contacts in MOSFET devices are properly implemented using a self-aligned process. It involves (i) the deposition of a metal overlayer onto the device top surface, (ii) the thermal activation of the silicidation reaction where Pt and Si form a direct interface, and (iii) the removal of the metal excess either due to partial Pt consumption or due to unreacted Pt over an insulating film (e.g., SiO₂ or Si₃N₄ spacers). Owing to its noble metal properties, platinum is known to be exclusively soluble in aqua regia (AR) solutions (HCl/HNO₃/H₂O) implemented under various dilution and temperature conditions.⁵ However, previous reports reveal that AR is far from being satisfactory because it requires the superficial oxidation of PtSi to achieve selectivity with respect to platinum.^{6,7} Upon completion of the silicidation reactions, silicon atoms can further diffuse to the surface of the silicide and react with oxygen.^{8,9} In order to obtain a fully protective SiO₂ overlayer, an oxidation step at high

temperature (600 °C) in O₂ ambient is, therefore, recommended.^{5,7,10} However, this strategy is hardly applicable to very thin silicide layers because oxygen can reach and alter the PtSi/Si interface, both morphologically and electrically. In this letter, a highly selective etch procedure that circumvent the use of AR is proposed. It is based on the low temperature transformation of a chemically stable Pt layer into a more reactive Pt_xGe_y phase that is easily etched in sulfuric peroxide mixture (SPM). It is demonstrated that this process does not alter the integrity of the PtSi layers. Its suitability to selectively etch platinum with respect to its monosilicide phase is consolidated through the accurate extraction of the Schottky barrier height.

In the following description of the samples, Pt and Ge were systematically deposited by e-gun evaporation. Starting from a base pressure of 1×10^{-7} mbar, a gentle Ar⁺ plasma etch at 150 eV was realized to definitely eliminate residual traces of contaminants. The experimental investigations involved three sets of samples. The first one (S1) consists in *p*-type Si substrates on which a 20 nm thick SiO₂ full sheet layer was thermally grown. A 20 nm thick Pt layer covered by a 45 nm thick Ge overlayer was annealed at temperatures ranging from 200 to 600 °C to study the mechanisms of Pt_xGe_y phase transformation by grazing angle x-ray diffraction (XRD) and the etching properties of the resulting alloy in SPM. The second set of samples (S2) was devised to probe electrical characteristics of PtSi, namely, the sheet resistance and the Schottky barrier height, to evaluate the impact of the proposed germanidation selective etch. It starts from the same initial substrate than S1 but accommodates large square windows ($100 \times 100 \mu\text{m}^2$) opened in the SiO₂ top layer. These windows are associated by pairs and are separated by a micrometer gap, hence, forming back-to-back contacts separated by a silicon resistance. To proceed to the contact silicidation, samples S2 first received a deoxidation dip in hydrofluoric acid (1%) for 30 s and were subsequently

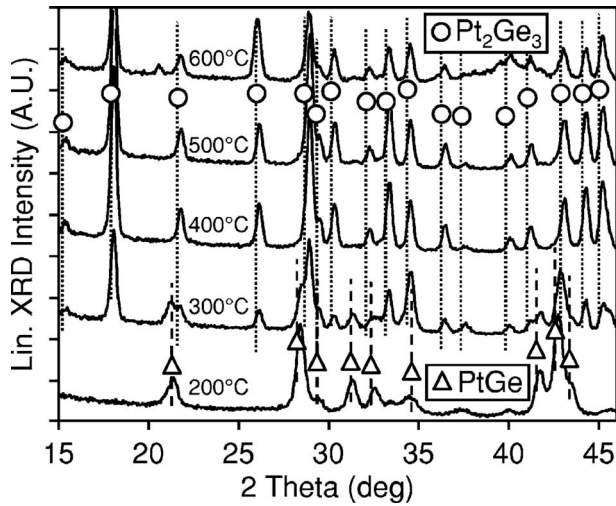


FIG. 1. XRD spectra of the Pt_xGe_y phases obtained from alloying of a Ge(45 nm)/Pt(20 nm) stack on a SiO_2 substrate (sample set S1) showing changes in Pt_xGe_y stoichiometry with the temperature of germanidation.

covered by a 20 nm thick Pt layer. PtSi was obtained by rapid thermal annealing (RTA) at 500 °C for 4 min under forming gas ($N_2:H_2, 95:5$). It is worth noting that the silicidation reaction occurred only on the contact regions offering a bare Si surface while Pt remained in its metallic state in regions covered by SiO_2 . At this stage, samples S2 were reloaded in the evaporation system to deposit a 45 nm thick Ge overlayer. Finally, the germanidation of untransformed Pt was achieved by RTA at temperatures ranging from 100 to 600 °C for 5 min in forming gas. When specified, the elimination of the sacrificial Pt_xGe_y phase was realized using SPM for 2 min. A third set of samples (S3) was processed similarly to S2 but without the deposition of Ge. The unreacted Pt was subsequently removed using a standard AR solution. For the sake of accurate comparison with samples treated with the germanidation-based selective etch, S3 samples received the same final germanidation anneal than the S2 counterparts although Ge was not deposited.

Based on S1 samples, the mechanism of germanidation was investigated using four-points probe sheet resistance measurements as well as XRD analysis. The diffraction peak analysis in Fig. 1 shows that the sample annealed at 200 °C is composed of the PtGe phase. This phase exhibits the lowest sheet resistance as reported in Fig. 2. In Figure 2(a), the corresponding morphological characterization by cross-sectional transmission electron microscopy (TEM) confirms that the entire Pt layer reacted with Ge. At 300 °C, the peak doublet located around 22° on the XRD spectra in Fig. 1 highlights the presence of both PtGe and Pt_2Ge_3 phases. At 400 °C and above, only the Pt_2Ge_3 phase is detected. The corresponding sheet resistance that increases up to $\sim 18 \Omega/\square$ can be related to the structure in columnar grains as evidenced by the TEM view in Fig. 2(b). Around 600 °C, the Pt_xGe_y layer was found to agglomerate resulting in a significant increase ($\sim 30 \Omega/\square$) of the sheet resistance, as shown in Fig. 2.

Considering atomic densities¹¹ of 6.64×10^{22} and 4.42×10^{22} at./cm³ for Pt and Ge, respectively, the thicknesses of Ge consumed by the germanidation reaction are 30 nm for the formation of PtGe and 45 nm for the Pt_2Ge_3 phase. In order to feed the reaction of Pt_2Ge_3 phase transformation with a sufficient amount of germanium to totally ab-

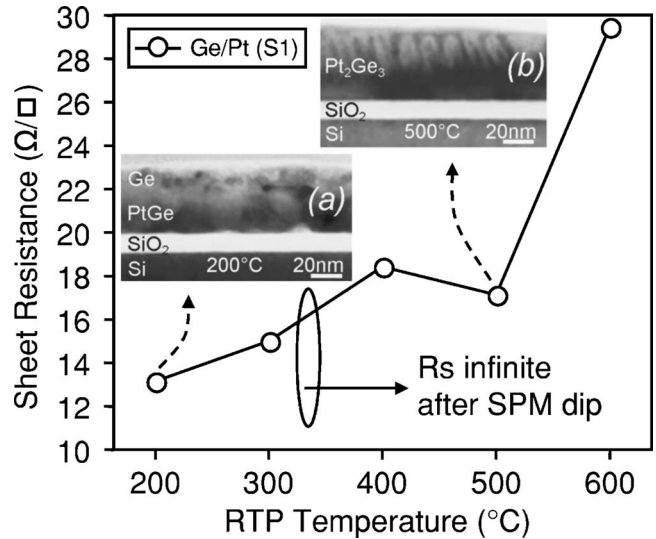


FIG. 2. Variations of the sheet resistance with the temperature of germanidation of the Pt_xGe_y layers presented in Fig. 1 (sample set S1). Note that this resistance becomes infinite after etching in SPM, indicating that the underlying Pt layer was totally consumed by the germanidation reaction. Inset: (a) TEM cross section showing the morphology of the uppermost Ge/Pt layers after alloying at 200 °C. The PtGe phase transformation does not totally consume the Ge overlayer, (b) same as (a) for a germanidation temperature of 500 °C. The Ge overlayer is totally absorbed by the resulting Pt_2Ge_3 phase.

sorb platinum, the thickness of the Ge overlayer was set 45 nm. After platinum germanidation in the PtGe phase, the TEM analysis in Fig. 2(a) confirms that a 15 nm thick unreacted Ge overlayer is still present on the top of the sample with a thickness that closely matches the expected value. Because the remaining Ge layer reacts with PtGe to form the Pt_2Ge_3 phase at higher temperatures, no trace of unreacted germanium is detected as evidenced in Fig. 2(b). As already pointed out in the literature,^{12–15} the above experiments suggest that the Ge content in the Pt_xGe_y phases increases with temperature. Another important result is the demonstration that the stoichiometry of the platinum germanide layer can be tuned by an appropriate selection of the Ge overlayer and of the temperature of reaction.

In order to check for the solubility of the PtGe and Pt_2Ge_3 phases, S1 samples were dipped into SPM ($H_2SO_4:H_2O_2, 1:1$) for 2 min. A highly exothermic reaction inducing a violent ebullition was observed at the surface of the substrate. After chemical reaction, scanning electron microscopy observations (not presented here) and sheet resistance measurements in Fig. 2 confirm that both PtGe and Pt_2Ge_3 phases were completely etched away. It is worth noting that a remaining Ge overlayer standing over the platinum germanide phase cannot act as a barrier to etching because Ge also etches rapidly in SPM. By way of partial conclusion, the above described series of experiments confirm that an alternative exists to the aggressive and unstable use of AR. However, the innocuousness of Ge deposition and Pt_xGe_y formation, the constraint of selectivity between Pt and PtSi, as well as the impact of Pt_xGe_y etching on the underlying PtSi contact still remain pending queries. The first question can be partially tackled from the thermodynamics standpoint. The heat of formation of PtSi (Ref. 16) ($\Delta H_f = -0.50$ kJ/g) being lower than that of PtGe (Ref. 17) ($\Delta H_f = -0.34$ kJ/g), Pt is expected to predominantly form a silicide rather than a germanide. Considering that the silicide phase is already

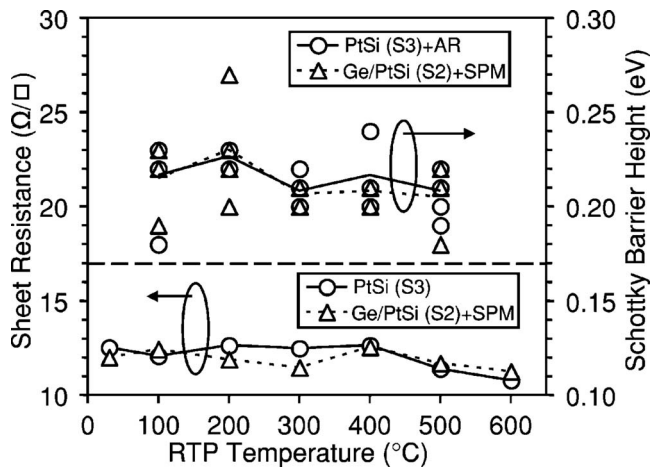


FIG. 3. Sheet resistance and measured Schottky barrier height to holes (Φ_{bp}) of the PtSi layer: comparison of results obtained from (i) a conventional process with AR (sample set S3, note that the sheet resistance was measured before the AR selective etch) and (ii) the proposed selective etch based on sacrificial Pt_xGe_y formation and SPM selective etch (sample set S2). The effect of the germanidation temperature is described. For the sake of comparison, the conventional PtSi process was exposed to the same (postsilicidation) thermal budget, although Ge was not present.

formed before Ge is deposited, this assertion is even more physically sound. To consolidate this view, samples from sets S2 and S3 for which Pt excess was removed using the Pt_xGe_y +SPM sequence and AR, respectively, have been compared from the electrical standpoint. It is worth noting that some of the PtSi contacts (not measured) were severely attacked by the AR etching. The PtSi sheet resistance was measured before the AR etching on large Pt-silicided areas, and the Schottky barrier height to holes (ϕ_{bp}) at the PtSi/Si interface was determined from back-to-back diodes according to an extraction procedure described elsewhere.¹⁸ In Fig. 3, PtSi control samples (S3) feature a stable sheet resistance of $12.5 \Omega/\square$, for a postsilicidation annealing (equivalent to the germanidation thermal budget) up to 400°C . At temperatures of 500 and 600°C , the sheet resistance was observed to slightly decrease to 11.5 and $10.5 \Omega/\square$, respectively. Samples S2 prepared with the germanidation technique closely follow the same behavior. The slight discrepancy between the sheet resistance of both samples can be attributed to scattering in sample-to-sample measurements and to variation of thickness of the PtSi layer.

The Schottky barrier height of the PtSi/Si junction was extracted for temperatures of germanidation ranging from 100 to 500°C after the AR etching. Measurements were repeated to obtain a statistically representative distribution, as shown in Fig. 3. While a usual dispersion was obtained for this type of experiment, it is interesting to note that the average ϕ_{bp} remains almost constant (0.21 – 0.23 eV) with temperature regardless of the initial contact stack and of the etching procedure. This measurement is also consistent with

ϕ_{bp} values usually reported in the literature.³ From the above experiments, it can be concluded that (i) deposition of Ge, (ii) its thermally activated transformation in Pt_xGe_y from metallic platinum in excess, and (iii) the final chemical etching in SPM does not impact the Schottky barrier height at the PtSi/Si interface. This result also confirms the thermodynamics-based assumptions that a Ge overlayer does not interact with the already formed PtSi/Si junction.

To conclude, the validation of a selective etch procedure based on a sequence involving germanidation of Pt in excess and removal of the sacrificial Pt_xGe_y in SPM opens an industrially viable integration scheme for PtSi contacts. Unlike the approach using a superficial oxidation of PtSi, the proposed technique avoids any unwanted consumption of silicon to build up the protective SiO_2 barrier. Therefore, it also considerably facilitates the integration and improves the scalability of PtSi on ultrathin silicon layers (e.g., ultrathin-body silicon-on-insulator) for which the amount of silicon is extremely limited.

This work was supported by European Commission through the METAMOS project (METAllic source/drain Architecture for Advanced MOS technology, IST-FP6-016677).

¹E. Dubois and G. Larrieu, *Solid-State Electron.* **46**, 997 (2002).

²G. Larrieu and E. Dubois, *IEEE Electron Device Lett.* **25**, 801 (2004).

³P. Gas and F. M. d'Heurle, in *Properties of Metal Silicides*, edited by K. Maex and M. Van Rossum (INSPEC, London, U.K., 1995), p. 280.

⁴W. J. Taylor, E. Verret, C. Capasso, J.-Y. Nguyen, L. B. La, E. Luckowski, A. Martinez, C. Happ, J. Schaeffer, M. Raymond, and P. Tobin, *Proceedings of the International Workshop on Junction Technology, 2004* (unpublished), pp. 107–112.

⁵Z. Zhang, S.-L. Zhang, M. Östling, and J. Lu, *Appl. Phys. Lett.* **88**, 142114 (2006).

⁶M. J. Rand and J. F. Roberts, *Appl. Phys. Lett.* **24**, 49 (1974).

⁷M. J. H. van Dal, A. Lauwers, J. Cunniffe, R. Verbeeck, C. Vrancken, C. Demeurisse, T. Dao, Y. Tamminga, A. Veloso, J. A. Kittl, and K. Maex, *IEEE Trans. Electron Devices* **53**, 1180 (2006).

⁸S. M. Zhou, M. Hundhausen, T. Stark, L. Y. Chen, and L. Ley, *J. Vac. Sci. Technol. A* **17**, 144 (1999).

⁹G. Larrieu, E. Dubois, X. Wallart, X. Baie, and J. Katcki, *J. Appl. Phys.* **94**, 7801 (2003).

¹⁰R. T. P. Lee, K.-M. Tan, A. E.-J. Lim, T.-Y. Liow, G.-Q. Lo, G. Samudra, D. Z. Chi, and Y.-C. Yeo, in *Extended Abstracts of the International Conference on Solid State Devices and Materials (SSDM), 2006* (unpublished), pp. 1110–1111.

¹¹R. C. Weast, *CRC Handbook of Chemistry and Physics* 60th ed. (CRC, Boca Raton, FL, 1980), p. B-80.

¹²M. G. Grimaldi, L. Wielunski, M.-A. Nicolet, and K. N. Tu, *Thin Solid Films* **81**, 207 (1981).

¹³E. D. Marshall, C. S. Wu, C. S. Pai, D. M. Scott, and S. S. Lau, *Mater. Res. Soc. Symp. Proc.* **47**, 161 (1985).

¹⁴Y. F. Hsieh and L. J. Chen, *J. Appl. Phys.* **63**, 1177 (1988).

¹⁵H. B. Yao, C. C. Tan, S. L. Liew, C. T. Chua, C. K. Chua, R. Li, R. T. P. Lee, S. J. Lee, and D. Z. Chi, *Proceedings of the International Workshop on Junction Technology, 2006* (unpublished), pp. 164–169.

¹⁶R. Pretorius, *Thin Solid Films* **290-291**, 477 (1996).

¹⁷W. G. Jung and O. J. Kleppa, *J. Alloys Compd.* **176**, 301 (1991).

¹⁸E. Dubois and G. Larrieu, *J. Appl. Phys.* **96**, 729 (2004).