



**HAL**  
open science

## Spacer-first damascene-gate FinFET architecture featuring stringer-free integration

F. Cornu-Fruleux, Julien Penaud, Emmanuel Dubois, Philippe Coronel,  
Guilhem Larrieu, Thomas Skotnicki

► **To cite this version:**

F. Cornu-Fruleux, Julien Penaud, Emmanuel Dubois, Philippe Coronel, Guilhem Larrieu, et al..  
Spacer-first damascene-gate FinFET architecture featuring stringer-free integration. IEEE Electron  
Device Letters, 2007, 28, pp.523-526. 10.1109/LED.2007.897443 . hal-00255851

**HAL Id: hal-00255851**

**<https://hal.science/hal-00255851v1>**

Submitted on 18 Sep 2024

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

# Spacer-First Damascene-Gate FinFET Architecture Featuring Stringer-Free Integration

F. Cornu-Frulleux, J. Penaud, E. Dubois, P. Coronel, G. Larrieu, and T. Skotnicki

**Abstract**—This letter presents a new Damascene-gate FinFET process that inherently suppresses stringers, resulting from gate and spacers patterning. The so-called *spacer-first* integration scheme relies on the engineering of a hydrogen silsesquioxane layer by electron beam lithography followed by two selective compartmentalized development steps to successively release the Damascene-gate cavity and the source/drain (S/D) contact regions. In contrast to the existing *gate-first* and *gate-last* integration approaches, the resulting FinFET process does not impose any restriction or interdependency on the sizing of the fins, gate, spacers, and S/D regions. A complete morphological and electrical validation is proposed in the particular case of wrap-around self-aligned metallic Schottky S/D contacts.

**Index Terms**—FinFET, hydrogen silsesquioxane (HSQ), multiple gate, Schottky barrier.

## I. INTRODUCTION

IMPROVED electrostatics, superior current drive, and gates self-alignment constitute intrinsic advantages of the FinFET architecture over planar bulk [1]–[6]. However, technology has to face new challenges, resulting from the highly 3-D nature of the gate wrapping around fins. First, hard constraints are placed on reactive ion etching (RIE): Whatever the considered gate architecture (*gate-last* [1], *gate-first* [2], or *Damascene* [3]), effective stringer removal techniques still remain an unsolved challenge to eliminate dielectric or metallic residues [4], [5]. Second, the formation of spacers along the gate sides is even more critical because fins also inherit the same spacer structure in the source/drain (S/D) regions. In a general context for which FinFETs suffer from high series resistance due to a narrow fin section [6], this issue is exacerbated by the considerable reduction of the fin surface, offering bare silicon to subsequent epitaxial regrowth or silicidation [5]. In contrast, this letter presents a Damascene-gate FinFET process that inherently suppresses stringers, resulting from gate and spacers etching.

F. Cornu-Frulleux is with the Institut d'Electronique, de Microélectronique et de Nanotechnologie (IEMN), Department Institut Supérieur d'Electronique et du Numérique (ISEN), Centre National de la Recherche Scientifique (CNRS) 8520, 59652 Villeneuve d'Ascq, France, and also with STMicroelectronics, 38926 Crolles, France.

J. Penaud, E. Dubois, and G. Larrieu are with the Institut d'Electronique, de Microélectronique et de Nanotechnologie (IEMN), Department Institut Supérieur d'Electronique et du Numérique (ISEN), Centre National de la Recherche Scientifique (CNRS) 8520, 59652 Villeneuve d'Ascq, France.

It holds the following distinctive advantages over existing approaches: 1) the active fin channel is not exposed to RIE and associated damage; 2) wrap-around silicided fins S/D can abut on the gate spacer in a self-aligned manner; and 3) sophisticated stringer removal techniques by selective etching are not needed. This last advantage totally relaxes constraints associated to the FinFET design because restrictions and interdependencies on fins, gate, spacers, and S/D dimensions are *de facto* eliminated. From a practical standpoint, the proposed integration scheme relies on the engineering of a hydrogen silsesquioxane (HSQ) layer by electron beam lithography followed by two selective compartmentalized development steps to successively release the Damascene-gate cavity and the S/D contact regions. It constitutes the first demonstration of a *spacer-first* integration scheme. For the sake of electrical demonstration, this FinFET architecture also features wrap-around metallic Schottky S/D contacts.

## II. SPACER-FIRST STRINGER-FREE DAMASCENE GATE INTEGRATION

Fig. 1 gives a schematic illustration of the main steps of the FinFET fabrication sequence. Starting from a 50-nm-thick SOI substrate, fins are classically patterned by e-beam lithography and RIE. A gate dielectric is subsequently grown by dry oxidation at 725 °C, leading to a uniform 2.6-nm-thick SiO<sub>2</sub> oxide along the (110)-oriented sidewalls of the fins. The originality of the process relies on the appropriate use of two remarkable properties of HSQ. First, HSQ is an excellent flowable low- $\kappa$  dielectric that provides a planarized isolation matrix in which fins are inserted [Fig. 1(a)]. Second, HSQ is a high-resolution electron [7], [8] or a photosensitive [9] inorganic negative-tone resist that evolves from a cage-like monomer to a network-like polymer under irradiation. When exposed to e-beam or UV, HSQ approaches the structure of SiO<sub>x</sub>. This second property is used to define a peripheral SiO<sub>x</sub> spacer that demarcates the Damascene gate cavity [Fig. 1(b)]. It is worth noting that HSQ inside and outside the spacer pattern retains the original cage-like structure that can be removed selectively in a development solution. In Fig. 1(c), a hard mask of Ge is deposited onto the whole structure and opened in the extrinsic gate area using noncritical lithography and etching. The inner material of the Damascene cavity is subsequently developed using a highly selective tetramethylammonium hydroxide (TMAH) 25% solution [10]. Note that the outer part of the HSQ isolation matrix is not exposed to the developer because it remains isolated from the inner part by 1) the SiO<sub>x</sub> spacer and 2) the leak-proof top hard mask. Therefore, after selective hard mask stripping, the

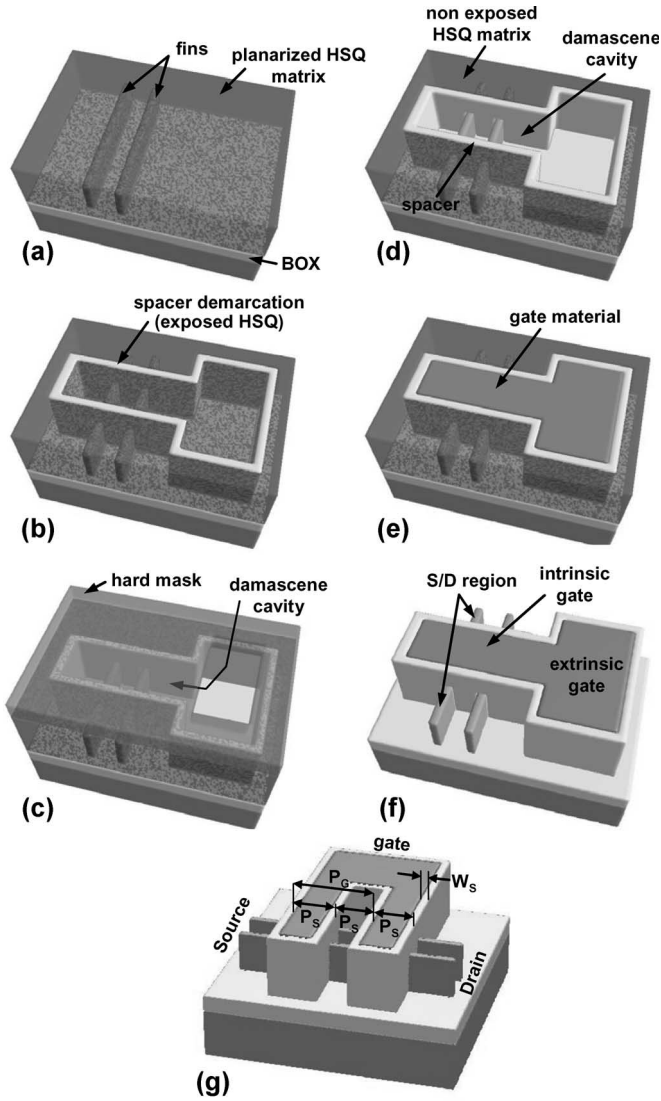


Fig. 1. Schematic illustration of the spacer-first stringer-free Damascene-gate FinFET. (a) Spin coating of a low- $\kappa$  dielectric (HSQ) to form a planarized isolation matrix in which silicon fins are inserted. (b) E-beam exposition of a narrow peripheral spacer that demarcates the Damascene gate cavity. (c) Deposition of a Ge hard mask followed by noncritical lithography and etching steps to open a window in the extrinsic gate region. The unexposed HSQ is removed from the Damascene cavity using the first compartmentalized development step in a highly selective TMAH solution. Note that the outer part of the HSQ isolation matrix is not exposed to the developer because it remains isolated from the inner part by the exposed HSQ spacer and the leak proof top hard mask. (d) Hard mask stripping. (e) Metal gate deposition (Cr) and planarization. (f) Second selective wet etching of the unexposed HSQ, leaving the S/D region free of dielectric stringers. (g) Schematic representation of a FinFET with two gate fingers, showing that the minimum gate pitch ( $P_G$ ) is twice the spacer pitch ( $P_S$ ), whereas the shortest gate length is given by  $P_S - W_S$ , where  $W_S$  is the minimum spacer width conditioned by the lithography resolution.

first compartmentalized development step leaves a Damascene cavity free of its original cage-structured HSQ [Fig. 1(d)]. The next steps consist of metal gate deposition and planarization by chemical mechanical polishing (CMP) [Fig. 1(e)]. At this stage of the process, the outer HSQ isolation matrix is submitted to a second compartmentalized development step in TMAH, which releases the S/D zones, leaving  $\text{SiO}_x$  (network-type HSQ) gate spacers unaltered and fins completely exempt of stringers on their sidewalls [Fig. 1(f)]. For the sake of morphological

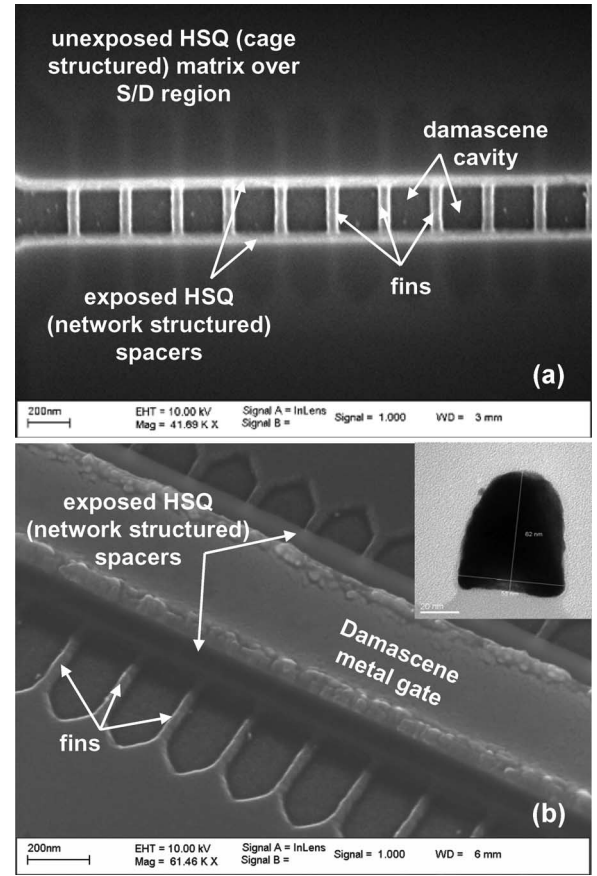


Fig. 2. Morphological validation of the proposed process. (a) SEM top view of the Damascene cavity after the first compartmentalized development step and hard mask removal, as schematized in Fig. 1(d). This demonstrates the feasibility of the dissolution of cage-structured HSQs in a low-volume cavity capped by a hard mask. Because the unexposed HSQ is developed in TMAH 25% with a contrast factor  $\gamma$  as high as 7 [10], this step leaves vertical and sharply defined cavity sidewalls corresponding to the gate spacers. Fig. 2(b) provides a tilted aerial view of the Damascene gate FinFET after the second compartmentalized development step that releases the S/D regions without producing any material residues along the fin sidewalls. In the case under study, chromium has been integrated as a gate material. Wrap-around low Schottky barrier metallic junctions have been considered as an attempt to address the issue of S/D resistance. PtSi, which offers a low Schottky barrier to holes ( $< 0.2$  eV), was selected for p-type MOSFET integration. PtSi formation is basically a two-step reaction ( $\text{Pt} \rightarrow \text{Pt}_2\text{Si} \rightarrow \text{PtSi}$ ). It requires the deposition of a well-controlled Pt overlayer that must be totally

validation of the process, Fig. 2(a) shows a scanning electron microscopy (SEM) top view of the Damascene cavity after the first compartmentalized development step and hard mask removal, as schematized in Fig. 1(d). This demonstrates the feasibility of the dissolution of cage-structured HSQs in a low-volume cavity capped by a hard mask. Because the unexposed HSQ is developed in TMAH 25% with a contrast factor  $\gamma$  as high as 7 [10], this step leaves vertical and sharply defined cavity sidewalls corresponding to the gate spacers. Fig. 2(b) provides a tilted aerial view of the Damascene gate FinFET after the second compartmentalized development step that releases the S/D regions without producing any material residues along the fin sidewalls. In the case under study, chromium has been integrated as a gate material. Wrap-around low Schottky barrier metallic junctions have been considered as an attempt to address the issue of S/D resistance. PtSi, which offers a low Schottky barrier to holes ( $< 0.2$  eV), was selected for p-type MOSFET integration. PtSi formation is basically a two-step reaction ( $\text{Pt} \rightarrow \text{Pt}_2\text{Si} \rightarrow \text{PtSi}$ ). It requires the deposition of a well-controlled Pt overlayer that must be totally

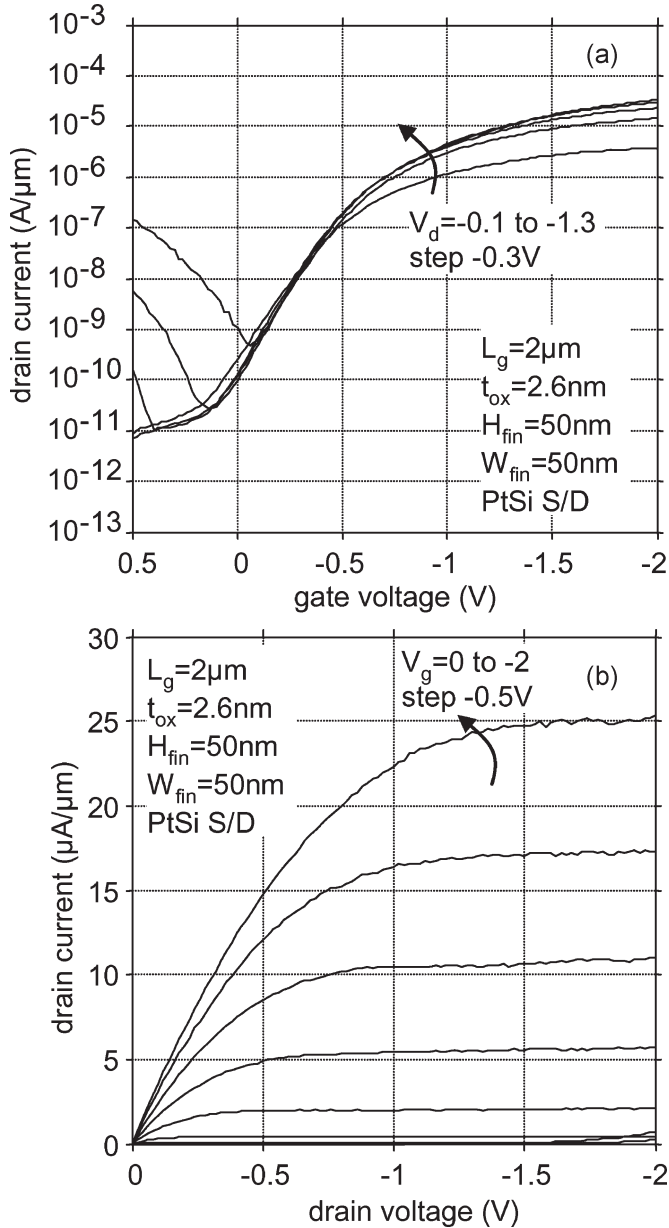


Fig. 3. Electrical validation of the spacer-first Damascene gate process with PtSi wrap-around Schottky contacts: p-type FinFET featuring  $L_g = 2 \mu\text{m}$ ,  $W_{\text{fin}} = 50 \text{ nm}$ , and  $H_{\text{fin}} = 50 \text{ nm}$ . (a)  $I_d$ - $V_g$  characteristic. (b)  $I_d$ - $V_d$  characteristic.

consumed by the silicidation reaction to effectively form PtSi, and not the Pt-rich phase. For that purpose, two 10-nm-thick evaporation steps with a  $\pm 30^\circ$  tilt angle were used to provide a tight control of Pt thickness and excellent step coverage on the fins. The silicidation reaction was activated by rapid thermal annealing at  $300^\circ\text{C}$  for 2 min under a forming gas ( $\text{N}_2 : \text{H}_2$ , 95 : 5). Unreacted Pt covering the gate and sidewall spacers was finally etched away using hot diluted aqua regia. The inset in Fig. 2(b) shows the rounded shape of the fin after full consumption of silicon induced by silicidation. The nonconventional nature of the proposed process calls for specific comments. First, it is worth noting that the footprint of the gate/spacers module depends critically on 1) the minimum spacer period  $P_S$  conditioned by the smallest lithography pitch and 2) the mini-

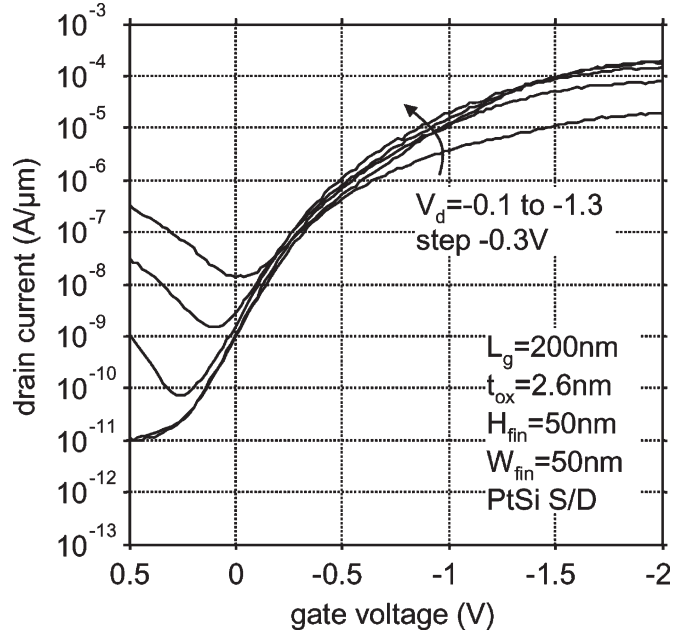


Fig. 4.  $I_d$ - $V_g$  characteristic of a Damascene gate p-type FinFET with PtSi wrap-around Schottky contacts.  $L_g = 200 \text{ nm}$ ,  $W_{\text{fin}} = 50 \text{ nm}$ , and  $H_{\text{fin}} = 50 \text{ nm}$ .  $I_{\text{ON}}$  reaches  $197 \mu\text{A}/\mu\text{m}$  at  $V_g = -2 \text{ V}$  and  $V_d = -1.3 \text{ V}$  under the definition of a channel width of  $2 * H_f + W_f$  or  $591 \mu\text{A}/\mu\text{m}$  when only the footprint  $W_f$  is considered.

um spacer width  $W_S$  that characterizes the ultimate resolution in HSQ [Fig. 1(g)]. Because the gate length is defined by the inner space between the two spacers, one direct consequence is that the minimum gate pitch  $P_G$  is twice the spacer pitch  $P_S$ , whereas the shortest gate length is limited to  $P_S - W_S$ . The previous requirements can be considered as extremely stringent constraints placed on lithography. However, progress in HSQ engineering is expected to alleviate this situation, demonstrating, for instance, 27-nm-period gratings at variable line width [8] and sub-8-nm resolution [7]. Second, although HSQ is a well-established material for interlayer dielectric isolation in the back-end of the line [11], [12], its impact on device performance and reliability still need to be consolidated when it is used as the spacer material.

### III. ELECTRICAL CHARACTERIZATION

Fig. 3 demonstrates the electrical functionality of a 2- $\mu\text{m}$ -long-channel p-type FinFET fabricated according to the present process. The fins' width  $W_f$  and height ( $H_f$ ) are both 50 nm. Fig. 4 presents the  $I_d$ - $V_g$  characteristic of a 200-nm-long device. In this case, the  $I_{\text{ON}}$  saturation current reaches  $197 \mu\text{A}/\mu\text{m}$  at  $V_g = -2 \text{ V}$ ,  $V_d = -1.3 \text{ V}$  under the definition of a channel width of  $2 * H_f + W_f$  or  $591 \mu\text{A}/\mu\text{m}$  when the footprint  $W_f$  is solely accounted for. Current observed in the positive  $V_g$  branch is typical of ambipolar operation in SB-MOSFETs. Although this effect slightly degrades the OFF-state current at large  $V_d$ , the  $I_{\text{ON}}/I_{\text{OFF}}$  ratio remains in excess of  $10^4$ . As far as PtSi Schottky S/D contacts characterized by weak lateral encroachment are considered,  $I_{\text{ON}}$  could be further improved by reducing the spacer width, which is currently set to 80 nm. Nevertheless, it is worth noting that the above  $I_{\text{ON}}$  figure compares well with previously published data [13], [14].

#### IV. CONCLUSION

A new *spacer-first* stringer-free Damascene gate process that inherently suppresses the issue of stringers formation has been demonstrated both from the morphological and electrical standpoints. The integration of wrap-around Schottky S/D junctions confirms effective stringer suppression along fin sidewalls and shows the feasibility of fully metallic S/D access. It is worth noting that the proposed process also offers an easy path for a 3-D massive and compact integration of nanowires. Starting from fins composed of alternated Si/SiGe layers, the formation of Si or SiGe nanowires can be realized at the cost of a single additional selective etch between Si and SiGe.

#### ACKNOWLEDGMENT

The authors would like to thank D. Delille from NXP for performing the transmission electron microscopy cross sections.

#### REFERENCES

- [1] X. Huang, W. C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y. K. Choi, K. Asano, V. Subramanian, T. J. King, J. Bokor, and C. Hu, "Sub-50 nm p-channel FinFET," *IEEE Trans. Electron Devices*, vol. 48, no. 5, pp. 880–886, May 2001.
- [2] Y. K. Choi, N. Lindert, P. Xuan, S. Tang, D. Ha, E. Anderson, T. J. King, J. Bokor, and C. Hu, "Sub-20 nm CMOS FinFET technologies," in *IEDM Tech. Dig.*, 2001, pp. 421–424.
- [3] C. W. Oh, S. D. Suk, Y. K. Lee, S. K. Sung, J. D. Choe, S. Y. Lee, D. U. Choi, K. H. Yeo, M. S. Kim, S. M. Kim, M. Li, S. H. Kim, E. J. Yoon, D. W. Kim, D. Park, K. Kim, and B. I. Ryu, "Damascene gate FinFET SONOS memory implemented on bulk silicon wafer," in *IEDM Tech. Dig.*, 2004, pp. 893–896.
- [4] J. Kedzierski, M. Jeong, E. Nowak, T. S. Kanarsky, Y. Zhang, R. Roy, D. Boyd, D. Fried, and H.-S. P. Wong, "Extension and source/drain design for high-performance FinFET devices," *IEEE Trans. Electron Devices*, vol. 50, no. 4, pp. 952–958, Apr. 2003.
- [5] A. Kanedo, A. Yagishita, K. Yahashi, T. Kubota, M. Omura, K. Matsuo, I. Mizushima, K. Okano, H. Kawasaki, S. Inaba, T. Izumida, T. Kanemura, N. Aoki, K. Ishimura, H. Ishiuchi, K. Suguro, K. Eguchi, and Y. Tsunashima, "Sidewall transfer process and selective gate sidewall spacer formation technology for sub-15 nm FinFET with elevated source/drain extension," in *IEDM Tech. Dig.*, 2005, pp. 844–847.
- [6] A. Dixit, A. Kottantharayil, N. Collaert, M. Goodwin, M. Jurczak, and K. De Meyer, "Analysis of the parasitics S/D resistance in multiple-gate FETs," *IEEE Trans. Electron Devices*, vol. 52, no. 6, pp. 1132–1140, Jun. 2005.
- [7] H. Namatsu, Y. Watanabe, K. Yamazaki, T. Yamaguchi, M. Nagase, Y. Ono, A. Fujiwara, and S. Horiguchi, "Fabrication of Si single-electron transistors with precise dimensions by electron-beam nanolithography," *J. Vac. Sci. Technol. B, Microelectron. Process. Phenom.*, vol. 21, no. 1, pp. 1–5, Jan. 2003.
- [8] M. J. Word, I. Adesida, and P. R. Berger, "Nanometer-period gratings in hydrogen silsesquioxane fabricated by electron beam lithography," *J. Vac. Sci. Technol. B, Microelectron. Process. Phenom.*, vol. 21, no. 6, pp. L12–L15, Nov. 2003.
- [9] M. Peucker, M. H. Lim, H. I. Smith, R. Morton, A. K. van Langen-Suurling, J. Romijn, E. W. J. M. van der Drift, and F. C. M. J. M. van Delft, "Hydrogen silsesquioxane, a high-resolution negative tone e-beam resist, investigated for its applicability in photon-based lithographies," *Microelectron. Eng.*, vol. 61/62, pp. 803–809, Jul. 2002.
- [10] F. Cornu-Frulleux, J. Penaud, E. Dubois, M. François, and M. Muller, "Optimisation of HSQ e-beam lithography for the patterning of FinFET transistors," *Microelectron. Eng.*, vol. 83, no. 4–9, pp. 776–779, Apr.–Sep. 2006.
- [11] H. J. Lee, E. K. Lin, H. Wang, W. Wu, W. Chen, and E. S. Moyer, "Structural comparison of hydrogen silsesquioxane based porous low-k thin films prepared with varying process conditions," *Chem. Mater.*, vol. 14, no. 4, pp. 1845–1852, 2002.
- [12] J. S. Jen and J. S. Chen, "Interdiffusions and reactions in Cu/TiN/Ti thermal SiO<sub>2</sub> and Cu/TiN/Ti/hydrogen silsesquioxane multilayer structures," *J. Electrochem. Soc.*, vol. 149, no. 8, pp. G455–G460, Aug. 2002.
- [13] H. C. Lin, M. F. Wang, F. J. Hou, H. N. Lin, C. Y. Lu, J. T. Liu, and T. Y. Huang, "High-performance p-channel Schottky-barrier SOI FinFET featuring self-aligned PtSi source/drain and electrical junction," *IEEE Electron Device Lett.*, vol. 24, no. 2, pp. 102–104, Feb. 2003.
- [14] B. Y. Tsui and C. P. Lin, "A novel 25 nm modified Schottky-barrier FinFET with high performance," *IEEE Electron Device Lett.*, vol. 25, no. 6, pp. 430–432, Jun. 2004.