Digital joint phase and sampling instant synchronisation for UMTS standard

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ABSTRACT

In asynchronous Direct-Sequence Code Division Multiple Access (DS-CDMA) receivers, one of the major functions is timing and phase synchronisation. Many proposed solutions treat these functions separately. In this paper we present a new joint synchronisation solution for UMTS standard. This solution is based on a digital delay and phase looked loops. In addition this implementation is programmable for the two modes of UMTS (FDD and TDD) with variable over-sampling factor. It has tested in real time on TigerSHARC DSP.

INTRODUCTION

In UMTS the communication system is asynchronous between mobile and base station. In addition the channel propagation effect, oscillator imperfections and other effects cause perturbation in received signal, which require synchronisation between base station and mobile. In UMTS standard synchronisation channels are transmitted to allow mobile to find base station location, cell's parameters and the beginning of the frame. This phase is named "acquisition", it's the first step that the mobile does, but this step gives an approximate synchronisation and it must be completed by a "tracking" synchronisation. This step "tracking" corrects the phase and the sampling instant continuously in time. This paper presents an implementation of digital joint tracking algorithm [1] for UMTS standard in real time.

UMTS

The access scheme is Direct-Sequence Code Division Multiple Access (DS-CDMA). And for radio access there's two modes, FDD (Frequency Division Duplex) and TDD (Time Division Duplex). In UMTS, a 10 ms radio frame is divided into 15 slots (2560 chip/slot at chip rate of 3.84 Mcps). A physical channel is therefore defined as a code (or number of a code used to spread this channel) and additionally in TDD mode the sequence of time slots is needed for the definition of a physical channel. The information rate of the channel varies with the symbol rate being derived from the 3.84 Mcps and the spreading factor (number of chips per symbol). Spreading factors (noted SF) are from 256 to 4 for FDD uplink, and from 512 to 4 for FDD downlink, and from 16 to 1 for TDD uplink and downlink. Thus the respective modulation symbol rates vary from 960 k symbols/s to 15 k symbols/s for FDD uplink (7.5 k symbols/s for downlink), and for TDD the momentary modulation symbol rates shall vary from 3.84 M symbols/s to 240 k symbols/s.

The used modulation scheme is QPSK with CDMA, the spreading (and scrambling) process is closely associated with modulation. So different families of spreading codes are used to spread the signal. In order to separate channels, codes derived from code tree structure are used. These codes are OVSF (orthogonal variable spreading factor). And for separating different cells in FDD mode Gold codes with 10 ms period (38400 chips at 3.84 Mcps) are used and for TDD mode we use codes with period of 16 chips and midamble sequences of different length depending on the environment.

In FDD mode a downlink fixed rate channel with predefined symbol (1+j) sequence is transmitted within each frame, this channel, named CPICH "common pilot channel", use the first spreading code in tree with spreading factor equal to 256. The proprieties of this channel allow the receiver to identify cell's location. In our work we have used this channel to carry out joint synchronization. In TDD mode each user slot has two data carrying parts separated by a "midamble" code bloc. We use this midamble code to carry out the estimation process.

DIJITAL JOINT SYNCHRONISATION ALGORITHM

The developed algorithm consists of four steps, as shown on figure (1), assuming that the baseband signal is obtained by radio frequency linear down conversion followed by a linear filtering system, and the "acquisition" is done correctly. The algorithm is composed of the following steps:

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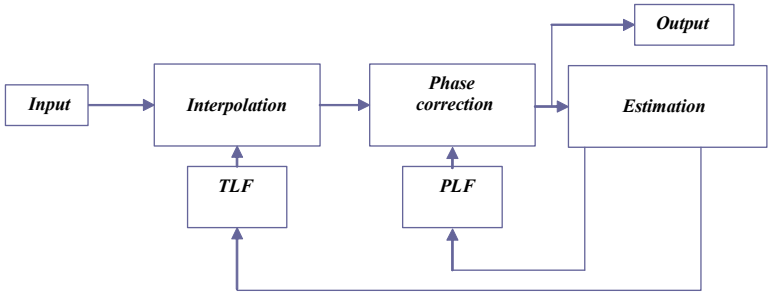

Figure 1: Tracking algorithm schema

1.Timing correction: We look to extract from the received samples the correct sample timing. To carry out this operation we interpolate the received signal by an adaptive linear FIR filters [2].
2.Phase correction: The second step is to correct the phase shift. The interpolated complex samples (I and Q) are multiplied by complex exponential of the estimated phase.
3. Joint estimation: The correction of the sampling instant and the phase require knowing time delay and phase shift. We developed an algorithm to estimate jointly and efficiently these parameters. Loop filters update the measurements.

Estimation for UMTS-FDD mode

The sampling instant delay and the phase shift are estimated over one symbol duration (256 chips). This estimation is used to correct the next symbol. We calculate the correlation in three points between corrected symbol and the sequence of scrambling code. From this calculation we obtain two parameters, which give us information about sampling instant delay and phase shift. These parameters are filtered in order to eliminate noise and to update them by using loop filters. The expressions for these parameters are:

$$\begin{cases} \Delta_{\varphi}(s) \cong 2\alpha(s) G_{cpich}\left[\varphi(s) - \hat{\varphi}(s)\right] + \eta_1(\varphi,\tau) \\ \Delta_{\tau}(s) \cong \dfrac{4\alpha(s) G_{cpich}}{OSF} \dfrac{\hat{\tau}(s) - \tau(s)}{T_e} + \eta_2(\varphi,\tau) \end{cases}$$

Where $\alpha(s)$ is the fading of propagation channel, $\hat{\tau}(s)$ is the estimation of the sampling instant delay, $\hat{\varphi}(s)$ is the estimation of phase shift, **s** denotes symbol's number, η_1 and η_2 are noise and G_{CPICH} is the gain of CPICH channel.

Estimation for UMTS-TDD

In this mode we process the received signal in a slot by slot manner (2560 chips). We have chosen this way because in the TDD mode we don't have a permanent channel with a known spreading code. In addition the TDD mode will be used in case of a good propagation channel conditions, that means we can consider the delay time and the phase shift are constant over slot duration. We use midamble code for estimation, so we calculate correlation function between the received midamble and the transmitted midamble in three points (aligned code, and with shifted code by +/-T_c/2). These measurements are filtered to estimate delay time and phase shift. Estimation of the sampling instant delay and the phase shift over actual slot is used to correct the next slot.

$$\begin{cases} \Delta_{\varphi}(s) \cong \alpha(s)\left(\varphi(s) - \hat{\varphi}(s)\right) + \eta_1(\varphi,\tau) \\ \Delta_{\tau}(s) \cong \dfrac{2\alpha(s)}{OSF} \dfrac{\hat{\tau}(s) - \tau(s)}{T_e} + \eta_2(\varphi,\tau) \end{cases}$$

These parameters are filtered and updated by a second order filters. The structure of these filters is the same as in the FDD mode. But the filters' coefficients are different due to gain, sampling frequency and updating time period. We study in the following section these loop filters.

***4.Early-late loop filter*:** the error $\Delta_{\tau}(s)$ is filtered by a second order filter with λ_1 and λ_2 as coefficients. μ_s is used to determine the interpolator impulse response : $h_s(i) = \sin c\left((i + \mu_s) \cdot T_e\right)$.

The updated interpolation filter is used to correct the sampling instant error for the next symbol (in FDD) or next slot (in TDD). The time delay loop filter is adapted by the following equations:

$$\mu_{s+1} = \mu_s + \varepsilon_s + \lambda_1 \Delta_\tau(s)$$
$$\varepsilon_{s+1} = \varepsilon_s + \lambda_2 \Delta_\tau(s)$$

We look for satisfying three conditions: system stability, speed response system and minimal variance (the residual error after convergence must be minimal). The close loop equations concluded to determine the stability region and the optimized filter coefficients :

For FDD mode: $\lambda_1 = \dfrac{0.15 \times OSF}{G_{CPICH}}$ and $\lambda_1 = \dfrac{0.05 \times OSF}{G_{CPICH}}$

For TDD mode: $\lambda_1 = 0.3 \times OSF$ and $\lambda_1 = 0.1 \times OSF$

5. Phase loop filters **:** The error $\Delta_\varphi(s)$ is filtered by a second order filter with γ_1 and γ_2 as coefficients. The output of the filter is used to correct the phase by complex multiplication. The phase is updated and corrected with the same proceeding as interpolation. The following equations show how a phase loop filter updates the phase:

$$\phi_{s+1} = \phi_s + \delta_s + \gamma_1 \Delta_\varphi(s)$$
$$\delta_{s+1} = \delta_s + \gamma_2 \Delta_\varphi(s)$$

For FDD mode: $\delta_1 = \dfrac{0.3}{G_{CPICH}}$ and $\delta_2 = \dfrac{0.1}{G_{CPICH}}$

For TDD mode: $\delta_1 = 0.6$ and $\delta_2 = 0.2$

COMPLEXITY STUDY

We have obtained the number of cycles required for every function and the global number of cycles required for tracking.

		Interpolation	*Phase correction*	*Correlation*	*Estimation*	*Total cycles*	*Time duration*
FDD mode	*OSF=2*	***51420 cycles***	***10480 cycles***	***31030 cycles***	***147 cycles***	***93077 cycles***	***372.31 µs***
	OSF=4	***51460 cycles***	***20740 cycles***	***31030 cycles***	***169 cycles***	***103399 cycles***	***413.60 µs***
	OSF=8	***102620 cycles***	***41140 cycles***	***15660 cycles***	***169 cycles***	***159589 cycles***	***638.36 µs***
TDD mode	*OSF=2*	***51224 cycles***	***10265 cycles***	***6186 cycles***	***132 cycles***	***67807 cycles***	***271.23 µs***
	OSF=4	***51226 cycles***	***20505 cycles***	***15390 cycles***	***132 cycles***	***87253 cycles***	***349.01 µs***
	OSF=8	***102450 cycles***	***41010 cycles***	***15390 cycles***	***132 cycles***	***158982 cycles***	***635.93 µS***

The criteria are to assure real time processing. All the parameters are shown in table (1), where we process the incoming signal in a slot by slot manner. The time duration of one slot is T_{slot} ***=666.667 µs***. The DSP clock period is T_{cycle} ***=4 ns***..The results are obtained for the two mode (TDD and FDD) and for different values of over sampling factors. As a conclusion, the real time processing is assured for all over sampling factors, but for OSF=8 the time is still critical.

IMPLEMENTATION RESULTS

The following figures show constellations of received CPICH channel and data channel in FDD mode and data channel in TDD mode. Simulation conditions are :
Delay function is linear with 100 ppm (10^{-4} T_e of drift per sample duration).
Phase shift: 194 radium/s.
Doppler frequency 220 Hz which corresponds to 120 km/h.

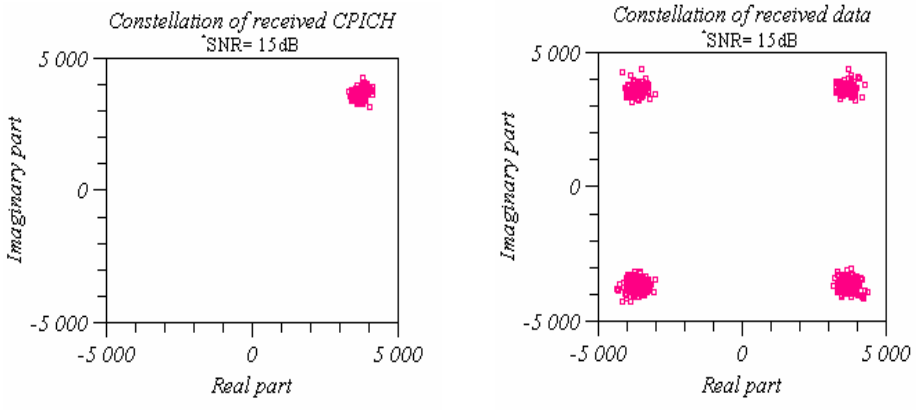

Figure 2: Constellation of CPICH and data in FDD mode

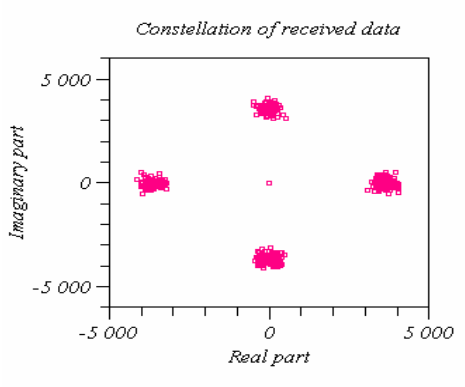

Figure 3: Constellation of received data in TDD mode

CONCLUSION

In this paper, joint chip timing and phase synchronization for reconfigurable standard UMTS was introduced. This algorithm was validated by simulation and implemented on 16-bit fixed-point arithmetic on DSP TigerSHARC. Simulation was carried out in many configurations to assure real time processing and to assure also the reconfigurability of the system. Implementation results also are presented .

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