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Qualification of Behavioral Level Design Validation for AMS & RF SoCs

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Abstract

The expansion of Wireless Systems-on-Chip leads to a rapid development of design and manufacturing methods. In this paper, the test vectors used for design validation of AMS & RF SoCs are evaluated and optimized. This qualification is based on a fault injection method. A fault model based on variation of behavioral parameters and a related qualification metric are proposed. This approach is used in the receiver's design of a WCDMA transceiver. A test set defined by verification engineers during the validation of this system is qualified and optimized. Then, this test set is compared with a second test set automatically generated by a developed tool.

Keys words: Test Qualification, characterization, design validation, AMS & RF SoCs, VHDL-AMS, behavioral modeling, fault injection.

1 Introduction

Telecommunication and multimedia electronic products integrate more and more complex Integrated Circuits (IC). Nowadays these complex ICs often called Systems-on-Chip (SoCs) embed both Analog and Mixed Signal (AMS) and RadioFrequency (RF) components. This increasing complexity and the hybrid nature of the AMS & RF SoCs involve the use of Top-Down design and verification flow. This approach permits to achieve first time right design of SoC. A challenge for the system design verification is to ensure that all system functionalities are verified. Further in the flow, all electrical parameters of embedded analog components must also be verified. In addition, hybrid nature of IC imposes SoC designers to use methods adapted for both digital, analog and radiofrequencies systems. Design validation and verification concern different abstraction levels of the design flow. [1] proposes an approach to generate and to validate the architecture of an RF transceiver described at functional level. In [1], the authors use known classical validation test benches (ie BER, Bit Error Rate, or EVM, Error Vector Magnitude...), as specified by telecommunication standards, which are assumed to be exhaustive enough for the complete validation of the design. The problem of the qualification of these test benches with low level abstraction descriptions is that it involves long time to simulate the system. In addition, the reuse of this approach for manufacturing test is very expensive.

A system verification with transistor level descriptions is presented in [2]. In this article, a formal verification method based on the extraction of parameters is developed. The verification is realized comparing the behavior of an extracted model with the specifications. This method is efficient because formal proof allows an exhaustive validation but the extraction of formal model from structural description is complex for the validation of large systems. [3] presents a verification method using behavioral level descriptions. The system is modeled with an HDL-A language and a code coverage metric is used for the qualification of the test set. This paper shows that code coverage metric is not enough for the verification and adds a frequency coverage metric. This method is interesting for the verification of the systems which could be described with a transfer function but it becomes too much complex for the validation of SoC. In [4], faults are injected on process parameters and then the induced behavioral parameters are extracted. In [5], faults are directly injected on behavioral parameters. Then, efficiency of multi tones signal to distinguish faulty and fault-free descriptions is evaluated. In this work, system specifications (i.e. expected output signal for a specified input signal) are considered as a reference. Relationships between specifications and measurements are computed and estimated. Comparison between behavioral simulation results and results computed from regressive estimations (MARS) allows to determine few optimized multi tone signals (magnitude and frequency). Both approaches [4, 5] generate vectors by using behavioral level descriptions, but they become too much time consuming when applied on complex systems. In this article, a new qualification tool is proposed to qualify the validation test sets used for AMS and RF SoC. Our PLAtform for the qualification of Systems with Mixed and Analog signals (PLASMA) is first detailed in section 2 and 3. Then, the receiver part of WCDMA system we used to carry out experimental results is presented in section 4. Then, the fault models are discussed in section 5. The principle of fault injection is developed in part 6. Experimental results on WCDMA receiver are exposed in the last section with a reduction of validation test sets and a comparison with an automatically generated test set.

2 Qualification of AMS & RF SoC Verification

In Top-Down design flow, the system is first described at functional level. Then, several successive refinement steps allow modeling the system at lower abstraction levels. At each step, simulations performed with test vectors defined by designers allow to verify the new description. This validation is achieved by comparing the simulation results of the next lower-level description with previously developed higher-level descriptions. Most of design faults due to bad choices of architecture or wrong parameters definitions should be detected using these simulations.

Some stimuli developed for the validation of high-level descriptions could not be applied for the validation of a lower level description because simulations become too time consuming. For example, a BER simulation using a lot of random input data cannot always be performed on a transistor level SoC description. Thus, efforts are required to minimize and to simplify these test cases. But how to be sure that all possible design faults are always detected after simplification?

Our approach for qualifying vectors is based on the classical fault injection technique [6, 7, 8]. Several faulty versions of the original description of the system under verification are created. Each faulty description contains only one fault. Test cases are used to stimulate these faulty descriptions with the goal of distinguishing the faulty programs from the original program. A faulty description is detected, when a test vector activates and propagates the induced fault toward an observable output. However, it is important to note that this test cases analysis does not achieve system verification, but only evaluates the quality of test vectors.

The choice of the abstraction level of the original description must be adapted for the verification of AMS and RF SoCs. In one hand, the use of a functional description is not possible to qualify test sets because this description does not make use of electrical parameters and so does not guarantee the validation of these parameters. On the other hand, the use of component level SoC description is impossible because the simulation time to qualify the test set is in this case too large. A trade off between these two abstraction levels is to use descriptions at the behavioral level. A few studies on behavioral modeling of RF transceiver have already been developing. For example, in [9], a BPSK transceiver has been modeling with the VHDL-AMS language. The accuracy of this model has been validated by comparing its simulation results with component level simulation results.

3 WCDMA transceiver

Our test sets qualification and optimization tool (PLASMA) has been experimented on an AMS and RF SoC. This SoC has been designed and manufactured by ST MICROELECTRONICS [10]. It is an integrated WCDMA

(Wideband Code Division Multiple Access) transceiver. This device has been developed in a 0.25 μ m BiCMOS technology. The complexity of this SoC is representative of current industrial realizations. As the simulation of the complete system at the transistor level is very time consuming; an approach based on the simulations of behavioral level descriptions is needed.

3.1 Brief presentation of WCDMA

The studied system is the receiver part of a WCDMA (Wideband Code Divided Multiple Access) transceiver. WCDMA is a technology used for third-generation cellular systems (3G). The frequency range down-link (Bases Station to User Equipment) or receiver part is [2110-2170MHz]. The modulation defined in the WCDMA standard is an IQ modulation based on two signals: I "in-phase" component of the waveform, and "Q" represents the quadrature component. WCDMA standard specifies several parameters: maximal and minimal output power, maximal power out of frequency band, ACLR (Adjacent ChaneL Leakage Ratio)...

3.2 Architecture definition

In this section, the architecture of the receiver part is presented. This architecture and the related blocks specifications will allow us to define the fault models.

The system has been designed using a Top-Down flow [10]. First, the architecture has been chosen. Then, the system has been divided into several blocks. The parameters of each block have been fixed in order to fit the system specifications. During these steps, the system has been modeled at different abstraction levels: functional, behavioral, and structural levels. In the following, only the behavioral level is used to qualify the test sets.

The architecture of the receiver part is a Zero Intermediate Frequency (Zero-IF) Wireless Radio architecture (*Fig. 1*). It only employs one stage to down-convert the RF signal directly to the desired base-band signal.

The figure 1 presents the architecture of the receiver part (Rx). It is a classical architecture made of Low Noise Amplifier (LNA), external Surface Acoustic Wave (SAW) RF filter, mixers, base-band Voltage Gain Amplifiers (VGA) and internal filters. Digital registers (not illustrated in *Fig. 1*) control the LNA and VGA gains. These registers permit to control the receiver parameters; they can be used to control the system during validation.

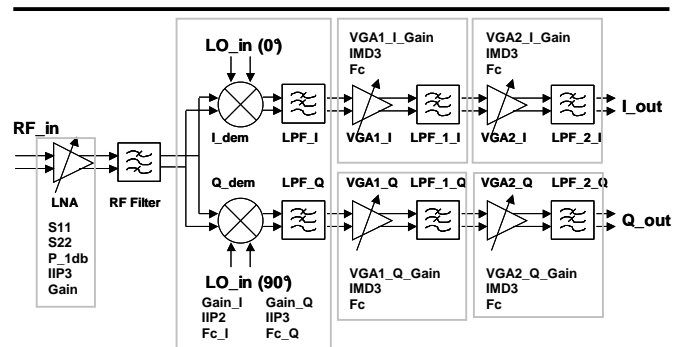


Fig. 1: WCDMA Receiver Part (RX)

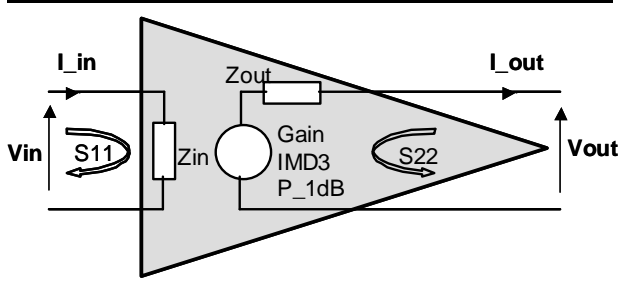


Fig. 2: Amplifier model.

3.3 Amplifier behavioral model

The amplifier behavioral model is presented in order to illustrate with one example this level of modeling. Amplifier functional and electrical parameters are also defined.

The amplifier model is made of one functional parameter, the power gain (Gain), and several electrical parameters: input and output impedances (Z_{in} , Z_{out}), S parameters (S_{11} , S_{22}), compression point at 1dB (P_{1dB}), third-order intermodulation distortion (IMD3). Figure 2 presents the model of the amplifier with its functional and electrical parameters. The table 1 specifies the limits of several parameters. Each parameter is defined by a typical value and with one or two worst-case values (minimum and/or maximum admitted values). In Tab. 1, the gain is specified by two limits because both limits are critical; the other parameters have only one critical limit.

The other blocks of the system are modeled in the same way plus additional parameters: IIP2 (Second-Order Intermodulation Distortion), DC offset, and cut off frequency. The figure 1 gives the modeled parameters of each block. Finally, the receiver part is modeled by 23 functional and electrical parameters (Fig. 1). These parameters are critical parameters in the system design. Obviously, our qualification process could be applied on a description involving additional parameters. This case study with 23 parameters will allow us to estimate the computation time required by this method. The WCDMA transceiver is modeled with VHDL-AMS an hardware description language [10]. The simulations are realized with the Mentor Graphics simulator's ADvance MS RF. The Mentor Graphics behavioral VHDL-AMS library's CommLib RF [11] is used for the modeling.

4 Fault model definition

The definition of the fault model is a crucial point of our approach because it is directly linked to the accuracy of the

Parameters	Typical Value	Minimum	Maximum
S_{11}	-12dB	Not Specified	-10dB
S_{22}	-10dB	Not Specified	-8dB
Gain	15dB	14dB	16dB
IMD3	1dB	-1dB	Not Specified
P_{1dB}	-9dB	-12dB	Not Specified

Tab. 1: Limits of a few amplifier parameters

test set qualification. Due to the choice of mutation-based fault injection, data contained in the original description or choice of modeled parameters are essential. In our fault model, only small modifications of the original description are considered. That means that we assume that wrong parameters values when they exist are not too far to their tolerance ranges. Moreover, we assume that if the test set is able to detect these small parameters variations then it is also able to detect larger variations. In addition, it is also assumed that multiple faults would be more detectable than single ones so only single faults are injected. During the Top-Down design flow, the behavioral level description is developed before transistor level description. The physical level does not already exist and correlations could not yet be extracted. Therefore, correlations between behavioral parameters are not taking into account in this paper.

During the development of the SoC, designers specify blocks parameters (local parameters) with typical, maximum and minimum values (Tab. 1). Then, the aim of the design validation is to verify that these local specifications satisfy global system specifications. Thus, we will verify that validation test set detects the variation of local parameters outside of their specified ranges. So, it seems possible to set the local parameter value just across its limits and then to compare simulation results with specifications of the SoC. But due to the natural desired analog system robustness, such small variations should have no effect on the global specification of the SoC and then, the closer the parameter value is to the limit; the more difficult is the mutant detection.

The mutants are created by translating one parameter of the original description to a value outside of its specifications. In [4, 12], faults are injected on physical parameters and their faulty values are fixed at a percentage of the typical value: for example in [12], 50% of the typical value. This approach may mislead the test qualification because this fault could be hard to detect in some cases or easy to detect in other cases. Hence, in our approach, to avoid this problem, the value of the faulty parameter is computed starting from tolerance ranges. The limit value of detection is obtained with the use of a dichotomy algorithm (Fig. 3). The initial faulty parameter value is computed using tolerance ranges (i.e. minimal and maximal specified values); an exploration range is first specified. The maximal accepted value P_{max_fault} is equals to 25 times the tolerance range: $P_{max_fault} = P_{max} + 25.(P_{max} - P_{typ})$ where P_{max} is the high limit value (Fig. 3). The initial faulty parameter value of a mutant is specified at the middle of $[P_{max}, P_{max_fault}]$ range. This faulty value depends on both its tolerance range ($P_{max} - P_{typ}$) and its maximal value P_{max_fault} . If this mutant is detected, the next faulty value is brought closer to P_{max} . On the other case, it is moved away. The detection limit is

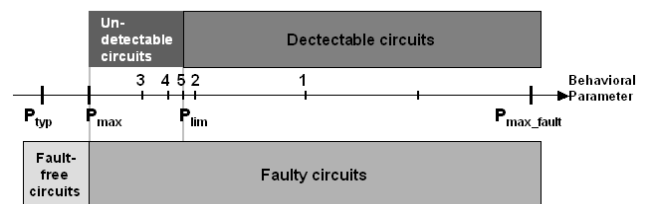


Fig. 3: Definition of faulty value

iteratively computed by simulating several faulty parameter values. The dichotomy algorithm is iterated 5 times and determines a good estimation of the detection limit P_{lim} . The injected faulty value is linked to the test quality: the higher the test quality is, the closer to the limits induced faults must be detected.

This detection limit is computed for every mutated parameter and every qualified vector. Relative Parametric Coverage (RPC) qualifies the detection limit; RPC is defined in Eq. 1.

$$RPC_{PL1} = 1 - \frac{(P_{fault_{PL1}} - P_{max_{PL1}})}{P_{max_{fault_{PL1}}} - P_{max_{PL1}}} \quad (1)$$

When the detection limit is equal to the specification limit, the RPC is 100%. The farther this detection limit is from the specification limit, the lower is the RPC. The test set optimization is realized by saving the vector that leads the highest RPC.

The total relative parametric coverage RPC is the average of all behavioral parameters relative parametric coverage RPC_{PLx} .

5 Fault injection and simulation

Fault injection and fault simulation are used to qualify test set. The principle of the fault simulation relies on the comparison of the simulation results (Fig. 4). Faulty and fault-free models are simulated with the same input vectors. When the comparison of simulation results involves a difference, the fault has been both activated and observed. Fault-free and faulty circuits are simulated with pre-defined test sets. The faulty values of detected and undetected mutants are modified as presented in part 4 and circuits are re-simulated with the same test sets. The simulation is realized 5 times and permits to determine a faulty value close to the limit of detection. Then, the total RPC is computed in order to qualify the test set. In addition, the test set optimization is also possible. This optimization can be done by keeping only vectors that make observable at least one fault and induced the maximal RPC.

In Fig. 4, the simulation results of faulty models are compared with several fault-free models simulation results. The use of several fault-free simulation results permits to

obtain a simulation results range representative of fault-free models. The choice of several fault-free models will be justified in part 5.2.

5.1 Faulty models

Faulty models or mutants are created from fault-free model. The mutant is generated by modifying the value of a behavioral parameter. The number of faulty models is imposed by the number of behavioral parameters. When a parameter is specified by two limits (for example, the gain in Tab. 1), two mutants are generated: a first for the low limit and a second for the high limit; when it is specified by one limit (ex: IMD3), only one mutant is generated. Due to this consideration, the receiver part of WCDMA SoC modeled by 23 behavioral parameters involves the generation of 36 faulty models. All faulty models simulation results are compared with fault-free models simulation results. This comparison determines the ability of the test vectors to detect the behavioral faults.

5.2 Computation of the fault-free models

Faults detection is based on the comparison between faulty models and fault-free models. In fact, analog circuit fault simulations could not be compared to only one "typical model". Typical model means a fault-free model made of behavioral parameters fixed at their typical value. Although this model has the best probability to be manufactured, other fault-free models instanced with parameters inside of their specification ranges also have to be considered in order to obtain the realistic ranges of fault-free simulation results. Finally, these measurement ranges are the references for the mutant detection.

Obviously, it is impossible to simulate all fault-free models because the variations of each parameter involve an infinite number of possible fault-free models. Therefore, a direct and simple approach to define fault-free ranges is to sample the fault-free population. The samples set must represent an accurate estimation of the real fault-free models population. The number of samples increases the simulation time for the vectors qualification. Thus, a trade off between accuracy and number of fault-free models has to be made. The fault-free sample set is generally generated with two main approaches:

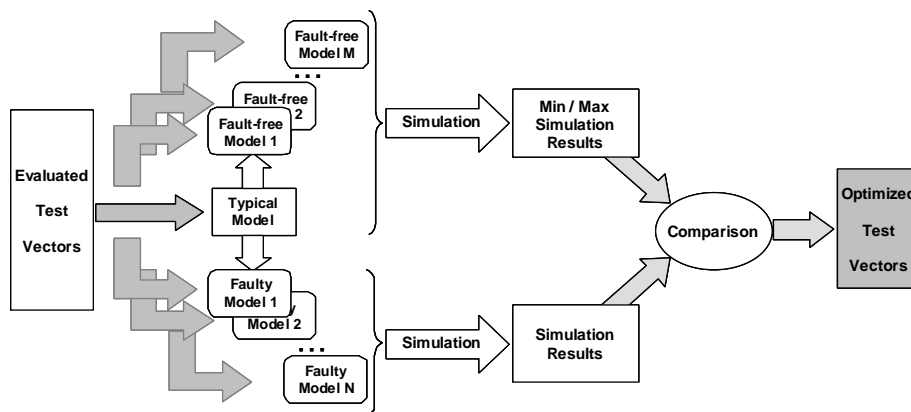


Fig.4: Test vector qualification & optimization

- *Random sampling* approach as in the Monte Carlo analysis [12, 13]. Instances of the fault-free circuit are generated randomly choosing parameters in the specifications ranges.
- *Worst-case min-max* approach [14]. Only worst-case fault-free models are selected. All parameters are fixed to their minimal or maximal values.

Our test vector qualification method has been developed for the validation of complex systems. The number of fault-free models required by the random sampling approach depends on the total number of parameters and the desired accuracy. In our case, the RX part modeled at behavioral level could be described with 23 parameters. Thus, this random approach leads to the use of an unacceptable number of fault-free models. With the second method, the number of worst-case possibilities is $2^{23} \approx 8$ millions. So, it is also impossible to simulate all worst-case combinations.

In our case, fault-free models are defined using the statistical distributions of behavioral parameters. Then, the statistical parameters of the simulation results can be extracted. Generally, Gaussian estimation is done thanks to Monte Carlo analysis but this method requires the simulation of many samples to be accurate enough. In PLASMA, the number of fault free simulated models is decreased by analyzing the statistical characteristics of the results: i.e. the average (μ) and the standard deviation (σ) of fault-free simulation results. The number of fault free simulated models is increased as long as μ and σ variations are not negligible. Then, the fault free measurement ranges can be determined by defining the limits at 6σ .

6 Experimental Results

This approach has been applied to the WCDMA receiver part. A list of test vectors has been manually generated to validate the design in its operating range. PLASMA tool will identify the useful vectors and reject redundant vectors. First, fault-free models and mutants are simulated with the pre-defined vectors. Only the vectors that detect the mutated parameters are saved. Then, the RPC obtain with this initial test set is compared with a second RPC obtained by the simulation of test set automatically generated.

	Frequency	Power
RF	2113.4 MHz	-60dBm
RX LO	2112.4 MHz	-7dBm

Tab. 2 A: Two tones input signal parameters

LNA Gain	-15dB
VGA1 Gain I	-10dB
VGA1 Gain Q	-10dB
VGA2 Gain I	23dB
VGA2 Gain I	23dB

Tab. 2 B: WCDMA Receiver part configuration

6.1 Test sets

During the design of the WCDMA system, a list of test vectors has been defined for its validation. These vectors aim to validate system specifications within different configurations (Gain, Offset) and with different input signals (frequency, power). They should verify the values of the programmable gains, the IMD3, the IMD2... The validation test set is made of vectors with single tone or bi-tone signals on RF and RX Local Oscillator (LO) inputs; one example of test vector parameters is given in Tab. 2. Tab. 2A describes RF input signal whereas Tab. 2B gives receiver gains configuration controlled thanks to digital registered inputs. In a first stage, designers define simple vectors to validate the design (mainly single tone). If the validation is not achieved, more complex vectors will be used. In this paper, we verify behavioral parameters with only single tone vectors.

In the following experimental results, a test set made of 80 single tone vectors are be evaluated. PLASMA will analyze these test benches and are identify the useful vectors and reject redundant vectors.

In a second part, a test set automatically generated by PLASMA is qualified. During the generation of this second test set, only single tone vectors are generated and the values of frequency and magnitude are randomly defined. These values are selected into the model validity domain. The test sets are evaluated by comparing total relative parametric coverage.

6.2 Simulation results

80 vectors have been evaluated with 37 fault-free models and 36 faulty models. These vectors manually defined aim to measure the RX Gains for the numerous possible gain configurations. These vectors have been defined to validate the RX behavioral model in its operating range only.

The simulation has been realized with ADMS RF from Mentor Graphics on 3 GHz Pentium-4, with 1 GB RAM, running a Linux Operating System. Over 36 mutated parameters, 28 have been detected during the entire dichotomy process. The total computation time is about 15 hours. For this sample of test data, the total Relative Parametric Coverage FC previously defined in section 4 is 68% (Tab. 3).

Mutants which have not been detected are mutants with faults injected on non-linearity parameters (compression point, IIP2, IIP3). In fact, the non-linearity parameters cannot be detected by using small power input signals specified by the operating range. These parameters can have an effect only when a block works in its saturation range. In addition, only a few variations on filters' cut off frequencies are detected. Indeed, for all vectors, the deviation between RF signal frequency and RX LO signal frequency is lower than filters' cut off frequencies. So, the increase of cut off frequency value can never be detected. However, decrease of cut off frequency value can be detected but only for high variations.

Each vector of the 80 vectors detects a least one behavioral faulty parameter but after compaction, only 4 vectors are kept to achieve the same RPC. After compaction, the number of stimuli is divided by 20 (Tab. 3).

	Validation test set manually defined	Automatically generated test set
Number of initial vectors	80	20
Mutation score	28/36=0.77	34/36=0.94
Relative Parametric Coverage	0.68	0.90

Tab. 3: Qualification results

In a second step, the test set automatically generated has been evaluated. Over 36 mutants, 34 mutants have been detected. It takes only about 4 hours to generate these test vectors and to perform their evaluation. This duration is lower than the previous one because there are only 20 vectors to evaluate. The relative parametric coverage of this test set is 90.1%. This FC is better than the previous one because the input signal parameters are selected in a large range corresponding to the model validity domain. In opposition with previous test vectors included in the operating range, with this large range, mutants induced on cut off frequencies and non-linearity parameters can be detected. However, the simulation of the system in its saturation range can be problematic because some mutants could be masked. In fact, in that case, variations induced on LNA parameters as coefficient reflection (S_{22}) and variations induced on amplifier non-linearity are not detected because their impact on system behavior is hidden.

7 Conclusion

A method and a tool (PLASMA) for the qualification of test vectors have been presented in this paper. The method is based on faults injection and simulation. A behavioral fault model relying on the mutation approach has been defined. The different descriptions (faulty and fault-free models) are automatically instantiated by PLASMA. The classification of vectors is realized by comparing simulation results of faulty descriptions with fault-free descriptions. The main advantage of our method is to evaluate complex systems by considering behavioral faults. A relative parametric coverage metric based on faulty parameters value gives a measure of test quality. This measure allows designers to complete their test vectors.

First, manually predefined test set chosen for the design validation of AMS & RF SoCs is qualified. In a second step, a test set automatically generated by the developed tool is also evaluated and compared with previous results. Simulation results show that an optimized test set can be rapidly generated and reach better performances than the initial manually generated test bench.

8 References:

[1] S. Vitali, D. Laurentiis, N. Albertazzi, G. Agnelli, F. Rovatti, "Multi-standard simulation of WLAN/UMTS/GSM transceivers for analog front-end validation and design", ISWCS'04, pp 16- 20, 2004.

- [2] A. Ghosh, R. Vemuri, "Formal Verification of Synthesized Analog Designs," IEEE International Conference on Computer Design (ICCD'99), p. 40, 1999.
- [3] Yuan-Bin Sha; Mu-Shun Lee; Chien-Nan Jimmy Liu, "On code coverage measurement for Verilog-A" High-Level Design Validation and Test Workshop, pp 115 – 120, 2004.
- [4] F. Liu, S. Ozev, "Fast Hierarchical Process Variability Analysis and Parametric Test Development for Analog/RF Circuits", International Conference on Computer Design (ICCD '05), pp. 161-170, 2005.
- [5] A. Halder, S. Bhattacharya, A. Chatterjee, "Automatic Multitone Alternate Test Generation For RF Circuits Using Behavioral Models," International Test Conference 2003 itc03, p. 665, 2003.
- [6] G. Al-Hayek, C. Robach, "From Design Validation to Hardware Testing: a Unified Approach", Journal of Electronic Testing : theory and application 14, pp 133-140, 1999.
- [7] A.J. Offutt, R.H. Untch, "Mutation 2000: Uniting the Orthogonal", Mutation 2000: Mutation Testing in the Twentieth and the Twenty First Centuries, pages 45--55, San Jose, CA, October 2000.
- [8] B.Charlot, S.Mir, E.F.Cota, M.Lubaszewski, B.Courtois, "Fault modeling of suspended thermal MEMS" IEEE International Test Conference (ITC'99), USA, 28-30 , pp. 319-328, 1999.
- [9] E. Normark, L. Yang, C. Wakayama, P. Nikitin, R. Shi, "VHDL-AMS behavioral modeling and simulation of a Pi/4 DQPSK transceiver system", Behavioral Modeling and Simulation Conference, 2004. BMAS 2004. Proceedings of the 2004 IEEE International Issue pp 119 - 124, 2004.
- [10] Y. Joannon, V. Beroulle, R. Khouri, C. Robach, S. Tedjini, J-L. Carbonero, "Behavioral modeling of WCDMA transceiver with VHDL-AMS language", Design and Diagnostics of Electronic Circuits and Systems (DDECS'06), pp. 113-118, 2006.
- [11] MENTOR GRAPHICS, "CommLib RF VHDL-AMS Library", Manual, October 2005.
- [12] A. Khouas, A. Derieux, "Methodology for Fast and Accurate Analog Production Test Optimization", 5th IEEE International Mixed Signal Testing Workshop (IMSTW'99), pp. 215-219, 1999.
- [13] K. Saab, N. Ben-Hamida, B. Kaminska, "Parametric Fault Simulation and Test Vector Generation", Design Automation and Test in Europe (DATE '00), p. 650, 2000.
- [14] M.W. Tian and C. J. Shi, "Worst Case Tolerance Analysis of Linear Analog Circuits using Sensitivity Bands", IEEE Transactions on Circuits and Systems - I: Fundamental Theory and Applications, vol. 47, n. 8, pp. 1138–1145, 2000.