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# Using of Behavioral level AMS & RF Simulation for Validation Test set Optimization

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## Abstract

*The expansion of Wireless Systems-on-Chip leads to a rapid development of new design and test methods. In this paper, the test benches defined for design validation or characterization of AMS & RF SoCs are first optimized and then re-used for production testing. Although the original validation test set allows the verification of both design functionalities and performances, this test set is not well adapted to manufacturing test due to its high execution time and high test equipments costs requirement. The optimization of this validation set is based on the evaluation of each test stimuli. This evaluation relies on a high level faults simulation method. Hence, a fault model based on the variations of behavioral parameters and its related qualification metric are presented. This approach is used on the receiver part of a WCDMA transceiver. The test bench optimization realized is evaluated for manufacturing test thanks to structural fault coverage measurements.*

## I. Introduction

New efficient methods have emerged to design analog, RF and mixed (AMS&RF) or hybrid Integrated Circuits (ICs). Nowadays, the test of these IC is becoming a crucial challenge for manufacturers. The expectations of final consumers impose these systems to include more functionalities, better portability, more autonomy...and of course better quality. They are becoming Systems-on-Chip (SoCs) or Systems-in-Package (SiP). This increasing complexity forces designers to define new design methodologies adapted to these complex systems with shorter time to market and lower manufacturing cost constraints. However, the problem is not only to achieve short time to market but also to control the quality of final products. In fact, the more complex systems are, the more difficult and expensive production is.

The test production of AMS&RF SoC is often performed using a sub-set of the characterization test stimuli. The evaluation of this sub-set is empirically made. This paper presents a method to generate test production stimuli for AMS&RF SoCs. The generation is based on the evaluation of characterization test set thanks to high level fault injection and simulation technique.

The increasing SoCs complexity involves high simulation time for AMS&RF systems. In some cases, it is impossible to simulate the whole system at transistor

level! This problem can be partially solved by describing the electrical system with higher description level (behavioral or functional level) rather than structural level. So, when it is impossible to simulate and generate test sets at structural level (using low level faults models), we propose to use behavioral level descriptions. Obviously, this work can also serve verification team in charge of verifying that system architecture meets the specification requirements. In this paper, we show on a test case study the quality of this high level test approach.

In a first part, the fault simulation techniques with structural and with behavioral level descriptions are presented. Then, the definitions of the faults models used to validate circuits at structural or behavioral levels are given. In addition, the different descriptions of the WCDMA system applied to validate our method are presented. In the fourth section, our PLAtform for System qualification with Mixed and Analog signals (PLASMA) is detailed. Then, results provided by PLASMA for the receiver part of the WCDMA transceiver are presented. Finally, the behavioral fault coverage is compared with structural fault coverage.

## II. Fault injection & simulation

### A. Fault injection

The fault injection is a verification technique used for a long time. It has been used for production testing, for high level testing, and for design validation of digital circuits. It has also been used for the manufacturing test analysis of AMS&RF circuits described at the transistor level [1, 2]. The principle is always based on the simulation of faulty circuits generated from the original description under test. The faulty circuit can be either created depending on the abstraction level by modifying a functionality, or a mathematical operator, or a specification, or a component value...

### B. Fault modeling level

The classical modeling level used for the qualification of manufacturing test set is the structural level. It is based on parameter variations of low-level components: inductor, capacitor, resistor, or transistors. The mains structural languages used for test qualification are SPICE-like languages.

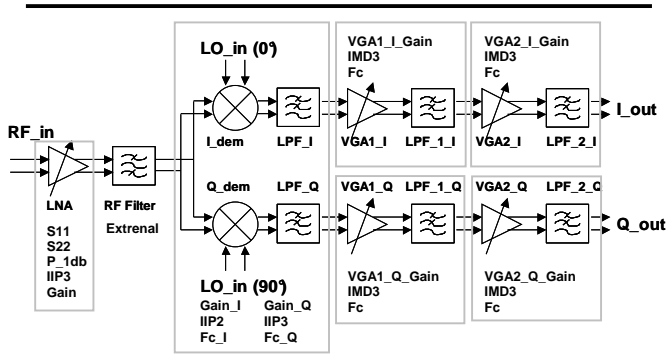


Fig. 1: WCDMA Receiver Part (RX)

The increasing complexity of SoCs leads to add the behavioral abstraction level descriptions in the AMS&RF SoC design flow. This abstraction level permits to describe complex systems with accuracy between functional level and structural level accuracy. The behavioral level is a trade off between strengths of functional and transistor levels that are respectively short simulation times and high accuracy of models. This level has also led to the standardization of behavioral languages like VHDL-AMS [3].

In our tool PLASMA, which operates on behavioral descriptions, the fault model is made of only a single and small modification of the original description. We assume that a huge modification of the description has little chance to appear during the design process. However, if this kind of fault appears, it should be easy to detect. In our case, only mutations are used; it means that faulty models are generated by only modifying the value of behavioral parameters.

### III. WCDMA System

The studied system is the receiver part of a WCDMA (Wideband Code Divided Multiple Access) transceiver. WCDMA is a technology used for third-generation cellular systems (3G). The frequency range down-link (Bases Station to User Equipment) or receiver part is [2110-2170MHz]. The modulation defined in the WCDMA standard is an IQ modulation based on two signals: I "in-phase" component of the waveform, and "Q" represents the quadrature component. WCDMA standard specifies several parameters: maximal and minimal output power, maximal power out of frequency band, ACLR (Adjacent Chanel Leakage Ratio)...

Figure 1 presents the architecture of the receiver part (Rx).

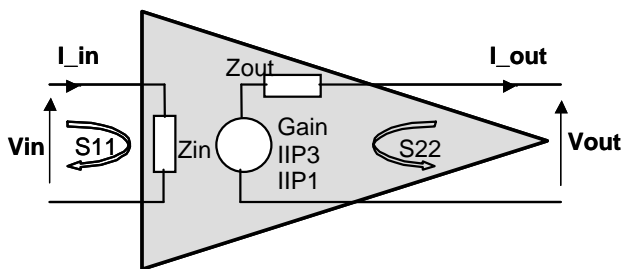


Fig. 2: Behavioral model of LNA

Parameters	Typical Value	Minimum	Maximum
S11	-14.47dB		-10.25dB
S22	-6.1dB		-1dB
Gain	13.85dB	11.85dB	15.85dB
IIP3	-0.24dBm	-5.03dBm	
IIP1	-8.84dBm	-18.4dBm	

Tab. 1: Limits of a amplifier parameters

It is a classical architecture made of Low Noise Amplifier (LNA), external Surface Acoustic Wave (SAW) RF filter, mixers, base-band Voltage Gain Amplifiers (VGA) and internal filters. Digital registers (not illustrated in Fig. 1) control the LNA and VGA gains. These registers permit to control the receiver parameters; they can be used to control the system during validation [4].

#### A. Behavioral model

The behavioral model of the LNA is presented in order to illustrate this modeling level. In behavioral modeling, two classes of parameters, functional and electrical parameters, are defined. The amplifier model is made of one functional parameter, the power gain (Gain), and several electrical parameters: input and output impedances ( $Z_{in}$ ,  $Z_{out}$ ), S parameters ( $S_{11}$ ,  $S_{22}$ ), compression point at 1dB (IIP1), third-order intermodulation distortion (IIP3). The figure 2 presents the behavioral model of the amplifier with its functional and electrical parameters. The table 1 specifies the limits of several parameters. Each parameter is defined by a typical value and with one or two worst-case values (minimum and/or maximum admitted values). In Tab. 1, the gain is specified by two limits because both limits are significant; the other parameters have only one significant limit.

The other blocks of the system are modeled in the same way with a few additional parameters: IIP2 (Second-Order Intermodulation Distortion), DC offset, and cut off frequency. The figure 1 gives a parameters list for each block. Finally, the receiver part is modeled by only 23 functional and electrical parameters (Fig. 1). These parameters are the most significant parameters in the

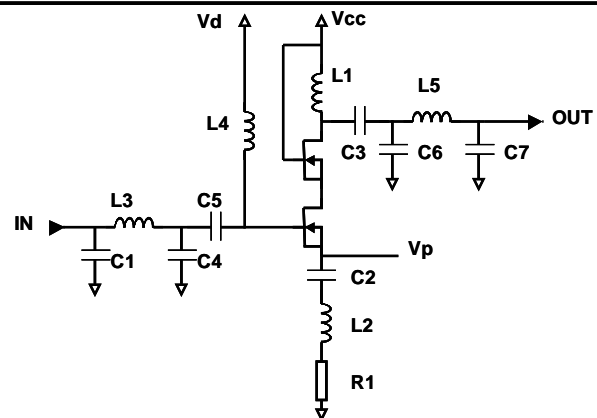


Fig. 3: Structural model of LNA

system design. Obviously, our qualification process could be applied on a description involving additional parameters. The WCDMA transceiver is modeled with VHDL-AMS language.

### B. Structural model

Our qualification tool only uses behavioral models. However, the evaluation of our high level test approach requires the use of a lower abstraction level. Only LNA has been described at the transistor model (fig. 3) because it would be too time consuming to simulate the entire system at structural level. So, the evaluation is only realized for LNA behavioral and structural parameters. Of course, other structural evaluation could also be realized for each part of the system. The simulation of the structural LNA into the system is possible using multi-abstraction simulation technique. It means that simulations are realized using several abstraction levels: LNA is described at transistor level and others blocs are described at behavioral level. The simulations are realized with the Mentor Graphics ADvance MS RF Simulator. The Mentor Graphics behavioral VHDL-AMS library's CommLib RF [5] is used.

The 2.1GHz LNA includes an amplifier stage based on cascode structure (Fig. 3). The advantage of this architecture is to control the noise and the linearity. Input and output matchers are added for the impedance adaptation.

## IV. PLASMA: PLAtform for System qualification with Mixed and Analog signals

PLASMA is described in this part. PLASMA is an automatic test set qualification and generation software platform based on fault injection and simulation. The fault simulation technique relies on the comparison of the simulation results of fault free and faulty circuits (Fig. 4). Faulty and fault-free models are simulated with the same input vectors. When the comparison of simulation results involves a difference, the fault has been both activated and propagated toward one or more primary outputs; we say that the fault is detected. Although PLASMA contains an automatic stimuli generator, only test set qualification part and optimization will be discussed in this paper. The

optimization functionality involves the reduction of the predefined test set by identifying and saving only the vectors which detect a fault.

### A. Free fault models definition

The qualification of pre-defined test sets is realized by comparing simulation results. Fault-free models are simulated with pre-defined vectors and provide simulation results presumed to be “good” measurement values. The next comparison is only possible thanks to these fault free measurement ranges. Obviously, simulation results limited to one model instantiated with typical specifications would not be enough. Fault-free models are defined as models instantiated with parameters values defined in their specifications ranges. There is an infinity of parameters combinations thus the problem is to determine a realist and representative number of fault-free models. Some methods are based on Monte Carlo analysis, worst-cases combinations, single variation... [1,2,6]. In our case, fault-free models are defined using the statistical distributions of behavioral parameters. Then, the statistical parameters of the simulation results (i.e. measurements) can be extracted. Generally, Gaussian estimation is done thanks to Monte Carlo analysis but this method requires the simulation of too many models. In PLASMA, the number of fault free simulated models is decreased by analyzing the statistical characteristics of the results: i.e. the average ( $\mu$ ) and the standard deviation ( $\sigma$ ) of fault-free simulation results. The number of fault free simulated models is increased as long as  $\mu$  and  $\sigma$  variations are not negligible. Then, the fault free measurement ranges can be determined by defining the limits at  $6\sigma$ .

### B. Faulty model definition

In part II, fault model has been defined as a variation of behavioral parameters described in the model. Mutants are generated by translating one parameter of the original description to a value outside of its specifications, but the definition of this faulty value is difficult. When this value is too close to specifications limits, the fault is hardly detectable because circuit robustness or simulation tool accuracy mask fault. When this value is too distant to fault free detection limits, the fault is easily detected but less realistic and could be detected by most of stimuli.

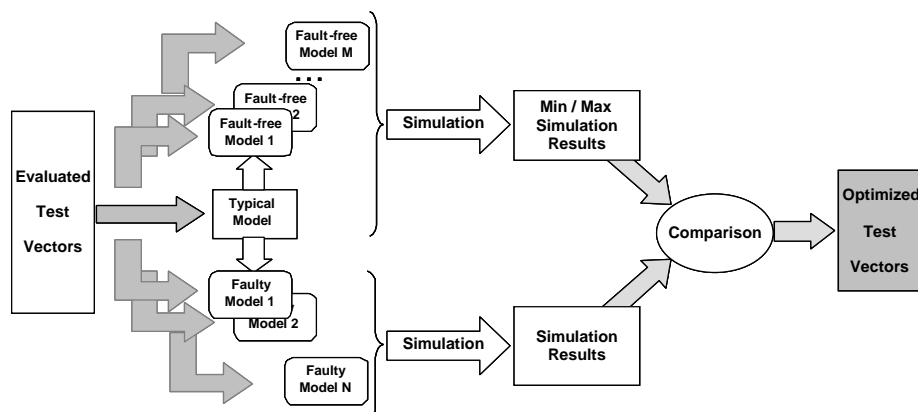


Fig.4: Test vector qualification & optimization

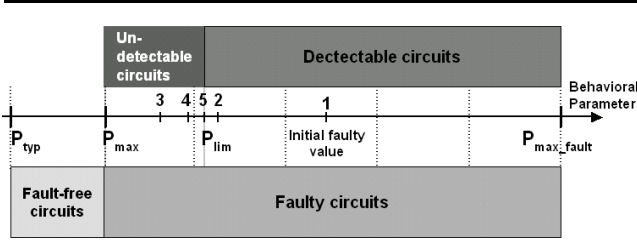


Fig. 5: Definition of faulty value

The faulty value definition is solving by simulating iteratively several parameters values. A first value is defined far from limit and a dichotomy algorithm allows PLASMA to determine the faulty detection limit (Fig. 5). The faulty parameter is computed starting from tolerance ranges (Minimal and maximal specified values). The initial faulty parameter value of a mutant is specified at the middle of  $[P_{max}, P_{max\_fault}]$  range where  $P_{max}$  is the limit value, and  $P_{max\_fault}$  is the maximal accepted faulty value. This faulty value depends on both its tolerance range ( $P_{max} - P_{typ}$ ) and its maximal value  $P_{max\_fault}$  (Fig. 5). This maximal accepted value  $P_{max\_fault}$  equals to 5 times the tolerance range:  $P_{max\_fault} = P_{max} + 5.(P_{max} - P_{typ})$ . The dichotomy algorithm is iterated 10 times and determines a good estimation of the detection limit  $P_{lim}$ .

This detection limit is computed for every mutated parameter and every qualified vector. Relative Parametric Coverage (RPC) qualifies the detection limit; RPC is defined in Eq. 1.

$$RPC_{PL1} = 1 - \frac{(P_{fault_{PL1}} - P_{max_{PL1}})}{P_{max\_fault_{PL1}} - P_{max_{PL1}}} \quad (1)$$

When the detection limit equals to the specification limit, then the RPC is 100%. The farther this detection limit is from the specification limit, the lower is the RPC. The test set optimization is realized by saving the vector that leads the lowest RPC.

## V. Test set optimization for WCDMA RX part based on behavioral faults simulation

### A. Definition of the predefined test set

During the design of complex electrical systems, a verification plan must be defined. This plan defines how to validate the design [7]. This plan involves the definition of test benches. These test benches consist of vectors which aim to validate system specifications within all configurations (Gain, Offset) and with different input signals characteristics (frequency, power). For example, these vectors or stimuli verify the values of the programmable gains, the IIP3, the IIP2... Generally, this manually generated test sets is assumed to be adapted to the verification of the specifications. The problematic of this paper is to evaluate and to optimize this test set, its generation will not be discussed here. The metric for manufacturing test evaluation is presented in the next section.

The validation test set is made of stimuli with single tone signals applied on the RF\_in input and the RX LO\_in

	Frequency	Power
RF	2113.4 MHz	-60dBm
RX LO	2112.4 MHz	-7dBm

Tab. 2: Two tones input signal parameters

LNA Gain	-15dB
VGA1 Gain I	-10dB
VGA1 Gain Q	-10dB
VGA2 Gain I	23dB
VGA2 Gain I	23dB

Tab. 3: WCDMA Receiver part configuration

input (fig. 1); one example of test vector parameters is given in Tab. 2 and Tab. 3. Tab. 2 describes the two RF signals RF and LO whereas Tab. 3 gives receiver gains configuration controlled thanks to digital registered inputs. In the following experimental results, a test set made of 98 manually proposed single tone vectors will be evaluated. These test benches have been optimized with PLASMA.

### B. WCDMA faulty models

Faulty models of WCDMA receiver part are defined as presented in section II A. The number of faulty models is fixed by the number of behavioral parameters. When a parameter is specified by two limits (for example, the gain in Tab. 1), two mutants are generated: a first for the low limit and a second for the high limit; when it is specified by one limit (ex: IIP3), only one mutant is generated. Due to this consideration, the receiver part of WCDMA SoC modeled by 23 behavioral parameters involves the generation of 36 faulty models.

### C. Optimization results

The simulation has been realized with ADMS RF from Mentor Graphics on a 3 GHz Pentium-4, with 1 GB RAM, running a Linux Operating System.

The 98 validation vectors have been optimized with our PLASMA tool. Over 36 mutated parameters, 32 have been detected by the 98 validation vectors during the entire dichotomy process. The mutation score is 89% and the total computation time is about 18 hours. The average RPC computed with all behavioral parameters is 83%.

Each vector of the 98 vectors detects a least one behavioral faulty parameter but after compaction, only 4 vectors are kept to achieve the same RPC. After compaction, the number of stimuli is divided by 24.5. The table 4 shows the Behavioral Parameter detection (BPD) limits of the LNA behavioral parameters and the Relative Parameter Coverage RPC. The two faults which have not been detected concern the variations of S22, or IIP3 parameters. S22 variation is not detected due to the system robustness which masks its impact. Test benches are not relevant for the detection of IIP3 mutation. These two faults would be detected by a test set generation adapted to their activation and propagation in the system.

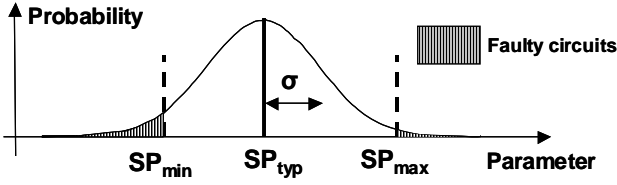


Fig. 6: Capability Process definition

## VI. Evaluation of behavioral fault modeling for manufacturing test

In the previous section, the results of the validation test set optimization has been shown, the efficiency of this optimization for manufacturing test is evaluated in this section. Obviously the application test cost of the compacted stimuli is lower than the application of the complete validation test set. The advantage of the described technique based on behavioral faults injection is the time reduction to qualify vectors; but is this high level fault model significant for manufacturing test? The evaluation will be provided by making comparison with a fault model described at lower abstraction level: the structural fault model.

Designers can estimate the distribution of structural parameters values. The Capability Process CPk (eq. 2) is a statistical parameter that allows designers to qualify the robustness of the structural parameters according to both the process and the device specifications. Parameters are assumed to have a Gaussian distribution and the CPk is defined by:

$$CPK = \frac{\text{Min}((P_{typ} - P_{min}); (P_{max} - P_{typ}))}{3\sigma} \quad (2)$$

Where  $P_{typ}$  is the typical value of a parameter defined in the specifications,  $P_{max}$  and  $P_{min}$  are specified limit values,  $\sigma$  is the standard deviation (Fig. 6). The probability to obtain a faulty circuit (hatched area) can be computed from these different values. During the determination of test stimuli, some faulty circuits are not detected (the darkest area in Fig 5), this undetected zone is due to system robustness, measurement accuracy or due to stimuli not adapted to the detection. We aim to decrease this undetected number by finding the most relevant stimuli. Thus, the vector quality is quantified by computing the number of remaining undetected faulty circuits. Our high level testing approach will be evaluated by comparing the number of undetected faulty circuits induced with behavioral and structural fault model.

During this evaluation, we assume that structural fault modeling is the reference. The first stage of the evaluation is the computation of structural faulty parameter detection limit (SPd). This limit is the limit that would be obtained if a structural faulty model were used. SPd is computed with our PLASMA tool using a transistor level description of the LNA. In order to decrease the simulation time, only LNA is described at this transistor level (the other blocs are described at behavioral level). Moreover, we only

simulate compacted test set (4 vectors) determined in section V. B. The SPd value for each structural parameter involves mutants which are not detected (with the optimized test set). The number of these mutants is represented by the union of dotted and hatched areas in figure 7.

The second stage of the evaluation should be the comparison between SPd limits with the behavioral fault model parameter detection Bpd limits, but this comparison is only possible if the two detection limits are given at the same abstraction level. Thus, the behavioral faulty parameter detection limit (Bpd) computed during the optimization must be translated to a structural variation. The conversion is possible by simulating each block individually at the structural level. In this paper, the evaluation is only performed for the LNA; so only LNA block is simulated here. Test benches are used to measure the following LNA behavioral parameters: S11, IP1, Gain,... The translated detection limits of structural parameters  $SPd_T$  are extracted by computing a single parametric structural deviation that involves at least one behavioral parameter going out of its detection limits Bpd. A variation of a structural parameter out of  $SPd_T$  has lot of chances to be detected by the compacted test data. However, the induced correlated variations of several behavioral parameters due to the variation of a single structural parameter can sometimes be masked. At the contrary, it is also possible that these correlated variations involve an easiest detection. However, the following analyses shows that the  $SPd_T$  limits computed with Bpd limits are very close to SPd reference limits.

The behavioral fault model is qualified by comparing the number of undetected faulty circuits computed from SPd with the number of undetected faulty circuits computed from  $SPd_T$ . The figure 7 shows two areas (under the Gaussian curve) corresponding to these numbers. SPf is the fault limit for the structural parameters;  $SP_{min}$ ,  $SP_{max}$  in Fig.6. In Fig. 7, the area between SPf and SPd (dotted area + hatched area) or SPf and  $SPd_T$  (dotted area) are respectively the real number and the estimated number of faulty circuits that is not detected by the compacted test set. The hatched area (between SPd and  $SPd_T$ ) is the number of faulty models that are supposed detected but which are not detected with behavioral fault model: it is the error that is made when evaluating the test coverage using behavioral modeling. In the case of Fig. 7, the evaluation is a little optimistic because supposed detected circuits are not really detected (as shown with structural fault model). As previously explained, this area is due to

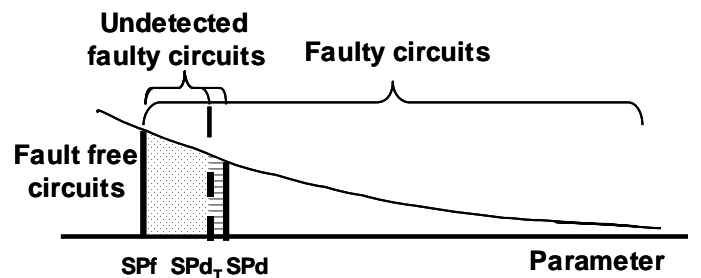


Fig. 7: Detection limit of Structural parameter

relations between structural and behavioral parameters. In fact, our fault model is based on single behavioral variation but a modification of one structural fault leads variations of several behavioral parameters. In our high level fault model, the effects of these correlated behavioral parameter variations are canceled.

Table 5 presents several characteristics of all structural parameters of the LNA: typical value, limit detection value (SPd)... The values of SPd and SPd<sub>T</sub> obtained for parameters are very close. In fact, the relative error measure through the number of undetected mutants with SPd and SPd<sub>T</sub> is only 2%. The error obtained for each parameter is nearly equal. In fact, SPd and SPd<sub>T</sub> values are very close from specification limit and this 2% step is due to the detection limit method based on dichotomy. In fact, more iteration during the detection limit computing will increase the accuracy of limit value and modify the number of faulty circuits. Therefore, the relative error on faulty circuits will probably varying a little from 2%.

## VII. Conclusion

In this paper, a production test generator (PLASMA) has been presented and evaluated. In the proposed strategy, the validation test benches developed by designers to verify all specified parameters are re-used. We show that re-using these test benches for the production testing is relevant. Generally the number of validation test benches is huge, so we propose to optimize them with a behavioral fault injection method. We assume that the detection of maximum behavioral faults allows the detection of numerous physical defects. This assumption is verified by comparing simulation results generated with behavioral

fault model and structural fault model. The metric used to evaluate our high level fault model accuracy is the number of un-detected faulty circuits. This metric qualifies the efficiency of the test stimuli. Results show that the numbers of un-detected mutants are almost the same with a behavioral or a structural fault model. These results have been obtained for the faults detection of a LNA embedded in a WCDMA receiver. We are realizing additional experiments in order to observe if behavioral fault model use always leads to correct production test set evaluation.

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	Structural Parameter	Typical Value	Specification limit value	Number of faulty circuits	Detection limit of Structural Parameter SPd	Number of undetected faulty circuit defined with SPd (PPM)	Detection limit of translated Structural Parameter SPd <sub>T</sub>	Number of undetected faulty circuit defined with SPd <sub>T</sub> (PPM)	Relative error of number of undetected faulty circuits defined with SPd <sub>T</sub> (%)	
Resistance (Ohms)	R1 Max	2,500E+00	3,250E+00	7,944E-01	3,254E+00	8,791E-02	3,253E+00	7,111E-02	2.12	
	C2 Min	1,000E-06	9,000E-07	7,944E-01	8,995E-07	8,790E-02	8,996E-07	7,109E-02	2.12	
Capacitor (F)	C2 Max	1,000E-06	1,100E-06	7,944E-01	1,100E-06	8,802E-02	1,100E-06	7,099E-02	2.14	
	C3 Min	1,000E-12	9,000E-13	7,944E-01	8,995E-13	8,788E-02	8,996E-13	7,109E-02	2.11	
	C3 Max	1,000E-12	1,100E-12	7,944E-01	1,100E-12	8,785E-02	1,100E-12	7,099E-02	2.12	
	C4 Min	3,252E-13	2,897E-13	7,944E-01	2,895E-13	8,788E-02	2,895E-13	7,107E-02	2.12	
	C4 Max	3,252E-13	3,607E-13	7,944E-01	3,609E-13	8,788E-02	3,609E-13	7,107E-02	2.12	
	C5 Min	1,000E-11	9,000E-12	7,944E-01	8,995E-12	8,788E-02	8,996E-12	7,109E-02	2.11	
	C5 Max	1,000E-11	1,100E-11	7,944E-01	1,100E-11	8,802E-02	1,100E-11	7,116E-02	2.12	
	C6 Min	1,400E-12	1,260E-12	7,944E-01	1,259E-12	8,794E-02	1,259E-12	7,111E-02	2.12	
	C6 Max	1,400E-12	1,540E-12	7,944E-01	1,541E-12	8,794E-02	1,541E-12	7,111E-02	2.12	
	C7 Min	1,000E-11	9,000E-12	7,944E-01	8,995E-12	8,788E-02	8,996E-12	7,109E-02	2.11	
	C7 Max	1,000E-11	1,100E-11	7,944E-01	1,100E-11	8,802E-02	1,100E-11	7,116E-02	2.12	
	Inductor (H)	L1 Min	1,000E-06	9,500E-07	7,944E-01	9,498E-07	8,788E-02	9,498E-07	7,113E-02	2.11
		L1 Max	1,000E-06	1,050E-06	7,944E-01	1,050E-06	8,819E-02	1,050E-06	7,099E-02	2.16
		L2 Min	2,500E-09	2,375E-09	7,944E-01	2,374E-09	8,785E-02	2,375E-09	7,106E-02	2.11
L2 Max		2,500E-09	2,625E-09	7,944E-01	2,626E-09	8,785E-02	2,625E-09	7,106E-02	2.11	
L3 Min		1,060E-08	1,007E-08	7,944E-01	1,007E-08	8,796E-02	1,007E-08	7,142E-02	2.08	
L3 Max		1,060E-08	1,113E-08	7,944E-01	1,113E-08	8,796E-02	1,113E-08	7,142E-02	2.08	
L4 Min		1,000E-06	9,500E-07	7,944E-01	9,498E-07	8,788E-02	9,498E-07	7,113E-02	2.11	
L4 Max		1,000E-06	1,050E-06	7,944E-01	1,050E-06	8,819E-02	1,050E-06	7,099E-02	2.16	
L5 Min		4,300E-09	4,085E-09	7,944E-01	4,084E-09	8,791E-02	4,084E-09	7,103E-02	2.12	
L5 Max		4,300E-09	4,515E-09	7,944E-01	4,516E-09	8,791E-02	4,516E-09	7,103E-02	2.12	
Transistor	LM X1 Min	2,400E-07	2,360E-07	7,944E-01	2,360E-07	8,819E-02	2,360E-07	7,143E-02	2.11	
	LM X1 Max	2,400E-07	2,567E-07	7,944E-01	2,568E-07	8,790E-02	2,567E-07	7,119E-02	2.10	
	WF X1 Min	1,000E-05	9,900E-06	7,944E-01	9,900E-06	8,802E-02	9,900E-06	7,116E-02	2.12	
	WF X1 Max	1,000E-05	1,200E-05	7,944E-01	1,201E-05	8,793E-02	1,201E-05	7,108E-02	2.12	
	LM X2 Min	2,400E-07	2,360E-07	7,944E-01	2,360E-07	8,819E-02	2,360E-07	7,143E-02	2.11	
	LM X2 Max	2,400E-07	2,567E-07	7,944E-01	2,568E-07	8,790E-02	2,567E-07	7,119E-02	2.10	
	WF X2 Min	1,000E-05	9,900E-06	7,944E-01	9,900E-06	8,802E-02	9,900E-06	7,116E-02	2.12	
	WF X2 Max	1,000E-05	1,200E-05	7,944E-01	1,201E-05	8,793E-02	1,201E-05	7,108E-02	2.12	

Tab. 5: Structural Parameter detection limits (SPd) and Error on un-detected faulty circuits