



HAL
open science

Behavioral modeling of W-CDMA transceiver with VHDL-AMS language

Yves Joannon, Vincent Beroulle, Rami Khouri, Chantal Robach, Smail
Tedjini, Jean-Louis Carbonero

► **To cite this version:**

Yves Joannon, Vincent Beroulle, Rami Khouri, Chantal Robach, Smail Tedjini, et al.. Behavioral modeling of W-CDMA transceiver with VHDL-AMS language. DDECS'06, Apr 2006, Prague, Czech Republic. pp.113 - 118. hal-00250397

HAL Id: hal-00250397

<https://hal.science/hal-00250397v1>

Submitted on 13 Feb 2008

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Behavioral modeling of WCDMA transceiver with VHDL-AMS language

Yves JOANNON^{1,2}, Vincent BEROULLE¹, Rami KHOURI¹, Chantal ROBACH¹, Smail TEDJINI¹, Jean-Louis CARBONERO²
LCIS-ESISAR (INPG), Valence, France¹, ST MICROELECTRONICS, Crolles, France²

Abstract-This article presents the behavioral modeling of a WCDMA transceiver. The model has been developed in VHDL-AMS language. The WCDMA behavioral model is made of RF parameters like gain, impedance, IIP, leakages... The methodology uses to develop this model is included in a Top-Down design flow. The model has been validated thank to comparisons between simulation results and measurements on a silicon prototype.

1 INTRODUCTION

Currently, more and more complex multi-domain, analog and mixed-signal systems are developed. Wireless *System-on-Chip* (SoC) or *System-in-Package* (SiP) integrates both digital, analog and RF parts on a same substrate. This integration increases the design difficulties and involves the need of a new design methodology. Traditionally, Bottom-Up design flow starting at the transistor level is used by analog RF designers. Top-Down design flow, adopted for many years by digital designers, can be applied to analog and mixed-signal systems too. However, the huge gap between functional level models and transistor level models involves great design difficulties. So, behavioral models have been developed to fill this gap. This intermediate level relies on analytical equations which take into account electrical effects as for example mismatching, non-linearity... This level of modeling involves the use of new Hardware Description Languages (HDL) and simulation environments. These HDL allow the simulation of multi-domain systems at the following different abstraction levels: functional, behavioral, and transistor levels. This article presents the behavioral model of a RF front-end used during the Top-Down design flow of a Wireless System-on-Chip. The behavioral modeling is realized with functional specifications of each block. This model is used to validate system specifications and it allows the design and the validation of each block independently.

The development of behavioral model libraries should increase the interest of designers to use these models and this abstraction level. In fact, the re-use of existing behavioral models will decrease system validation efforts.

RF transceiver behavioral models have already been described using VHDL-AMS in [1] and [2]. In these articles, RF blocks models consists of simple analytical equations with functional parameters and few electrical parameters. The only electrical parameters used in these models are the noise figure and the phase noise. Our work focuses on the behavioral modeling of a RF transceiver using the classical RF parameters. Of course, our model uses functional parameters, but it also contains numerous electrical parameters: gain, impedance, third-order Interception Point (IP3), leakage...

In section 2, two mains design flow, Top-Down and Bottom-Up, are presented. Then, our WCDMA transceiver architecture is presented. The behavioral model of this WCDMA transceiver is described and validated in section 4. This validation was done first comparing block simulation results and theoretical responses, and then comparing system simulation results and measurements done on a silicon prototype.

2 DESIGN FLOW AND VALIDATION ENVIRONMENT

The increasing complexity of systems involves new difficulties for system designers. In order to reduce the size of the final products and to decrease the cost of the chips, manufacturers integrate more and more components in a single die. This integration of digital, analog and RF core involves the contribution of different specialized design teams. These issues impose to use a new design flow methodology. So, in this section, the different design flow methodologies are described and compared. This description will also present different levels of modeling and will justify the choice of our behavioral abstraction level.

2.1 Design flow

2.1.1 Bottom-Up design flow

The first design flow methodology presented here is the Bottom-Up methodology (Fig. 1). This is the traditional design approach [3], [4]. This method first consists in independently designing each macro-component or block of the system. Then these macro-components are combined together to form the final system.

Each block is designed and simulated at transistor level. Then, the layout is realized (Fig. 1 [d]), and a post-layout simulation taking into account the layout parasitic is conducted to obtain final performances of the block.

When all the blocks are designed and verified, they are interconnected. The post layout parasitic extraction is then realized: this allows to obtain a structural model that includes all parasitic elements (Fig. 1 [c]). Unfortunately when systems are too large, simulations become very time consuming. Thus, a behavioral model is developed from this extracted model (Fig. 1 [b]). This new simplified model is less detailed but it can be simulate with reasonable simulation times. Finally, these simulations permit to verify the whole system and to validate it (Fig. 1 [a]).

2.1.2 Top-Down design flow

The second design flow methodology is the Top-Down methodology (Fig. 2). The system is first defined at functional

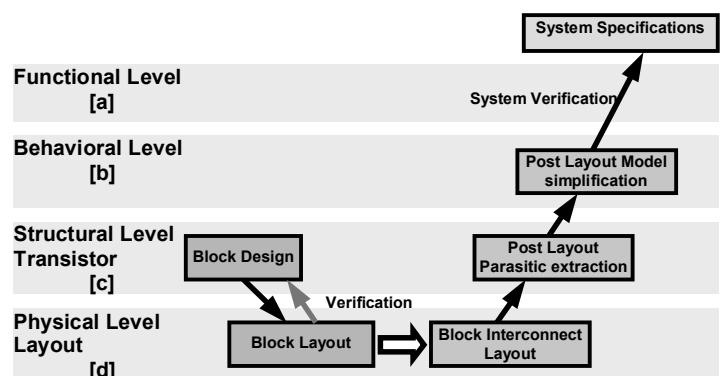


Fig. 1: Bottom-Up design flow.

level. Then, several successive steps permit to model the different blocks increasing the detail of the models.

First, system architecture is defined at **functional level** [a]. Different architectures are evaluated and the system is partitioned in several blocks or macro-components. Functional simulations permit the validation of this architecture comparing simulation results with the system specifications. Functional model does not implement electrical equations but only analytical relations between input and output (gain, transfer function...). When the architecture is validated, functional parameters are budgeted between different blocks: this means that global system characteristics (i.e.: gain, noise, IP3...) are distributed into several blocks. It is then possible to define the specifications of each block.

The next stage is the **behavioral level** [b]. The behavioral modeling permits to take into account the electrical parameters. However, these behavioral models are not defined at transistor level, they rather integrate electrical specifications using simplified analytical equations. The interest of this level is to define models that are not too complicated but that are sufficiently accurate. This behavioral model allows the simulation of huge systems that could not be simulated at structural level. More than only a functional validation, this system simulation validates the electrical interface between the different blocks. This level can be divided into several abstraction sub-levels; each sub-level is defined by the detail of parameters. Behavioral model is verified by simulation and comparison with functional model. This step permits to go down to the transistor level.

At this step, the structures or netlists of the blocks are defined [c]. The specifications of each block allow their design separately from each other. Thus, these blocks can be designed in parallel by several specialized teams. The blocks are simulated and validated at **transistor level**. One of the advantages of Top-Down design is that behavioral models have previously been built, so each structural block description can be validated in the overall system using other block behavioral models. This validation is possible thanks to multi-abstraction simulation: one block is described at structural level and others are described at behavioral level. Thus, the final netlists of all the blocks is not necessary to start validation of an individual netlist. Moreover, designers can validate their blocks in the system without having to understand the details of each other design block. Then, blocks are assembled together to obtain the system structural level.

The last design level is the **physical level** [d].

2.1.3 Meet in the middle design flow

The “Meet in the middle” methodology is made of Top-Down and Bottom-Up methodologies. This method takes advantages of each approach.

The first step is coming from Top-Down design flow: system

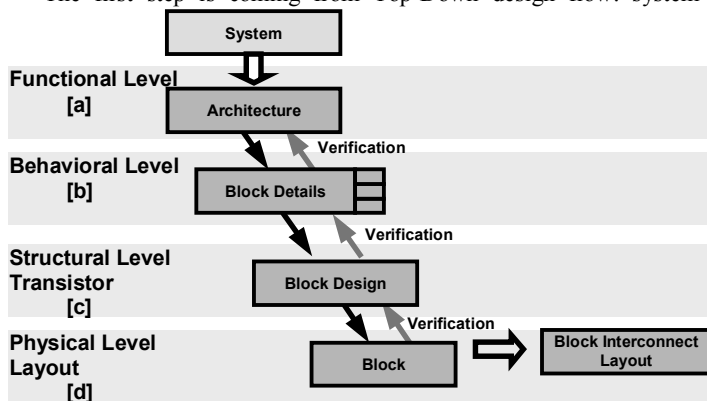


Fig. 2 : Top-Down Design Flow.

architecture is described thanks to functional block models. Once again, system specifications are budgeted into numerous block specifications. In this methodology, a trade-off between system engineers and component designers allows them to determine realistic specifications for each block. Then, these blocks are separately designed and assembled together. Finally, the system is validated as in a Bottom-Up design flow.

2.2 Validation environment

Simulation is important for electronics system validation. Moreover simulation also allows to compare and to optimize system architectures. In previous parts, it has been shown that simulation is used at each stage. In this context, several descriptions languages could describe electrical systems at different levels of abstraction.

Historically, the first type of language for analog electrical modeling is a structural language; that is the well-known SPICE type language. This language permits to model the system with built-in primitives: transistors, resistor, inductor are assembled to compose the system. The system simulation at transistor level needs long time due to the high number of equations to be solved. The advantage of this language is that simulation results are quite similar with real system answers. But, in most of industrial cases, complex systems could not be entirely simulated at structural level. At the opposite, the second type of language is a functional language; these languages are proprietary languages (Matlab) or based on C language. These languages support functional parameters but could not easily implement electrical characteristics.

2.2.1 Hardware Description Language:

The use of different language between functional and structural level is an important issue. System engineers and designers use incompatible languages and tools. Thus, misunderstanding could appear during the design. To eliminate these errors, a new type of hardware description language have been defined, these languages permit the description of systems at behavioral level.

There are two mains HDL that support the description of analog and digital parts: Verilog-AMS and VHDL-AMS [5]. The second one has been used to describe our transceiver system. VHDL-AMS is the only mixed-signal standardized HDL (IEEE 1076-1999). VHDL-AMS is independent of design methodologies, manufacturing technologies, software tools... Hierarchic description is possible and permits the description at different abstraction levels. The HDL improves the communication between designer teams by increasing the quality of specifications and documentations.

2.2.2 Simulation Tools

Advance MS RF (ADMS RF) [6] from *Mentor Graphics* support VHDL-AMS descriptions. ADMS RF permits, in addition to digital and analog simulation, RF steady state (SST) and modulated steady state simulations (MODSST), thanks to Harmonic Balance based algorithms. This makes possible a fast simulation of digitally modulated RF signals, and consequently, simulation of most of the complex mixed signal wireless systems [7].

For example, this unified simulation environment permits multilingual modeling and simulation. Indeed, it is possible to simulate a complex system which digital part is a VHDL gate level IP, its analog part is a SPICE Netlist and its RF front-end is a VHDL-AMS behavioral description.

ADMS RF integrates a RF library, *Commlib RF*, composed of mains RF blocks like LNA, Power Amplifier, mixer, filters... These models are described at a behavioral level; they are specified by characteristic impedances, S parameters, gain, IIP3, noise...

Our simulation environment has been previously presented and the modeling level we target has been determined. The RF system modeled is presented in this part.

3.1 Principle of WCDMA

The Wide Code Divided Multiple Access is a technology used for third-generation cellular systems (3G). The 3G has the main objective of creating a world standard for telecommunication. It substitutes the second-generation and increases the data rate from 9.6kbps (2G) to a theoretical data rate of 2Mbps.

The frequency range is defined by the Frequency Division Duplex mode; this mode specifies a frequency range for the up-link (User Equipment to Base Station : [1930-1980MHz]) and the down-link (Bases Station to User Equipment: [2110-2170MHz])

The WCDMA standard does not assign a specific frequency to each user. Several users can use the same frequency channel thanks to data coding.

The 3G standard specifies several parameters like maximal and minimal output power, maximal power out of frequency band, ACLR... For our design, these parameters correspond to system specifications and are used to determine block specifications during the Top-Down design flow.

3.2 Architecture description

After this short presentation of WCDMA technology, receiver and transmitter architectures are described.

3.2.1 Receiver Part

The architecture uses is a Zero Intermediate Frequency (IF) Wireless Radio architecture. It employs only one stage to down-convert the RF signal directly to the desired base-band signal. The zero IF architecture is easily integrated because it is made of only low pass filters and mixers. Its disadvantage is due to DC offset that deteriorates the Signal Noise Ratio.

Fig. 3 presents the architecture of the receiver (Rx) part. The RF signal is amplified by a Low Noise Amplifier; then, the signal is filtered by an external dedicate RF filter (Surface Acoustic Wave filter).

Some mixers, a Local Oscillator (LO) and a 90 degrees phase shifter down-convert the RF signal to two base-band signals. These signals are amplified and filtered in order to obtain I and Q signals. Digital registers affect the LNA, VGA gains and the offset compensator value. These registers permit to control the receiver parameters; they are used to control the system during validation.

3.2.2 Transmitter part

The transmitter architecture is a super heterodyne architecture (Fig.

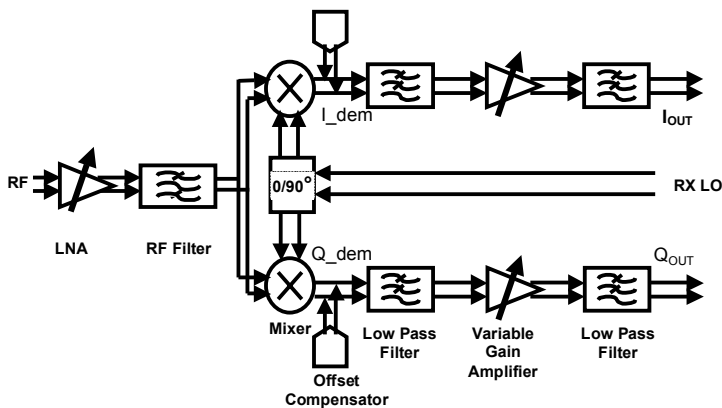


Fig. 3 : WCDMA Receiver Part.

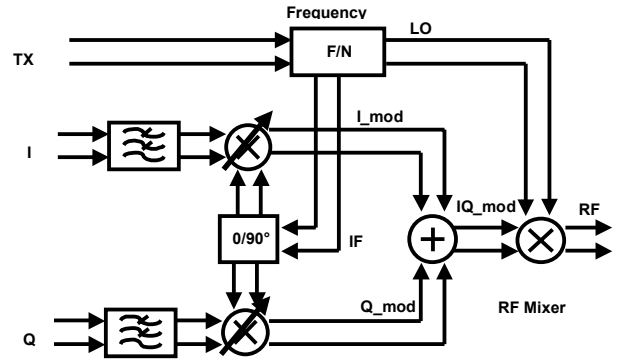


Fig. 4 : WCDMA Transceiver Part.

4). A frequency divider block (F/N) generates two frequencies clocks (IF and LO). The data signal is up-converted to RF frequency in two stages. Base band signals are first up-converted at an intermediate frequency (IF) and IQ-modulate by IF mixers and 90° phase shifter. The IQ modulated signal is then converted to the RF frequency.

Digital registers parameterize the IF mixer gain and the frequency divider ratio.

4 WCDMA TRANSCEIVER MODELING AND VALIDATION

This part presents the behavioral system modeling and its validation. The level of abstraction is first discussed; then an example of the model is presented. The conversion of datasheet parameters to electrical equations is described. To finish, different simulation and validation results are presented.

4.1 Abstraction level definition

The abstraction level must first be defined before developing the behavioral model. Behavioral level is always located between functional level and structural level. But, the gap between these two levels is large, so the abstraction level has to be precisely defined.

In our case, the abstraction level of the model is fixed by the transceiver datasheet. This datasheet is extracted from system specifications or 3G standard. Moreover, this datasheet defines each block specification thank to a "meet-in-the-middle" design flow. The modeling of system using parameters specified in this datasheet is a good compromise between complexity and accuracy.

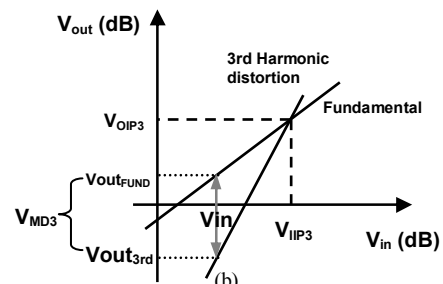
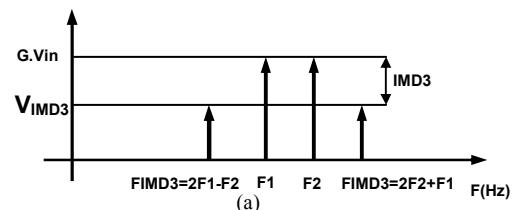


Fig. 5 (a) (b): IMD third harmonic distortion.

4.2 Transceiver modeling and validation

The transceiver architecture permits to identify three main blocks: amplifiers, filters and mixers. These blocks are modeled implementing specified parameters: impedances, IP, S-parameters, cut of frequency... The Commlib RF Mentor Graphics library is used to start developing these models [8]. However, these models must be adapted to our specifications. For example, designers define LO leakage (dBVp: Absolute voltage level in decibel) but the parameter used to model leakage in Commlib RF is the S_{13} parameter (dB).

4.2.1 Voltage Gain Amplifier IMD3 Modeling

In this part, the amplifier model from Commlib RF is modified to implement Intermodulation distortion IMD3. The parameter used to model the non-linearity in Mentor Graphics library is the Input Intermodulation distortion from the third harmonic Product (**IIP3**) in dBm. The 3rd order Intercept Point (IP3) is the point where the third-order term as extrapolated from small-signal conditions crosses the extrapolated power of the fundamental (Fig. 5). In our case, designers have specified Intermodulation distortion IMD3 from the third harmonic $V_{out_{3rd}}$ (dBVp). This parameter is the voltage value at a specific frequency ($2F_2+F_1$) with a specified P_{in} .

The $V_{out_{3rd}}$ is determined by putting a dual tone signal ($F_1=10.5\text{MHz}$ and $F_2=20\text{MHz}$) on the VGA input and measuring the voltage at a specific frequency ($F_{out}=1\text{MHz}$).

The IIP3 definition [10] is illustrated on Fig. 6. Then, it is possible to convert IMD3 in V_{IIP3} :

$$V_{IIP3} = \frac{V_{IMD3}}{2} + V_{in} = \frac{V_{out_{FUND}} - V_{out_{3rd}}}{2} + V_{in} \quad (1)$$

$$V_{IIP3_dBvp} = \frac{(Gain_{dB} + V_{in_dBvp} - V_{IMD3_dBvp})}{2} + V_{in_dBvp} \quad (2)$$

$$V_{IIP3_amp} = \frac{1}{2} \cdot 10^{V_{IIP3_dBvp} / 20} \quad (3)$$

The parameter V_{IIP3} converted in voltage (3) is then inserted in the output equation :

$$V_{out} = a1 \cdot V_{in} + a3 \cdot (V_{in})^3 \quad (4)$$

with $a3 = -\frac{4}{3} \cdot \frac{a1}{V_{iip3}^2}$ and $a1$: the voltage gain of the VGA.

To validate the IIP3 modeling and the IMD3 conversion, a simulation has been performed. The model validation is achieved varying the IMD3 from -120dBVp to 10dBVp and measuring the voltage at a specific frequency: $2F_1-F_2$ (1MHz).

On Fig. 6, the IMD3 variation is linear in the range from -120dBVp to -10dBVp . The answer is non linear after -10dBVp , due to saturation of the output signal.

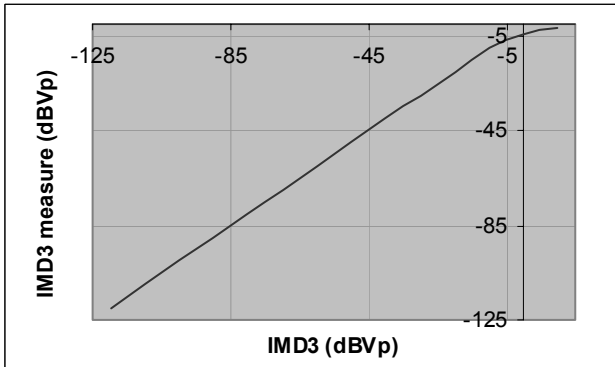


Fig. 6: IMD3 modeling validation.

```

Library IEEE;
Library IEEE_proposed;
Use IEEE.MATH_REAL.ALL;
Use IEEE_proposed.electrical_systems.all;
Use IEEE.STD_LOGIC_1164.ALL;

Entity LNA is
  Generic (
    -- Electrical parameters
    Gain : real := 15.0;           -- Gain
    Zin  : real := 50.0;         -- Input Impedance
    Zout : real := 50.0;         -- Output Impedance
    P_compression_dBm : real := -9.0; -- Compression point
    IIP3_dBm : real := 1.0;      -- Input IP3 (dBm)
  );
  Port (terminal in_p, out_p : electrical);
End Entity LNA;

Architecture bhv of LNA is
  -- Branch Quantities
  Quantity v_in across i_in through in_p;
  Quantity v_out across i_out through out_p;
  -- Free Quantities
  Quantity v_gain, v_comprese, v_out_imp : real;
  -- Gain calculation
  Constant a1 : real := 2.0 * 10.0**(Gain/20.0) * sqrt(Zout/Zin);
  -- Compression point conversion
  Constant P_compression : real := 10.0**((-30.0+P_compression_dBm 2.0)/10.0);
  Constant V_compression : real := sqrt(2.0*P_compression*Zout);
  -- IIP3 conversion
  Constant IIP3 : real := 10.0**(IIP3_dBm-30.0)/10.0;
  Constant V_IIP3 : real := sqrt(2.0*IIP3*Zout);
  Constant a3 : real := -4.0/3.0 * a1 / (V_IIP3 ** 2.0);

  Begin
    -- Current calculation
    i_in == v_in / Zin;
    i_out == v_out_imp/Zout;
    -- Compression Point
    if (v_in >= V_compression) use
      v_comprese == V_compression;
    elsif (v_in <= -V_compression) use
      v_comprese == -V_compression;
    else
      v_comprese == v_in;
    end use;
    -- Gain
    v_gain == a1 * v_comprese + a3 * (v_comprese ** 3.0);
    v_out == v_gain + v_out_imp;
  End architecture bhv;

```

Fig. 7: VHDL-AMS model of the LNA.

The VHDL-AMS source code of the Low Noise Amplifier is given in Fig. 7.

All the models of block are assembled together to built the transceiver RF front-ends. In the next section, simulation results are presented and compared to silicon prototype measurements.

4.2.2 RX/TX validation with RF stimulus

Comparison between measurements achieved on a real system prototype on silicon and simulation results are used to verify our system. All the simulations of our system use analysis conducted in the frequency domain. This kind of analysis allows us to decrease simulation time.

4.2.2.1 RX part gain validation

This first validation consists in measuring the RX gain. A single tone signal ($F=2113.4\text{MHz}$, $P=-80\text{dBm}$) is applied at the LNA input and a single tone signal ($F=2112.4\text{MHz}$) at the LO input mixer. The voltage at Q_{OUT} node (Fig. 4) is measured at 1MHz and the total gain of the system is then computed. Making the VGA gain varying from -7dB to 23dB , the total Rx gain is obtained by measurements and simulations (Fig. 8). In both cases the answer is linear and the gain varies from 41dB to 72dB . In theory, RX gain should vary linearly from 41.2dB to 71.2dB : the maximal relative error is less than 1%.

4.2.2.2 RX part IMD3 validation

The next validation concerns the IMD3 simulation. This validation consists of measuring third harmonic intermodulation distortion IMD3 for different values of VGA gain. A dual tone signal is put on the LNA input ($F_1=2123.4\text{MHz}$, $P_1=-40\text{dBm}$, $F_2=2133.4\text{MHz}$,

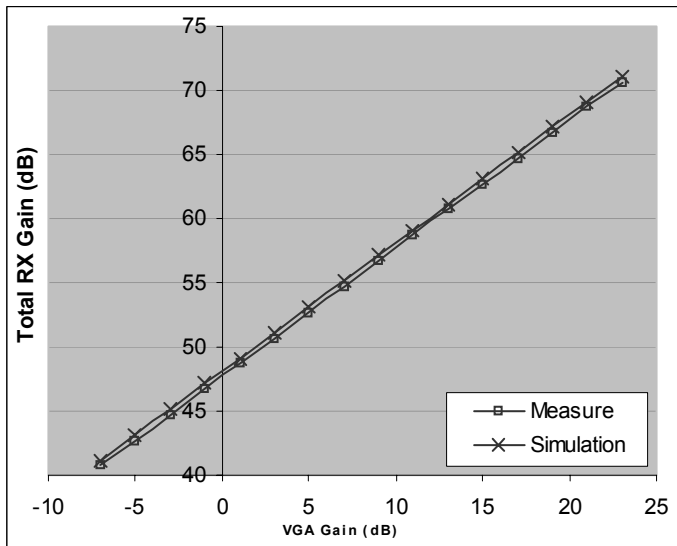


Fig. 8: RX gain simulated and measured versus VGA.

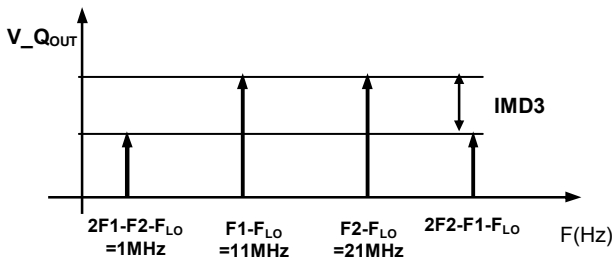


Fig. 9: Intermodulation distortion from third harmonic.

$P_1 = -40\text{dBm}$) and a single tone signal is applied at the LO input of the mixer ($F_{LO} = 2112.4\text{MHz}$). The IMD3 (dBV) is measured at $2 * F_1 - F_2 - F_{LO} = 1\text{MHz}$ (Fig. 9).

In Fig. 10, the amplifier gain varies from -15dB to 15dB and the IMD3 voltage is measured at 1MHz . In both cases, the answers remain linear and the IMD3 voltages vary from -62dB to -31dB .

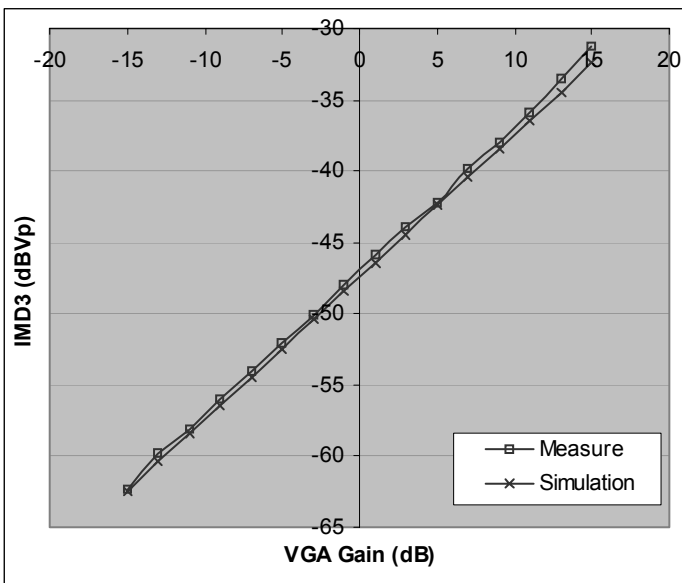


Fig. 10: IMD3 RX gain versus VGA.

The maximal relative error is 3% between the RX model simulation and silicon prototype measurement results. This simulation validates the non-linearity due to the IMD3 of the prototype.

4.2.2.3 Validation of the transmitter leakage

The Transmitter (TX) leakage validation consists in measuring the output signal at a specific frequency. The simulation is performed at the $F_{RF} = F_{LO} + F_{IF}$ frequency, and allows us to evaluate the leakage between the LO input and the output of the IF mixer (Fig. 4).

In that case, two single tone signals are put at LO input (F_{LO}), and at IF input (F_{IF}). Base-band single tone signals are also applied at the I and Q inputs (Fig. 4). The IF mixer gain varies from -54dB to 10dB and measurements are made at $F_{RF} = F_{LO} + F_{IF}$ frequency.

The maximal error between simulation results and measurements is 2dB ; this difference is due to the technology spreading on the silicon prototypes (Fig. 11). As the LO leakage of the prototype is behind the LO leakage of the transmitter model, thus we can conclude that the prototype suits the specifications.

Other similar simulations concerning offset compensation and gain accuracy have been carried out. Comparisons between simulation results and prototype measurements allow us to validate our Top-Down design.

4.2.3 RX/TX validation with "sequential stimulus"

In the previous section (s 4.2.2), transceiver validations have been presented. These simulations are conducted with pseudo-periodic input signals (single or multi-tone) and are based on the measurements of the signal powers at specific frequencies. In this section, digital input pattern is used to validate the transceiver model. Comparison between this digital input pattern and output signal allows the model validation. The analysis uses for these simulations is the modulated steady state, which has already been presented in part 2.2.2. Thanks to this analysis the simulation time is highly decreased.

4.2.3.1 Receiver simulation with digital patterns

The IQ modulated signals are generated using digital modulated sources from Eldo RF library. The digital input pattern is specified in a text file and this source modules this pattern. This signal is putted toward the RF input and the base band signal is measured. Fig. 12 presents the signal obtained at different nodes. The input

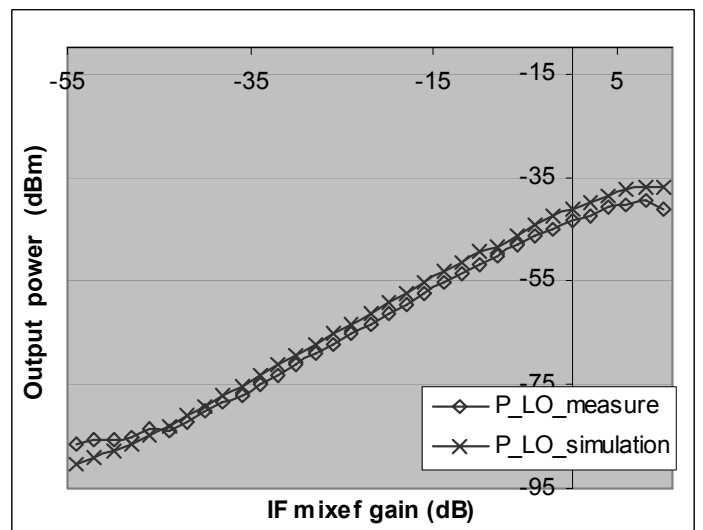


Fig. 11: Output power at LO frequencies versus IF mixer gain (TX).

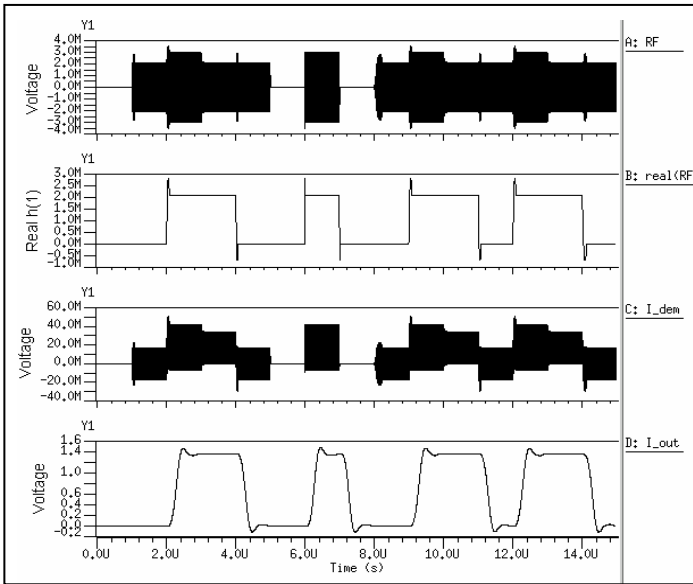


Fig. 12: Digital demodulation (reception chain).

signal (Signal *A* in Fig. 12 or RF node in Fig. 3) is the IQ modulated signal. Its frequency carrier is 2150MHz. Signal *B* is the real part of the RF input signal envelope, it represents the digital pattern used during IQ modulation. The input modulated signal is then demodulated; the mixer response corresponds to signal *C*. After amplification and filtering of this signal *C*, we obtain the base band signal *D*. The comparison between *B* and *D* signals permits to conclude that IQ demodulation works. Obviously, BER or eye diagram could be performed to completely validate the modulation and demodulation.

4.2.3.2 Transmitter simulation with digital pattern

In this section, the validation of the transmitter model relies on the modulation of a digital pattern. A digital pattern is put on the I input node (Fig. 4). The TX signals are presented on Fig. 13. Signal *A* is the input digital pattern. The base band signal is up-converted to F_{IF} frequency; signal *B* represents the modulated signal on node I_{mod}. I and Q channels are added in order to obtain the IQ modulating signal. Finally, the signal is converted to RF frequency (F_{TX}) signal

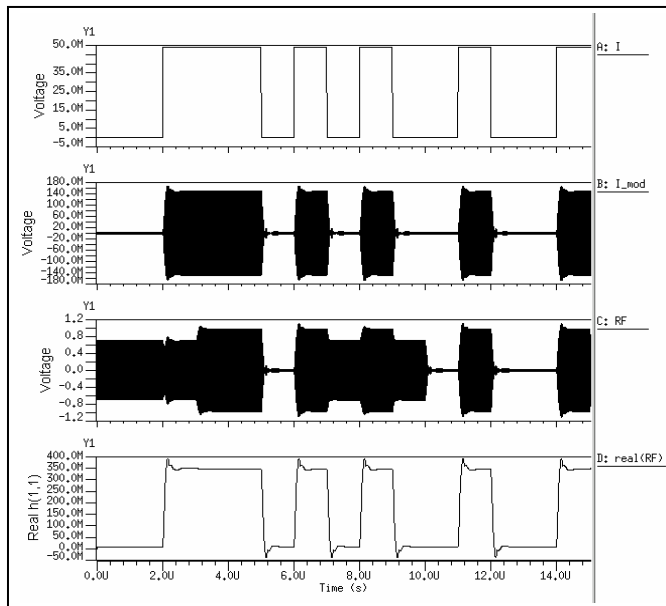


Fig. 13: Digital modulation (transmission chain).

C. This signal is the output signal; it is an IQ modulated signal at F_{RF} frequency. By extraction of the real part of the signal envelope, it is possible to obtain the IQ modulated digital pattern (signal *D*). This pattern is then compared to the input pattern (*A*) in order to validate the transmitter model.

5 CONCLUSION

The increasing integration of RF and mixed systems involves numerous design difficulties. The design of these highly complex systems lead to the use of a new design flow methodology: the Top-Down design flow. The model described in this paper fits in with this design flow. Behavioral modeling keeps the short time simulations from functional models and the accurate results of structural models. Specifications of a complete WCDMA communicating system have been implemented in a VHDL-AMS behavioral model. We validate the transceiver model comparing theoretical responses with measurements conducted on an integrated prototype.

This work contributes to the development of a VHDL-AMS RF component library that includes electrical parameters modeling used during ST Microelectronics RFIC validation flow.

REFERENCES

- [1] E. Normark, L. Yang, C. Wakayama, P.V. Nikitin, and C.-J. R. Shi, "VHDL-AMS modeling and simulation of a Pi/4 DQPSK transceiver system", pp. 119-124 in *Proc. IEEE Behavioral Modeling and Simulation Conf. (BMAS'04)*, San Jose, CA, Oct. 2004.
- [2] A. FAKHFAKH, "Contribution à la modélisation comportementale des circuits radiofréquence", Thesis, University of Bordeaux I, Ecole Doctorale Des Sciences Physiques et de l'Ingénieur, January 2002.
- [3] K. S. Kundert, O. Zinke, "The Designer's guide to Verilog AMS", CADENCE, pp 13-33, June 2004.
- [4] P. J. Ashenden, G. D. Peterson, D. A. Teegarden "The System Designer's guide to VHDL-AMS", MENTOR GRAPHICS, 2003.
- [5] J.J. Charlot, H. Levy, N. Milet-Lewis, T. Zimmer, "VHDL-AMS for mixed technology and mixed signal, an overview", MED'01, 9th IEEE Mediterranean Conference on Control and Automation, 27-29 juin 2001, Dubrovnik, Croatie.
- [6] "ADvance MSTM Reference Manual", Mentor Graphics, <http://www.mentor.com>
- [7] V. Beroulle, R. Khouri, T. Vuong, S. Tedjini, "Behavioral modeling and simulation of antennas: radio-frequency identification case study" pp 102- 106 in Behavioral Modeling and Simulation. (BMAS'03). March 2003.
- [8] MENTOR GRAPHICS, "CommLib RF VHDL-AMS Library", Manual, October 2005.
- [9] "3rd Generation Partnership Project; Technical Specification Group Radio Access Networks; User Equipment (UE) radio transmission and reception (FDD) », 3GPP, Mars 2003
- [10] Ken KUNDERT, "Accurate and Rapid Measurement of IP₂ and IP₃", The Designer's Guide Community, www.designers-guide.org/Analysis/intercept-point.pdf, May 2002.