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COMPENSATING THE TRANSMISSION DELAY IN NETWORKED CONTROL SYSTEMS

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Abstract: Recent interest in networked control systems (NCS) has instigated research in both communication networks and control. Analysis of NCSs has usually been performed from either the network or the control point of view, but not many papers exist where the analysis of both is done in the same context. In this paper an overall analysis of the networked control system is presented. First, the procedure of obtaining the upper bound delay value for packet transmission in the switched Ethernet network is presented. The upper bound delay algorithm applies ideas from network calculus theory. Next, the obtained delay estimate is utilised in delay compensation for improving the Quality of Performance (QoP) of the control systems. For the improvement of the performance a robust control based delay compensation strategy is used.

Keywords: Networked control systems, delay compensation, real time systems

1. INTRODUCTION

Automation systems of the future and even those currently in use today, will consist of a large number of intelligent devices and control systems connected by local or global communication networks. In these Networked Control Systems (NCSs), communications between process, controllers, sensors and actuators are performed through the network.

In most cases, the insertion of the network does not significantly affect the performance of the control system. However, for some time constrained systems (constraints coming from the dynamic of the physical process to observe and to control), the implementation of the NCS should be done considering the implications introduced by the network. For such systems, the insertion of the communication network into the feedback control loop introduces an additional delay, either constant or time varying, that makes the analysis and the control design more complex.

Studying the networked control systems requires the evaluation of the Quality of Service level provided by

the network and integration the values of these QoS parameters in the control design. One of the main limitations of the previous research on NCS is the lack of integrated control design and network evaluation. It is often assumed that either the control is specified (information timing constraints exists) or the performance of the network is well-defined (information about the delay distribution, uncertainty, deviation from mean value, missing value rate is assumed known). The results for the whole design cycle, where the network evaluation and control are integrated and performed the same context, are still lacking.

In this paper the whole design cycle for the NCS will be presented. A novel integrated approach will be presented where the estimated information about the network performance will be utilized in the control synthesis. First, the procedure of obtaining information about the delay (the upper bound delay) is presented and the obtained value is utilised in delay compensation. The delay algorithm presented applies ideas from network calculus theory, and the delay compensating strategies is based on robust control theory.

The paper is organized as follows: Chapter 2 is dedicated to introducing the upper bound delay estimation algorithm for the switched Ethernet network. In Chapter 3 the delay compensation strategy is introduced. Chapter 4 consists of the simulation results and discussion, and the paper ends with a concluding section in Chapter 5.

2. UPPER BOUND DELAY ESTIMATION

In the paper the switched Ethernet network is used as an example of the NCS network. The Ethernet networks are nowadays also more and more used in control applications and, in this context, it is important to understand the behaviour of the network in order to be able to control the network performance, such as delays (Georges et al., 2004). Next, the procedure of obtaining the upper bound delay over the network will be explained. The algorithm presented applies ideas from network calculus theory (see Cruz, 1991; Le Boudec and Thiran, 2001; Jasperneite et al., 2002). For more details of the algorithm, see Georges et al. (2005). First, the method to obtain a maximum delay for crossing a single Ethernet switch will be explained in Section 2.1, and the procedure of obtaining end-to-end delays in the network, based on the delays over the switches, will be given in Section 2.2.

2.1 Maximum delay for crossing the Ethernet switch

The first step in the Ethernet switch modelling is determination of an upper bound delay for crossing each of the basic components: FIFO multiplexer, FIFO queue, and demultiplexer. The upper bound delay over the switch is then the sum of the upper bound delays over these basic components, Figure 1:

$$\overline{D}_{switch} = \overline{D}_{mux} + \overline{D}_{queue} + \overline{D}_{output} \quad (1)$$

where the notation \overline{D} is used to represent the upper bound value of the delays.

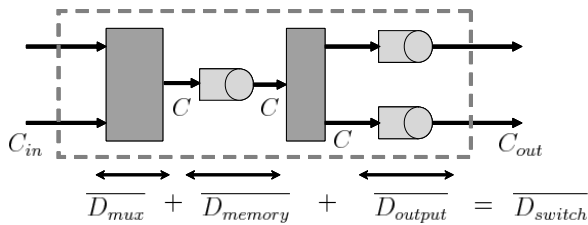


Fig. 1 Model of a 2 port-switch in a full duplex mode based on shared memory and a cut-through management.

In the mathematical analysis, the traffic arriving at the switch, both periodic and aperiodic is modelled as a 'leaky bucket controller'. Data will arrive at the leaky rate only if the level of the bucket is less than the maximum bucket size. Traffic models are called the

arrival curve in network calculus theory and, with the assumption that the traffic follows the leaky bucket controller and the incoming rate is limited by the port capacity, these curves are affine and have the form of:

$$b(t) = \min(C_{in}t - \sigma + \rho t) \quad (2)$$

where σ is the maximum amount of data that can arrive in a burst, ρ is an upper bound of the average rate of the traffic flow, and C_{in} is the capacity of the input port. In the same way, service curves are used to represent the minimal data processing activity of the components. Typical arrival and service curves are shown in Figure 2.

The approach is based on the evolution of a specific parameter, the backlog. The backlog is the number of bits waiting in the component, and it is a measure of congestion over the component. For the arrival curves in Figure 2, the upper bound backlog occurs at time t where the following line is a maximum:

$$b_1(t) + b_2(t + L/C_2) - C_{out}t \quad (3)$$

where b_1 and b_2 are the arrival curves of stream 1 and 2 at time t , L is the maximum length of the frames, C_2 is the capacity of the import port 2, and C_{out} is the capacity of the output link. When the upper bound backlog over the component is known, the upper bound delay over the component is then obtained by dividing the maximum backlog value by the capacity of the output link of the multiplexer. In a FIFO m-inputs multiplexer, the delay for any incoming bit from the stream i is upper-bounded by:

$$\overline{D}_{mux,i} = \frac{1}{C_{out}} \min_k \overline{B}_{mux,k} \quad (4)$$

where $\overline{B}_{mux,k}$ is an upper-bound of the backlog in the bursty periods u_k , such that $1 \leq k \leq m$. For $k = i$, the bursty period is defined by $u_i = \sigma_i / (C_i - \rho_i)$ and the backlog is upper-bounded by :

$$\overline{B}_{mux,i} = \sum_{z=1; z \neq i}^m \left(\sigma_z + \rho_z \left(u_i + \frac{L_z}{C_z} \right) \right) + u_i (C_i - C_{out}) \quad (5)$$

where σ_i is the burstiness of the stream i , ρ_i is the average rate of arrival of the data of stream i , L_i is the maximum length of the frames of stream i , and C_i is the capacity of the import port i . For $k \neq i$ such that $1 \leq k \leq m$, we have $u_k = \sigma_k / (C_k - \rho_k) - L_k / C_k$ and

$$\overline{B}_{mux,i} = \sum_{z=1; z \neq k}^m \left(\sigma_z + \rho_z \left(u_k + \frac{L_z}{C_z} \right) \right) + u_k (C_k - C_{out}) - \rho_i \frac{L_i}{C_i} + L_k \quad (6)$$

For the FIFO queue the delay of any byte is upper-bounded by:

$$\overline{D}_{queue} = \frac{1}{C_{out}} \frac{(C_{in} - C_{out})}{C_{in} - \rho_{in}} \sigma_{in} \quad (7)$$

For the demultiplexer it is assumed that the time required to route the output port is relatively negligible compared to the other delays, so that the demultiplexer does not generate delays.

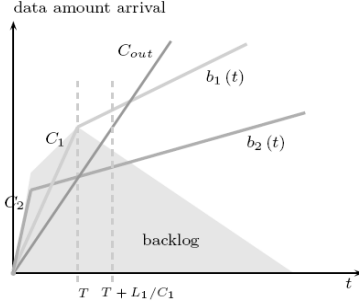


Fig. 2. Arrival and service curves and backlog evolution inside the two-input FIFO multiplexer.

2.2 Maximum end-to-end delays for crossing a switched Ethernet network

The computation of the upper bound end-to-end delays requires that special attention is paid to the input parameters of the previous equations. Indeed, the maximum delay value \overline{D} depends on the leaky bucket parameters: the maximum amount of traffic σ that can arrive in a burst and the upper bound of the average rate of the traffic flow ρ . In order to calculate the maximum delay over the network, it is hence necessary that the envelope (σ, ρ) is known at every point in the network. However, as shown in Figure 3, only the initial arrival curve values (σ^0, ρ^0) are usually known, and the values for other arrival curves have to be determined. To calculate all the arrival curve values the following equations can be used:

$$\begin{aligned} \sigma_{out} &= \sigma_{in} + \rho_{in} D \\ \rho_{out} &= \rho_{in} \end{aligned} \quad (8)$$

For example, for the arrival curve (σ^1, ρ^1) in Figure 3 the envelope after the first switch is:

$$(\sigma^1, \rho^1) = (\sigma^0 + \rho^0 \overline{D}_{switch}, \rho^0) \quad (9)$$

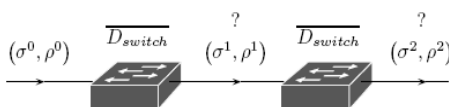


Fig. 3. Burstiness along a switched Ethernet network.

The last part of the method used to obtain the upper-bounded delay estimate is the resolution of the burstiness characteristic of each flow at each point of the network. First, the burstiness values are determined by solving the equation system:

$$\begin{bmatrix} a_{11} & a_{12} & \dots & a_{1n} \\ a_{21} & a_{22} & \dots & a_{2n} \\ \vdots & \vdots & & \vdots \\ a_{n1} & a_{n2} & \dots & a_{nn} \end{bmatrix} \begin{bmatrix} \sigma_1 \\ \sigma_2 \\ \vdots \\ \sigma_n \end{bmatrix} = \begin{bmatrix} b_1 \\ b_2 \\ \vdots \\ b_n \end{bmatrix} \quad (10)$$

and after solving the above equation, the upper bound end-to-end delays are obtained from

$$\overline{D}_i = \frac{\sigma_i^h - \sigma_i^o}{\rho_i} \quad (11)$$

where h is the number of crossed switches.

3. COMPENSATING THE ESTIMATED TRANSMISSION NETWORK DELAY EFFECT WITH THE ROBUST CONTROL BASED APPROACH

In this chapter the information available about the dynamic behaviour of the network, the upper bound delay estimate, is integrated in the control law. The main idea behind the approach is first to represent the communication network induced delays in the frequency domain as an uncertainty around the nominal plant. Information about the upper bound delay is utilized in formulating the representation of the uncertainty. Next, robust control methods are used to generate a control law that is able to meet the design specifications, to maintain the system performance, and to make the system insensitive even in the worst case disturbance for all the plants in the uncertainty set. The “worst-case” uncertainty is assumed to occur when the network delay equals the theoretical upper bound delay estimated by the algorithm based on network calculus theory. In order to facilitate understanding, the synthesis of both is done in continuous time. For implementation the obtained controllers should be discretized.

3.1 Problem formulation

The problem is studied from the controller point of view as a control problem in which the properties of the communication network have to be taken into account in the controller design. For the controller, the system that is actually being controlled, the system G_p , is a combination of the nominal plant (assumed to be fixed and certain) and uncertain (unknown, but bounded) dynamical effects of the network E . With the weighting functions, w_i , and normalized perturbations, Δ , the following expression for the networked controlled plant G_p is obtained:

$$G_p(s) = G(s)(1 + w_I(s)\Delta(s)); \underbrace{\|\Delta_I(jw)\| \leq 1}_{\|\Delta_I\|_\infty \leq 1} \quad (12)$$

3.2 Representing the network induced delay.

Next, information about the upper bound delay of the network is utilized in creating the weighting functions w_I . The weight can be obtained by finding the smallest radius $l_I(w)$ that includes all possible plants:

$$l_I(w) = \max_{G_p \in \Pi} \left| \frac{e^{UBD_1 s} G(jw) e^{UBD_2 s} - G(jw)}{G(jw)} \right| = \max_{G_p \in \Pi} |e^{UBD_1 s} e^{UBD_2 s} - 1|$$

$$l_I(w) = \begin{cases} e^{(UBD_1 + UBD_2)s} - 1; & w < \pi / (UBD_1 + UBD_2) \\ 2; & w > \pi / (UBD_1 + UBD_2) \end{cases} \quad (13)$$

And choosing the weight w_I such that

$$|w_I(jw)| \geq l_I(jw); \forall w \quad (14)$$

For example in this case the following weight can be chosen:

$$w_I(s) = \frac{(UBD_1 + UBD_2) \cdot s}{1 + (UBD_1 + UBD_2) \cdot s / 3.465} \quad (15)$$

This delay estimate was originally proposed by Wang, et al., (1994) to represent uncertain delays in the H_∞ framework in the design of robust controllers.

3.3 Controller synthesis

For a SISO case the controller synthesis problem can be solved in a relatively straightforward manner, since the SISO case with one complex multiplicative perturbation the Robust Performance (RP) problem can be approximated as a weighted mixed sensitivity problem where the condition is slightly strengthened:

$$\left\| \frac{w_p S}{w_I T} \right\|_\infty = \max_{\omega} \sqrt{|w_p S|^2 + |w_I T|^2} < \frac{1}{\sqrt{2}} \quad (16)$$

Where w_p is a weight for the sensitivity function S (usually an approximator of an integrator), and T is the complementary sensitivity function. For a MIMO case the use of a more complicated technique such as μ synthesis is required.

4. SIMULATION RESULTS AND DISCUSSIONS

In the simulations, the network of a real time process, a controller, and two overload traffic stations connected over a full duplex Ethernet switch, were used. The structure of the system is shown in Figure

4. To calculate the upper bound delay, the initial leaky bucket values of each stream were first identified. 6 are messages sent periodically. The traffic sent from the process to the controller is given by $b_1^0(t)$, and the traffic from the controller to the process by $b_2^0(t)$. The upper-bounds for these traffics will be computed in order to obtain the upper bounds, UBD_1 and UBD_2 . We consider also background traffic ($b_3^0(t)$, $b_4^0(t)$, $b_5^0(t)$, $b_6^0(t)$) from the stations to the process and to the controller in order to overload the network:

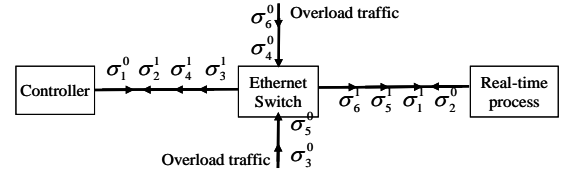


Fig. 4. The structure of the network

$$b_1^0(t) = b_2^0(t) = \sigma_1^0 + \rho_1 t = 72 + 7200t \quad (17)$$

$$b_3^0 = b_4^0(t) = b_5^0(t) = b_6^0(t) = \sigma_3^0 + \rho_3 t = 1526 + 305200t$$

Next, the route of each stream was identified and the output burstiness equations were formulated. After solving the burstiness values the end-to-end upper bound delay for streams 1 and 2 are:

$$UBD_1 = UBD_2 = \frac{\sigma_1^2 - \sigma_1^0}{\rho_1} \approx 3.5 \text{ ms} \quad (18)$$

In evaluating the effects of the network on the control system performance, the following model of a real time process and a nominal controller were used (time in ms):

$$P(s) = \frac{2}{(s+5)(s+0.2)} \quad C(s) = \frac{K_p s + K_I}{s}, \quad K_p = 0.5508, \quad K_I = 0.4529 \quad (19)$$

The delay compensation strategy based on the robust control approach was implemented by solving the mixed sensitivity problem in Equation 16. Equation 15 was used as a weighting function for the complementary sensitivity function T . As a weighting function w_p for the sensitivity function S the following approximation of the integrator was implemented:

$$w_p(s) = \frac{s/M + \omega_B}{s + \omega_B A} \quad (20)$$

Where ω_B is the bandwidth where control is effective, M is the desired maximum peak of w_b , and A is a small number used to avoid numerical problems. The H_∞ optimal controller for this mixed sensitivity problem was found using the MatlabTM Robust control toolbox.

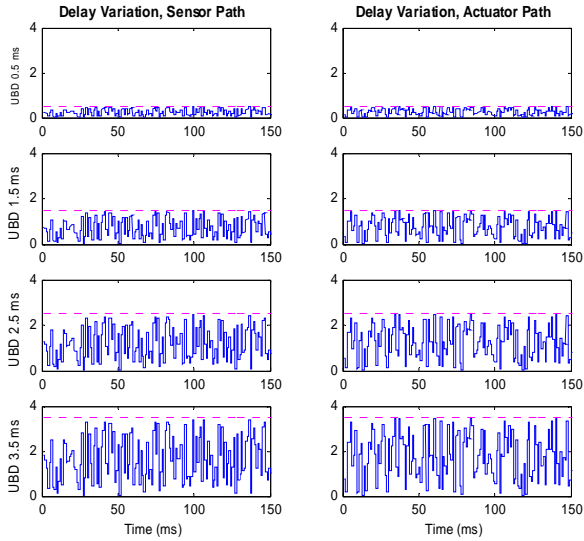


Fig. 5. Evolution of the sensor and actuator network delays.

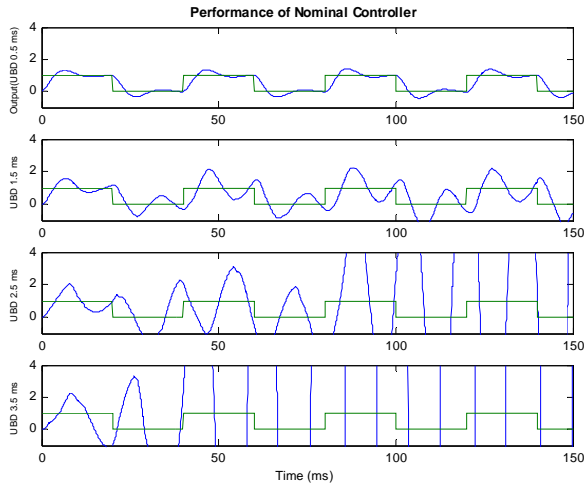


Fig. 6. Performance of the nominal controller as the delay increases

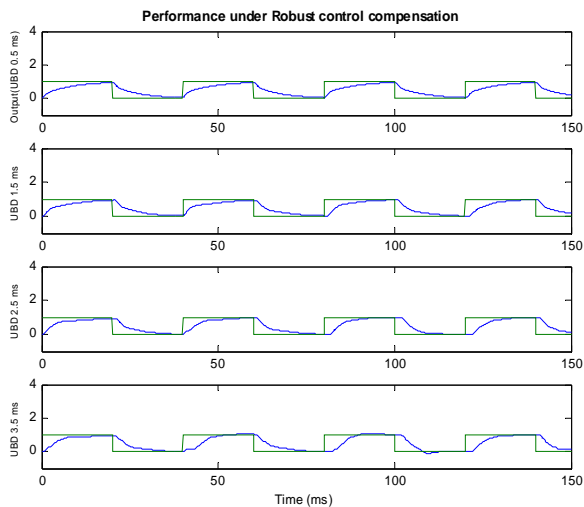


Fig. 7. Performance of the robust controller as the delay increases.

The simulation results are presented in Figures 5-7. Figure 5 shows the evolution of the sensor and actuator network delays, Figure 6 represents the performance of the system when controlled with a the nominal controller (Equation 19) as the delay increases, and Figure 7 indicates the performance of the robust controller as the delay increases. From the figures it can be concluded that the nominal system becomes unstable when the delay increases. The stability of the feedback control loop is regained when a delay compensation strategy such as the robust control based approach is implemented.

5. CONCLUSIONS

In this paper an analysis of the networked control system has been presented. A procedure for obtaining the upper bound delay value in the switched Ethernet network was presented, and the obtained delay estimate was used in the control compensation. Two control compensation strategies, the Smith predictor based compensation strategy and the robust control based compensation strategy, were presented and compared. It can be concluded that the upper bound delay estimate is an important measure of the networked control system which can also be used for the design and synthesis of a control system.

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