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# Non-destructive Failure Analysis and Modeling of Encapsulated Miniature SMD Ceramic Chip Capacitors under Thermal and Mechanical Loading

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**Abstract-** The use of multi-layer ceramic chip capacitors as integrated passive in e.g. system in package applications needs methods to examine and predict their reliability. Therefore, a non-destructive failure analytical technique is described to detect cracks in the ceramic and the metallic layers within encapsulated 0402 SMD capacitors. After choosing from techniques to reproducibly generate cracks, it is shown that an in-situ capacitance measurement is a convenient method to detect these failures unambiguously. Finite Element simulations support the experimental results. A reliability estimate for capacitor integrity under given loading conditions is given.

## I. INTRODUCTION

Multi-layer ceramic chip capacitors are often used as integrated passives in e.g. system in package (SIP) applications due to their small size but large capacitance. For these applications the capacitors have to go through an assembly and interconnection process, i.e. by adhesive or solder on e.g. a copper leadframe, followed by an encapsulation process (see figure 1), all of which pose potential reliability risks to the capacitor's structural integrity, as damage can lead to metal migration and much later to fatal failure by electrical shorts. Ceramic capacitors are known to fail due to failures caused during manufacture (cracks, voids) or extrinsic failures induced by overload during placing, thermal processing (e.g. soldering) or flexing on board-level (see e.g. [1]). For integrated passives, an encapsulation process is added to this, and molding compounds alter the stress state within a package, which may produce new reliability concerns or benefits (see e.g. [2]). This situation is depicted in figure 1.

To grant a reliable SIP packaging process, it is vital to know the lifetime of the component, and this implies concepts for testability and qualification. In this vein one needs a methodology to identify damaged miniature capacitors after packaging on a fairly large scale and in a rapid, preferably non-destructive way. A statement about reliability would come in handy. Such a method is what this paper aims at.

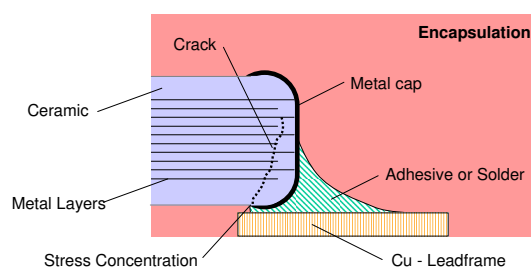


Fig. 1 *Schematic of a ceramic capacitor with typical flex-crack evolving at stress concentration due to thermo-mechanical loading. How can cracks be detected when an encapsulation is present?*

Investigations have been done for free-standing, non-encapsulated ceramic capacitors. Stress analysis as a function of material properties, mechanical loading and geometry has been carried out by experiment and simulation in [3] for 0805 or [4] for 0603 SMD capacitors. The focus of this paper, however, is to focus on the flex-crack detection of molded 0402 capacitors, facilitating their use for heterogeneous systems integration and SIP applications.

## II. METHODS OF FAILURE ANALYSIS

As illustrated in figure 1, the task faced by failure analysis is clear: A non-cleaving, compressed and most often skew

crack of several hundred microns length has to be detected across a layer of molding compound of at least half a millimeter's thickness within a capacitor of  $1 \times .5 \times .5 \text{ mm}^3$ . The need for non-destructive examination precludes unfortunately a priori the use of contact-less micro-deformation measurement, a method which would normally be ideal for non-cleaving cracks [5]. Scanning acoustic microscopy, although used for larger non-encapsulated capacitors [6], detects only boundary effects on that length scale but no failure. Curved surfaces of the metal cap and low frequency transducers needed for penetrating the mold further decrease intensity and resolution. Pulse IR thermography would not be able to detect flaws smaller in size to the thickness of the mold [7] (equal in size to the capacitor itself!). Laser-induced ultrasonic resonance [8] has been ingeniously used for free-standing capacitors of one single crack, but is unlikely to identify one within multi-interface SIP-structures. X-ray micro-computer tomography might succeed in theory, but it is not a method for large scale screening. Apart from that, adjacent layers with high absorption (AgPd-cap, SnAgCu-solder) may shield the minor changes in X-ray intensity resulting from the crack. An impedance or capacitance measurement [3] may be feasible if the crack manifests itself somehow, preferably unambiguously, in the capacitance value. This is not self-evident, especially a closed crack might not do so, even less when compressed by a molding compound. Still, as being a functional test and therefore non-destructive, this latter method will be investigated in this paper, as it also has the advantage to be rather simple, inexpensive and quick to be potentially eligible for larger scale examinations.

### III. CRACK GENERATION

Before non-destructive detection can begin, methods to prepare samples with cracks reproducibly generated have to be found. These cracks should go through the ceramic and the metal layers. As cracks are commonly introduced by flexure of the substrates the capacitors are mounted on, it is straightforward to check for controlled bending to generate cracks. In the following some of the investigated methods are briefly described:

#### A. Three Point Bending on Cu-plate

First, standard bending tests were undertaken [9]. So, a 0805 resistor was soldered to a copper plate (figure 2).

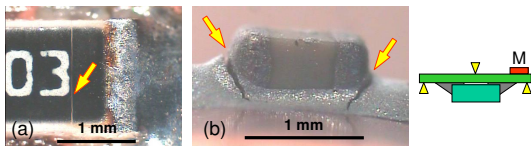


Fig. 2 Cracks (arrows) for 0805 soldered SMD resistor (a) and glued 0402 capacitor (b) after three-point bending.

In a standard testing machine performing the test

(Zwick 1446), the resistor duly cracked (a), the event being acoustically marked by a spike in the signal voltage of an attached piezo-microphone ( $M$ ). A glued 0402 capacitor, however, fails at the adhesive fillets (b). As this is not a brittle fracture, the microphone does not detect the event (not depicted). Soldering of this tiny component on non-structured copper did not work.

#### B. Shear Loading of Capacitor

Next, the capacitor was fixed within a shear tester (figure 3) (later also in cured epoxy) and a shear test was carried out, recording the shear force.

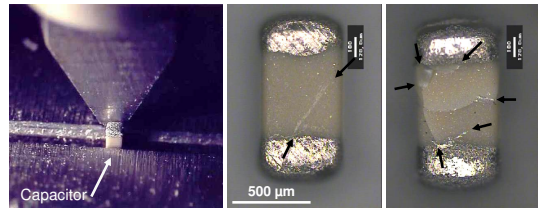


Fig. 3 0402 SMD Capacitor ( $1 \times .5 \times .5 \text{ mm}^3$ ) fixed in a shear tester. Crack patterns in capacitors to the right.

The test (figure 3) leaves the capacitors with not reproducible crack patterns and broken, i.e. not moldable. Shear forces extend over a range  $F \in [0.6; 1.3] \text{ N}$ . This may be due to difficulties in both fixing the capacitor and applying the force always in the same manner.

#### C. Three Point Loading of Capacitor

Then, a direct three point bending on capacitor level was attempted. To that the capacitor was soldered onto an especially designed organic test-board (FR-4). A fine but chisel was pressed downwards in the centre of the capacitor, allowing bending due to an undercut in the board.

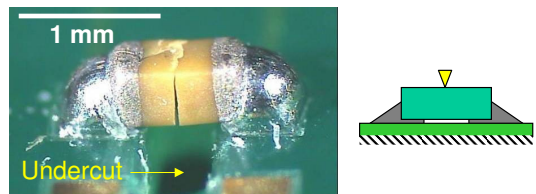


Fig. 4 Direct loading of the soldered capacitor by a blunted chisel applied in a testing machine.  $F = 47 \pm 1 \text{ N}$ , cf. [9].

The result can be seen in figure 4. A desired centre crack through the ceramic always appears, but it completely destroys the capacitor.

#### D. Three Point Bending of Board

As the solder joint proved sufficiently strong during the last experiment, three-point bending of the board is now performed. This set-up is depicted in figure 5.

Here, the damage done to the capacitor manifests itself

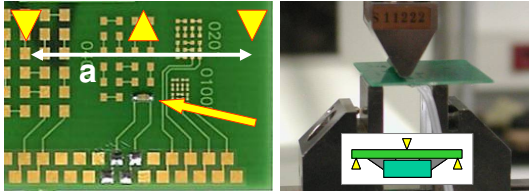


Fig. 5 Capacitor (arrow) soldered on board (0.8 mm thick) for concave three-point bending. Gap  $a = 20$  mm.

by a successive rupture of the individual metal layers from the metal cap (figure 6).

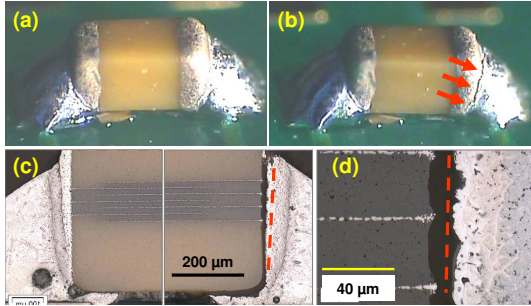


Fig. 6 Damage induced after three-point bending.

The crack can only be made visible in the microscope (c, d) if the capacitor is mechanically loaded (b). The cross section in this figure has been made using a clamp to make the crack cleave.

#### E. Outcome: Method of Choice

The method presented last was the only way of quickly, reproducibly and controllably pre-damaging capacitors. Although it is not the originally desired crack in the ceramic as depicted in figure 1, it is considered viable to test non-destructive failure analytical methods on these thus pre-damaged capacitors, as they can still be encapsulated by transfer-molding.

### IV. CAPACITANCE AND THERMO-MECHANICAL LOADING

The successive severing of metal layers should give rise to an easily measurable decrease in capacitance, thus facilitating in-situ monitoring during loading and unloading. So the set-up of figure 5 is complemented by an impedance-meter (Agilent 4294). The capacitance of the leads is below a measured  $C_{cable} < 10$  pF assuring accurate measurement of the capacitors in use ( $1.47$  nF). The result is depicted in figure 7, also showing force  $F$  and displacement  $d$ .

The damage clearly shows itself by a discontinuous decrease of the capacitance due to the successive tear-off of the metal layers. The process seems reversible in the sense that upon unloading the nominal value is reached again: The metal layers do successively re-contact the cap. This

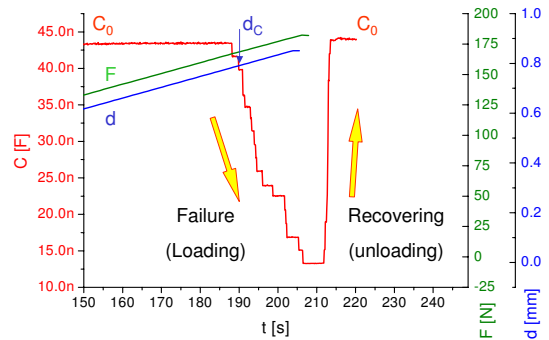


Fig. 7 In-situ capacitance measurements show a typical discontinuous decay from the nominal value  $C_0$  during mechanical loading.  $d_c = 0.85 \pm 0.1$  mm on 0.8 mm board.

leads to some very important conclusion: First, capacitance measurement is a potential and easy method to see cracks in a capacitor. Second, these cracks have to be mechanically loaded to show this effect and be detectable!

As mechanical loading is cumbersome for a large scale screening and potentially harmful for causing damage itself, one should look at a thermally induced mechanical load. In an encapsulated package, this thermo-mechanical stress will be the most important load case anyway. Exploiting the thermal mismatch between the capacitor and the organic board, the capacitor should experience a tensile force. So the capacitor is put on a hot plate and its capacitance monitored, albeit not continuously as before. The result is seen in figure 8.

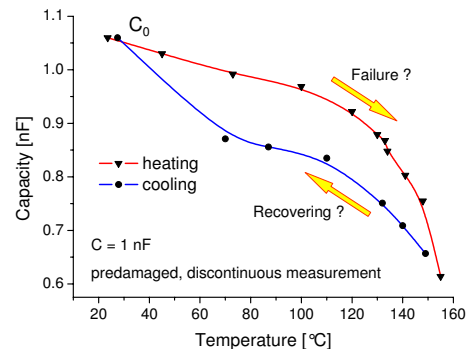


Fig. 8 Thermal loading of capacitor on organic board with  $C$ -recording in intervals. Damage cannot be clearly identified.

As the temperature is ramped up, the capacitance decreases. As the capacitance is only recorded at certain time intervals (to save memory and data channels), the evolving steps cannot be seen. Still, with comparison to figure 7, the drop in capacitance may already indicate damage. As will be shown further below, this is partially misleading, as ceramic capacitors show a pronounced temperature dependence with respect to the capacitance which could overlay the decay in capacitance due to damage. We now pro-



ceed to test the method on encapsulated capacitors and use thermo-mechanical loading to check for cracks.

## V. SIMULATION OF ENCAPSULATED CAPACITOR

First, an FE-simulation is carried out to evaluate the stress state of the capacitor. It is instructive to see its change with temperature. Material data were measured for that purpose. For the capacitor itself nano-indentation was used as only standard method applicable on that length scale (the metal cap measures only about  $20\ \mu\text{m}$  across). To extract the elasto-plastic material law, a coupled experimental-simulative procedure (outlined in [10]) was used.

TABLE 1 Material Properties

Material	Law	E [GPa]; $s_y$ [MPa]	CTE [ppm/K]	Tg [°C]	$\nu$	Method
SnAgCu	Visco-plastic	48	21		0.36	Tensile
Cu	Elasto-plastic	97; 180	16.5		0.35	Tensile
X7R BaTiO <sub>3</sub>	Elastic	113 ± 7	6.5*		0.3	N.I.
AgPd	Elastic	39 ± 5	16*		0.3	N.I.
Mold	Visco-elastic	26	8.5 < Tg < 30	122	0.3	Tensile
FR-4	Elastic	21	13 < Tg < 2.4	125	0.15	Tensile

*N.I.:* Nano-indentation. \* Data from literature [11].

The molding compound was modeled viscoelastically (figure 9). For the eutectic SnAgCu solder a viscoplastic secondary creep law was used. Please refer to our measurement data in [2, 12].

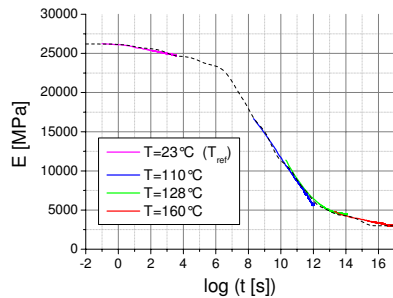


Fig. 9 Rate-dependent, viscoelastic behaviour of molding compound represented as mastercurve (Prony series). The high  $E$ -modulus indicates a highly filled epoxy resin.

As the simulation result, after cooling down from the stress-free point (at  $T_{\text{Cure}} = 175\ \text{°C}$ ) and relaxation at room temperature (RT), the maximum principal stress  $\sigma_1$  at are given in figure 10 after ramping up to  $T = 140\ \text{°C}$ .

At higher temperatures, notably at those above the glass transition temperature  $T_g$  of the molding compound (and board), there is a tensile stress (mostly, there is also shear stress) acting on the metal cap and the capacitor due to the CTE-mismatch between ceramic on one hand and the encapsulant and board on the other (see table 1). The tensile force is not distributed evenly across the metal cap but is largest at the bottom. So one could expect a gradual crack opening from the bottom to the top with increasing

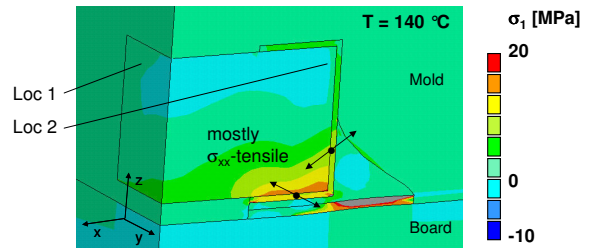


Fig. 10 *FE-simulation of molded capacitor (quarter symmetry)*.  $d_{\text{board}} = 0.8\ \text{mm}$ ,  $d_{\text{mold}} = 1.75\ \text{mm}$ . Around  $T_g$  of the mold, tensile stresses act on the cap (arrows).

temperature. This behaviour is once more depicted in the graphs in figure 11.

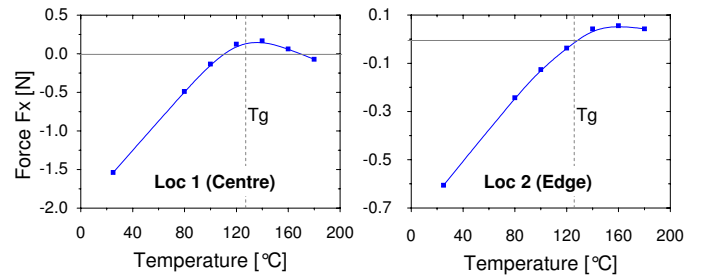


Fig. 11 Total force (in  $x$ -direction) on the capacitor.

Here, the total force acting on cross sections (in  $x$ -direction) of the capacitor is depicted as a function of temperature for two positions. As  $T$  goes up, the force on the central plane (loc. 1) and the cap (loc. 2) change from compressive to tensile, with an expected steep decrease in thermal mismatch around  $T_g \approx 122\ \text{°C}$ . As the effect is present all along the capacitor, crack opening should occur irrespective of position. At higher  $T$  the force becomes compressive again, as the CTE of the board decreases sharply beyond its  $T_g$ . At no time are there any large tensile stresses in the ceramic ( $\sigma_{xx} < 10\ \text{MPa}$ ), whereas compressive stress reaches e.g.  $\sigma_{xx} \approx -40\ \text{MPa}$  at RT. So the mold stabilizes the capacitor against flex cracks.

## VI. MEASUREMENT OF ENCAPSULATED CAPACITOR

Now the test-board (depicted in figure 5), with hand-placed and soldered capacitors, is encapsulated with a molding compound, the circuitry allowing in-situ capacitance measurement as before. The board is then stuck to a hot plate with a tacky thermal pad. The temperature is measured by an IR camera (figure 12).

Two different kinds of encapsulated test-specimens were prepared:

- Test-boards with undamaged capacitors,
- Test-boards with pre-damaged capacitors,

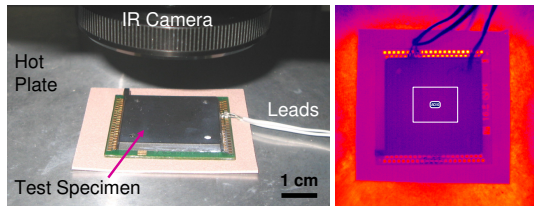


Fig. 12 Set-up for thermal loading of the encapsulated capacitor. The IR-image shows perfect temperature homogeneity across the package.

where pre-damaged capacitors were prepared as outlined in section III.D and IV. A representative three curves (out of more than  $N = 100$  undamaged molded capacitors) are given in figure 13.

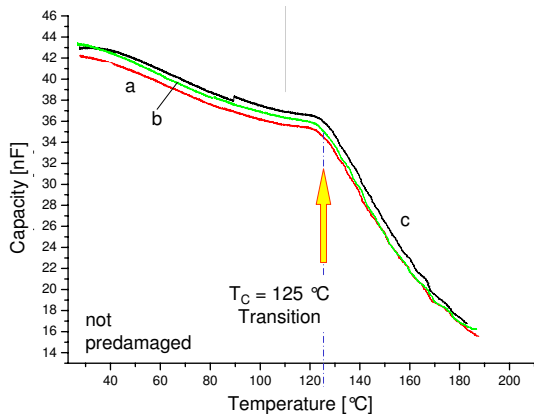


Fig. 13 Typical temperature dependence of the capacitance of non-damaged capacitors.

Conspicuous is the change in behaviour around  $T_C = 125 \text{ }^\circ\text{C}$  already mentioned in figure 8. The reason for this behaviour lies in the use of the ferroelectric  $\text{BaTiO}_3$  ceramic,  $T_C$  being its Curie temperature at (reversible) structural phase change. Due to dopants the transition interval is somewhat stretched, rendering the dielectric constant and thus the capacity a strong function of temperature.

As this is a continuous measurement and no steps are detected, the capacitors have survived the molding process intact. Different from this is the result from the pre-damaged capacitors in figure 14, where some representative curves are plotted.

First, it is clear that all pre-damaged capacitors show the discontinuous decrease in capacitance, which singles them out as damaged. The shape of the curve, however, can differ depending on how the capacitor was damaged. Capacitors  $d$  and  $e$  show a quick decay, whereas this is not the case for  $f$ . To tell a damaged capacitor unequivocally from an undamaged one, it is therefore necessary to perform a continuous measurement, although this may be costly with respect to time and memory.

One capacitor showed signs of damage after a second

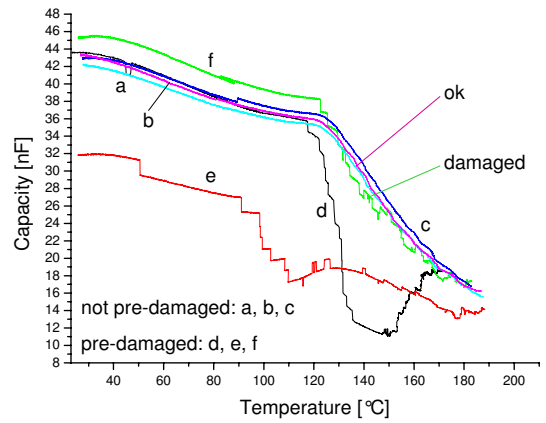


Fig. 14 Unambiguous detection of failure in encapsulated capacitors by discontinuities in the curves (cf.  $b$  vs  $f$ ).

measurement (figure 15). This could be due to intrinsic damage or damage induced by the soldering or molding process, gradually emerging, or even induced by the first measurement cycle, although  $T$  never exceeds  $T_{cure}$ .

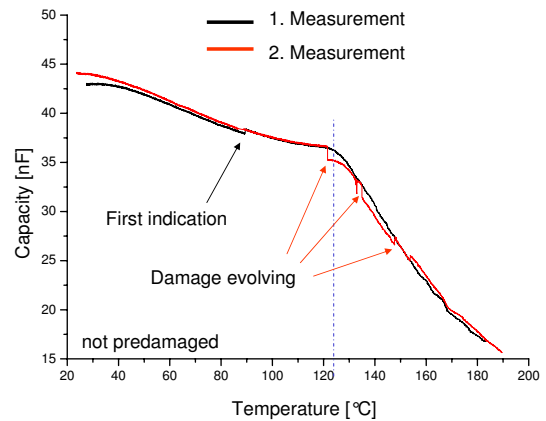


Fig. 15 Signs of minor damage after multiple loading.

A first sign can already be seen in the first measurement cycle (cf. curve  $c$ ).

## VII. EVALUATION OF FAILURE

Is it possible to use the data obtained in the experiments to make a statement about the reliability of these molded capacitors? In section III.D a three-point bending test has been described, tearing-off the metal cap, whereas fracture of the ceramic was not observed. Using the FE-model, without the mold, the stresses at critical displacement  $d_c$  can be evaluated. This shows some interesting results (figure 16).

First, the capacitor is loaded in compression at the top  $\sigma_{xx, top} = -30 \text{ MPa}$  and in tension at the bottom  $\sigma_{xx, btm} = 70 \text{ MPa}$ . That means, the solder acts merely as a hinge during bending, being itself not stiff enough to

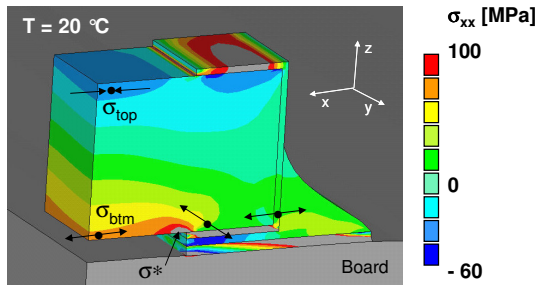


Fig. 16 *FE-model for convex three-point bending as in figure 5. Depicted are  $\sigma_{xx}$ -stresses at onset of damage (cf. figure 7).  $d_c = 0.9\text{ mm}$ . Material data as in table 1.*

communicate a bending force. Therefore, the cap starts tearing off at the bottom solder corner where large tensile stresses develop,  $\sigma_{xx,c} \approx 40\text{ MPa}$  being therefore a critical tensile stress for cap tear-off. Below the capacitor, the solder is loaded also in shear up to the expected stress concentration at  $\sigma^*$ . Taking the critical value for ceramic tensile fracture, a value of around  $\sigma_{xx,c} \approx 70\text{ MPa}$  [3] is found. This indicates, that in the bending test the critical value for ceramic fracture was just missed. (Although our test in figure 4 indicates slightly higher tensile strength if compared to [9].) Still, being nearly always in compression during service conditions, encapsulation of the presented kind should not affect the reliability of ceramic capacitors in that sense.

### VIII. CONCLUSIONS AND OUTLOOK

In this paper a method for non-destructive detection of cracks in molded SMD 0402 ceramic chip capacitors, e.g. SIP integrated passives, was presented. Fairly rapid, even small-scale non-destructive failure analysis of encapsulated miniature components with even smaller cracks proves challenging even for advanced methods. It was found, however, that continuous monitoring of the capacitance represents a convenient means to do so. During measurement, the package has to be heated up to exert a thermo-mechanical tensile strain which puts a force on the capacitor opening existing cracks which will then manifest themselves unambiguously in a capacitance decrease in discrete steps over temperature. The results, although obtained through capacitors soldered onto organic boards, should be qualitatively transferable on to capacitors glued to copper leadframes and overmolded as the underlying CTE relationships hold. Since it proved difficult to introduce cracks reproducibly into the ceramic, various methods of flexing have been attempted achieving cracks across the metal cap. Future tests should include capacitors with cracks through the ceramic body. However, simulation shows that this effect should also prevail for that case. Eventually, critical stresses were determined for the observed failure modes proving good reliability of ceramic capacitors inside a molded package.

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### References

- [1] C. Davis, S. Maloy, and J. Wegman. Common cracking modes in surface mount multilayer ceramic capacitors. Technical report, TDK, 2000.
- [2] T. Braun, B. Wunderle, K.-F. Becker, M. Koch, V. Bader, R. Aschenbrenner, and H. Reichl. Improved Reliability Of Leadfree Flip Chip Assemblies Using Direct Underfilling By Transfer Molding. *Proc. 31st IEMT, Nov 8-10, 2006, Putrajaya, Malaysia*, 2006.
- [3] N. Blattau, D. Barker, and C. Hillman. Lead Free Solder and Flex Cracking Failures in Ceramic Capacitors. *CARTS, 24th Annual Capacitor and Resistor Technology Symposium*, pages 101–105, 2004.
- [4] J.M.J. den Toonder, C.W. Rademaker, and C.-L. Hu. Residual Stresses in Multilayer Ceramic Capacitors: Measurement and Computation. *Journal of Electronic Packaging*, 125:506–511, 2003.
- [5] J. Keller, D. Vogel, A. Schubert, and B. Michel. *Applied Scanning Probe Methods*, chapter Displacement and Strain Field Measurements from SPM Images. Springer, 2003.
- [6] P. Ramirez and F. Adams. Acoustic Imaging and Screening of Ceramic Chip Capacitors. *Passive Component Industry*, pages 16–20, July/August 2002.
- [7] O. Breitenstein and M. Langenkamp. *Lock-in Thermography*. Springer Verlag, 2003.
- [8] D.S. Erdahl and I.C. Ume. Online-Offline Laser Ultrasonic Quality Inspection Tool for Multi-Layer Chip Capacitors. *52nd ECTC*, 2002.
- [9] EPCOS. *Effect of Mechanical Stress*, pages 217–222. Number 10/02. EPCOS Corporate Communications, 2002.
- [10] B. Wunderle, R. Mrossko, E. Kaulfersch, O. Wittler, P. Ramm, B. Michel, and H. Reichl. Thermo-Mechanical Reliability of 3D-Integrated Structures in Stacked Silicon. *Proc. MRS Fall Meeting, Boston, USA, Nov. 2006*, 2006.
- [11] Purdue Univeristy. Microelectronics Packaging Materials Database ‘CINDAS’, 1999.
- [12] A. Schubert, R. Dudek, E. Auerswald, A. Gollhardt, B. Michel, and H. Reichl. Fatigue Life Models for SnAgCu and SnPb Solder Joints Evaluated by Experiments and Simulation. *Proc. of 53rd ECTC, New Orleans, USA, May 27-30*, pages 603–610, 2003.