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High robustness PNP-based structure for the ESD protection of high voltage I/Os in an advanced smart power technology

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Abstract --- A new device dedicated to the ESD protection of high voltage I/Os is presented. In addition to the use of specific design guidelines, the concept consists in coupling an open-base lateral PNP with a vertical avalanche diode within the same structure to obtain a non-snapback behavior together with very good R_{ON} capabilities ($\sim 1\Omega$). The protection of high voltage I/Os with a narrow ESD design window ranging from 80V to 100V can be implemented in a reduced surface of $151 \times 140 \mu m^2$, which represents a state-of-the-art breakthrough.

Index Terms — ESD protection, High voltage I/Os, smart power technology, PNP bipolar transistor.

I. INTRODUCTION

A major challenge in smart power technologies is the ESD protection of high voltage I/Os in applications such as the automotive and Power-Over-the-Ethernet markets. To avoid latch-up issues, the clamping voltage of the ESD protection device should be above the power supply one and below the breakdown voltage of the component to be protected [1]. Given the constraints of the ESD design window, single SCRs [2] or NPN devices with strong snapback cannot be used or only in stacked configuration thus significantly degrading the on-state resistance of the resulting high voltage ESD protection and/or its area efficiency [3]. To cope with these issues, we propose an efficient no-snapback device. Using an optimized PNP transistor as a no-snapback ESD protection was already described in a previous work and specific design rules were defined [4]. One of the main drawback of PNPs is their much higher on-resistance compared to their NPN counterparts [5]. In this work, the proposed protection, developed in the most advanced smart power technology of Freescale, consists in a structure combining an open-base lateral PNP bipolar transistor with a vertical diode within the same active silicon.

II. DESIGN GUIDELINES FOR A PNP SELF-BIASED BIPOLAR TRANSISTOR

When used as an ESD protection, a bipolar transistor is self-biased by the avalanche current of the base-collector junction. The physical

parameters, which govern the snapback behavior, can be extracted from the analytical expression of the self-biased transistor. By making some simplifications (negligible recombination, no access resistance), an implicit bias equation (1) is obtained:

$$\alpha M = 1 + \frac{I_B}{I_E} \quad (1)$$

Where α is the common base gain (in self-biased configuration), M the avalanche multiplication factor, I_B the current at base contact and I_E the current at emitter contact.

Once the bipolar transistor triggers, its current characteristics snaps back to a lower voltage, called holding voltage, I_E becomes much greater than I_B and the on-state is equivalent to an open-base bias configuration. In particular, the holding voltage is determined by the two parameters α and M when satisfying the following condition:

$$\alpha M = 1 \quad (2)$$

Equation (2) shows that, to reduce the snapback (i.e. increase the holding voltage) two methods can be contemplated: lowering the gain α to increase the corresponding M value and then the voltage or use a device with a lower avalanche multiplication factor M so as condition (2) results in a higher holding voltage.

In general, NPN transistors are preferentially used as ESD protections for their very low on-resistance (R_{ON}). However, their high gain results in a strong snapback that is a major drawback to meet ‘high-voltage’ specifications. One way, to solve this problem, is to replace the NPN by a PNP. Both, the differences in gain and multiplication factor tend to reduce the snapback. In general, PNP transistors exhibit a weak or no snapback. However, they have a serious handicap lying in their very much higher R_{ON} related to the low mobility of holes carriers. In addition to this, high current injection effects occurring during an ESD stress induce a modulation of the space charge region leading to an electric field modification that results in an equivalent resistance. During an ESD

stress, the current induced charge in the space charge region could be as high as 10^{18} cm^{-3} . In smart power technologies, the doping levels are lower or in the range of this value, meaning that these high injection effects have a significant impact on the on-state resistance of the PNP device. A comparative study of the evolution of the current-induced charge into the base-collector space charge region allowed demonstrating a strong behavior difference between PNPs and NPNs [6]. As shown in Fig. 1, this evolution is similar in an NPN and a PNP as far as the current density is smaller than a critical current (Normalized current density =1). For higher values, the charge in an NPN monotonously increases, whereas the charge in a PNP decreases when a threshold current density is exceeded (Normalized current density =5.4).

For the case of the NPN transistor, the charge variation results in a continuous narrowing of the space charge region with current increase that tends to reduce the R_{ON} and is beneficial for the ESD protection performance. In the case of a PNP, the charge decrease occurring at high current density results in the widening of the space charge region, which has a detrimental impact on the R_{ON} .

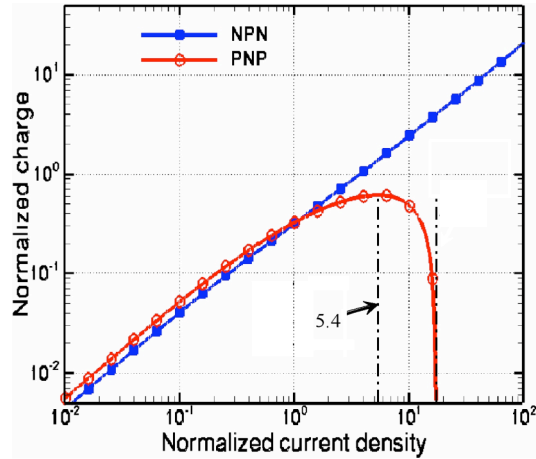


Fig. 1. Normalized current-induced charge in the base-collector space charge region versus normalized current density compared for NPN and PNP transistors [6].

PNPs were already explored as potential ESD protections but abandoned for this reason [3]. In a previous work [4], we defined four basic design rules to counterbalance the negative effects on R_{ON} :

- Minimize emitter length: given the low current gain, no ballast is needed for thermal stability.
- Maximize emitter perimeter in front of the collector.
- Use a low base doping and an abrupt collector doping profile.
- Suppress the base contact: thanks to the low current gain, there is no issue of leakage current increase.

Practically, this implies inter-digitized, or matrix (circular, hexagonal) configurations.

Using such design guidelines, area-efficient ESD PNP-based ESD protections were developed to protect high voltage I/Os of a smart power technology. The results are shown in Fig. 2 and Table I. For all devices, a very high HBM robustness is achieved, and for three of them it exceeds the tester capability (10kV). The on-resistance of the best device, DUT4, is 5Ω for a surface of $150 \times 100 \mu\text{m}^2$.

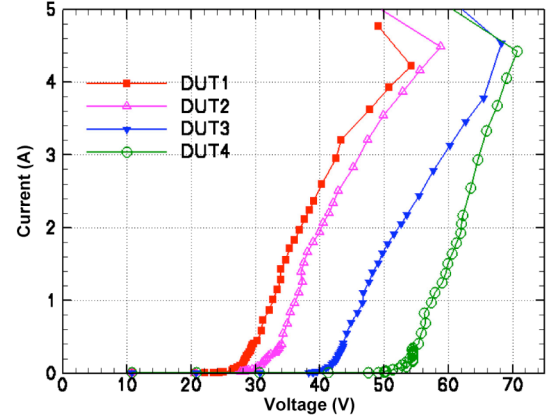


Fig. 2. TLP characteristics of four PNP-based ESD protection structures optimized for high voltage I/Os.

The obtained result is already satisfactory for protecting a 50V I/O but not enough for protecting an 80V one since it requires to stack two protections thus inducing a significant R_{ON} degradation. We then studied a way to improve the R_{ON} by implementing another current path in parallel with the PNP without increasing the footprint as described in the next section.

TABLE I
RESULTS OF HBM AND MM TESTING FOR THE DEVICES OF FIG. 2.

	DUT1	DUT2	DUT3	DUT4
V_{HBM} (kV)	9,5	≥ 10	≥ 10	≥ 10
V_{HBM}/S (mV. μm^{-2})	950	≥ 930	≥ 760	≥ 640
V_{MM} (V)	350	400	500	650
V_{MM}/S (mV. μm^{-2})	35	37	38	41

III. PRINCIPLE AND OPTIMIZATION

The proposed improved structure consists in a device combining an open-base lateral PNP bipolar transistor with a vertical diode within the same active silicon, as shown in Fig. 3. The technology is based on a P-type epi-layer on a P^+ substrate. An N^+ -buried layer and deep trenches provide insulation between the various active devices. The proposed PNP is composed of a deep P-type emitter diffused into the N-base that is left floating and the same deep P-diffusion is used as a collector. The avalanche diode is formed by the deep P-diffusion

and the N^+ -buried layer. Rigorously, in a floating base configuration, the diode is a vertical PNP transistor; however its base doping level is too high for a significant current gain. Hence the vertical structure can be reasonably approximate as a PN diode.

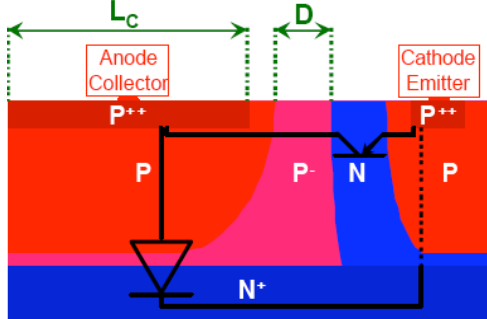


Fig. 3. Schematic cross-section of the lateral PNP transistor coupled to a vertical diode within the same structure.

Due to the non-snapback characteristics of the floating base transistor and the avalanche diode, both devices can operate concurrently and in parallel, provided that the PNP base-collector and the diode breakdown voltages are in the same range. As shown by the simulation result in Fig. 4, there are two current flows into the active silicon bulk, then allowing a significant R_{ON} reduction. Moreover, the most important feature concerning the R_{ON} reduction is the diode current contribution to the PNP bias current, leading to a great improvement of the current injection. In this arrangement, it has to be noticed that the diode is not implemented to help the PNP transistor triggering but to improve the on-state characteristics of the protection.

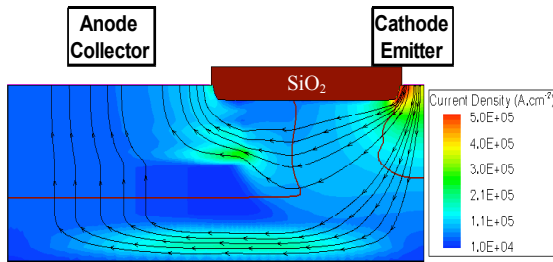


Fig. 4. Current density distribution, showing a lateral (PNP) and vertical (diode) current paths.

To take full advantage of this new feature, we can further minimize R_{ON} , through the optimization of the collector width L_C (Fig. 3), as it should be sufficiently wide to provide an important diode current without being detrimental to the total protection area. The second optimization consists in matching breakdown voltages of the PNP and the diode by adjusting the lateral distance D (Fig. 3). Regarding the diode breakdown voltage, the vertical doping profiles provided are technology

defined. Fig. 5.a shows the impact of the L_C distance on the R_{ON} . This parameter controls the diode area and then the maximum current it can handle. In this structure, the PNP breakdown voltage is not optimized (D distance) and it triggers before the diode at 30V; that explains the first high R_{ON} ($\sim 20\Omega$). When the diode triggers at 55V, the R_{ON} greatly improves and ranges from 7.4 to 2.4Ω depending on L_C . As expected, the failure current depends on the diode size. In addition, it was observed that increasing L_C beyond a certain value does not improve the R_{ON} value but allows increasing the failure current. Fig. 5.b presents the results for the optimization of the PNP breakdown voltage to make it trigger at about the same voltage as the diode. The larger distance D allows a concurrent triggering of both diode and PNP and thus directly entering into the low R_{ON} regime at turn-on. In this case, the triggering voltage can be adjusted without modifying the failure current that is an interesting property regarding the manufacturability. This trend is confirmed by the HBM and MM testing as summarized in Table II.

TABLE II

IMPACT OF DISTANCE D ON THE HBM AND MM ROBUSTNESS ($L_C = 18.3$ a.u.).

D (a.u.)	7.03	8.5	9.97
V_{HBM} (kV)	8.0	7.0	9.5
V_{HBM}/S (mV. μm^{-2})	680	570	740
V_{MM} (V)	500	500	450
V_{MM}/S (mV. μm^{-2})	42	41	35

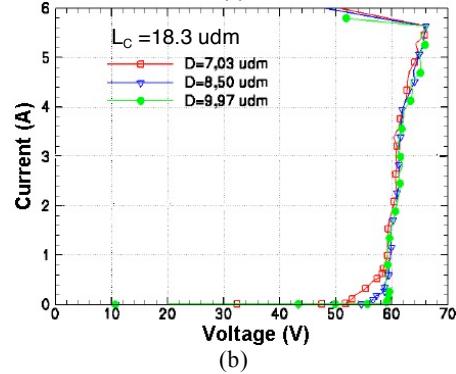
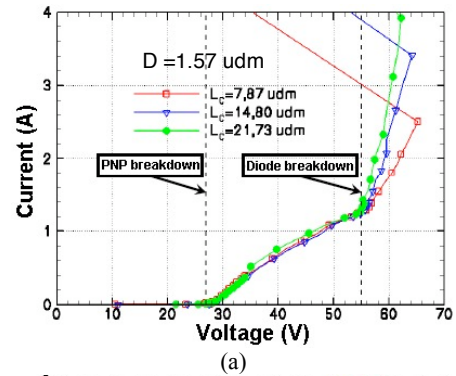


Fig. 5. TLP measurements showing the impact of the collector width L_C (a) and the distance D (b).

To evaluate the contribution of this coupling, we compared by simulation the currents of the standalone PNP, the standalone diode, the isolated PNP and diode in parallel and the coupled PNP-diode. It resulted that the current of the coupled PNP-diode is not the same as the one of the isolated devices in parallel. The coupling results in a significant current increase ranging from 41 % to 58 % compared to using the two isolated devices in parallel.

IV. MEASUREMENTS AND APPLICATION

The TLP characteristics of two improved structure are shown in Fig.6 and compared with the optimized PNP DUT4 of Fig.2 [4]. A R_{ON} reduction by a factor seven is observed: $0.7 \text{ m}\Omega\cdot\text{cm}^2$ for DUT4 and $0.1 \text{ m}\Omega\cdot\text{cm}^2$ for the improved PNP-diode component. Thanks to this low on-resistance, its measured HBM robustness is 8kV for a $100\times 100\mu\text{m}^2$ silicon area.

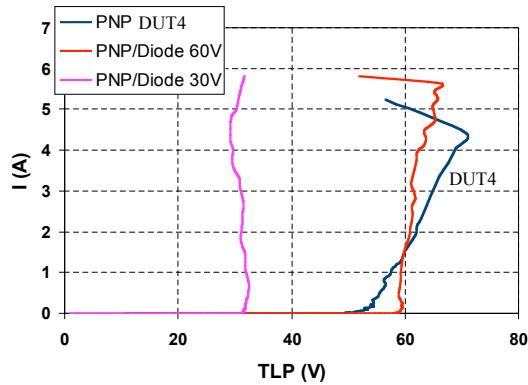


Fig.6. TLP characteristics of two optimized PNP-diode structures (30V and 60V clamping voltage) and of a standalone optimized PNP (DUT4 of Fig. 2).

Using this approach, PNP-diode protection devices with 30V and 60V clamping voltages were optimized (Fig.6) and taken advantage to develop a protection for a Power-Over-Ethernet application featuring an 80V-100V design window for 2kV HBM robustness. Stacking two devices with appropriate clamping voltages (30V and 60V) allowed meeting this specification as shown in Fig.7. The resulting on-resistance is 6.4Ω for a total surface of $151\times 140\mu\text{m}^2$, which corresponds at least to half of the surface required for a standard protection based on stacked NPN transistors. The HBM and MM robustness of the standalone structure is 6kV and 650V, respectively. To protect a device within the design window, the maximum HBM stress level is in the range of 2.5kV.

V. CONCLUSION

In this paper, we have demonstrated that a PNP-based protection structure can be greatly improved to provide a high ESD robustness for high voltage I/Os in an advanced smart power technology. By using specific design guidelines and coupling an open-base lateral PNP with a vertical avalanche diode, a low on-resistance (1Ω) can be obtained with a limited silicon area. This optimized structure was advantageously used to protect specific high voltage pins of a Power-Over-Ethernet chip.

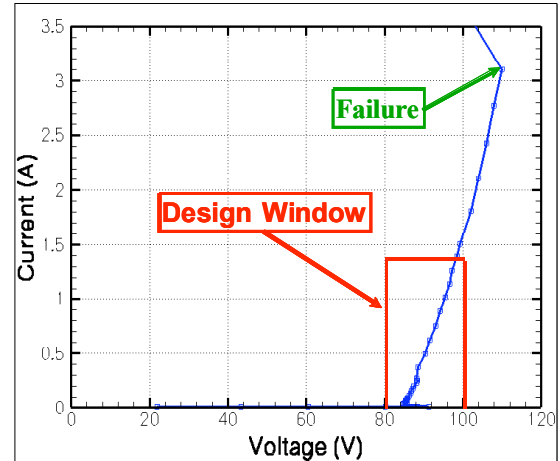


Fig. 7. TLP characteristics of the optimized protection for a Power-Over-Ethernet application using two stacked PNP-diode structures of 30V and 60V clamping voltages.

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