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THERMAL IMAGING OF Si, GaAs AND GaN -BASED DEVICES WITHIN THE MICROTHERM PROJECT

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ABSTRACT

Within the european project Microtherm, we have developed a CCD-based thermorefectance system which delivers thermal images of working integrated circuits with high spatial and thermal resolutions (down to 350 nm and 0.1 K respectively). We illustrate the performances of this set-up on several classes of semiconductor devices including high power transistors and transistor arrays in silicon, gallium arsenide and gallium nitride technologies.

operation of the integrated circuit itself produces local heat sources modulated at the working frequency f of the device. The circuit is illuminated by a monochromatic visible light. Since surface reflectivity is temperature dependent, the reflected light bears a small modulation at the frequency f , with an amplitude $\Delta R = \Delta T \cdot dR/dT$. This modulation can be detected with a lock in technique, or its spatially multiplexed equivalent if the CCD camera is triggered at the frequency $4f$. The thermal information can then be retrieved from these optical images by a numerical processing.

1. INTRODUCTION

Temperature is one of the key physical parameters which has to be addressed in the field of reliability of electronic devices. This concerns various domains of the semiconductor industry which include both high power devices (mainly GaAs, SiC, GaN and Si technologies) mostly for the telecommunication, aeronautic and aerospace markets but also the microprocessor industry (Silicon exclusively) where the dramatic effect of size shrinking and transistor density has made the heating problem one of the key points of their reliability.

The MICROTHERM project addresses two aspects in the field of thermal management for electronic devices:

- *Failure analysis*: The aim is to make high resolution thermal imaging in order to easily and precisely **locate** over-heated areas (hot spots) on a defective device.
- *Reliability Analysis*: Here the requirements are to precisely **measure** the temperature of the active part of a device in order to optimise its working point and life-time and to correctly size the associated cooling system.

For this purpose, we have developed a CCD-based Thermal-Photorefectance system which is able to deliver high resolution images of working integrated circuits. The

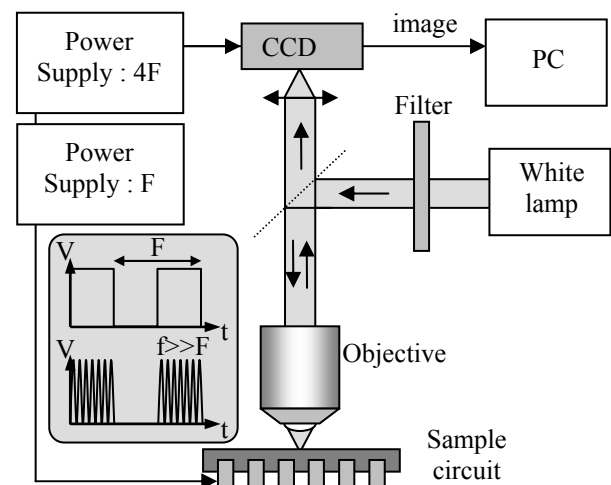


Figure 1: Experimental setup for thermal imaging by thermorefectance. The inset shows the two types of modulation used to power the electronic circuit in these experiments: either a simple low frequency modulation (F), or a high frequency (f) signal modulated by a low frequency carrier (F).

2. OPTIMIZATION OF THE ILLUMINATION

The choice of the illumination wavelength is a very important step in the measurement process. It is essential to choose a wavelength for which dR/dT is large to obtain a thermal signal. The optimal wavelength can be very

different for each material present on the sample surface, mainly because optical interference in the transparent encapsulation or intermetal layers [1, [2] drastically modify $R(\lambda)$ and $dR/dT(\lambda)$. The setup shown in figure 2 was specially designed to measure these coefficients and therefore enable a rapid choice of the optimal illumination wavelength. In this experiment, a slit is introduced in the Köhler illuminator of the microscope. This line is imaged on the sample surfaced and the reflected light is dispersed by a transmission grating. The prism has a low dispersion compared to that of the grating. Its main role is to deflect the first order of diffraction, which would otherwise not reach the CCD, towards the optical axis.

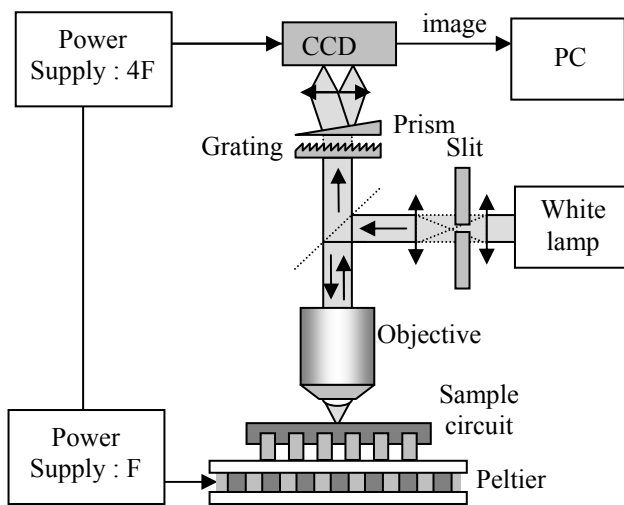


Figure 2 : Set up for the measurement of the wavelength dependence of $dR/dT(\lambda)$.

For each material studied here, we have conducted this kind of sensitivity study and chosen an optimal wavelength to conduct thermoreflectance measurements. In the examples shown below, Si-based transistors (figure 1) were studied at $\lambda=518$ nm, whereas GaAs transistors (figure 2) had an optimal thermoreflectance wavelength around 616 nm.

3. DEFECTS IN TRANSISTOR ARRAYS (ST)

Crystal defects are very harmful in present silicon devices when responsible for a source-to-drain junction piping and hence for a transistor leakage current. In particular, the geometry of the patterns of integrated transistors is found to be a key issue in the formation of crystal defects, both in experiments and in numerical simulations [3, [4]. These effects are difficult to characterise with existing methods. Photoemission spectra can reveal such defects, but the method is relatively slow and lacks sensitivity.

Leakage can induce high current densities and therefore localized heating, which can remain highly confined due to the thermally insulating dielectric environment of some transistor features. Therefore, thermal methods can be an interesting alternative for the study and localization of these defects.

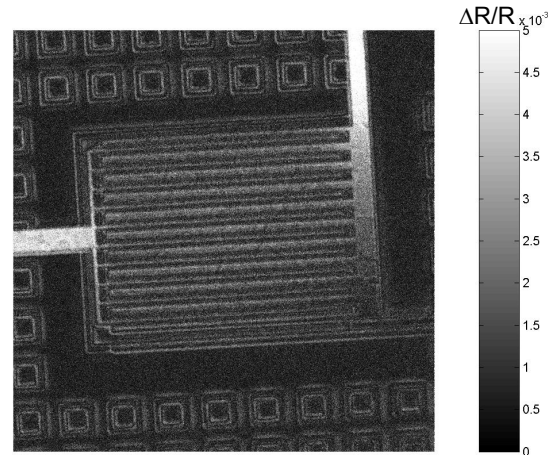


Figure 3: Thermoreflectance image of a non defective structure observed under a x50 objective (50x50 μm).

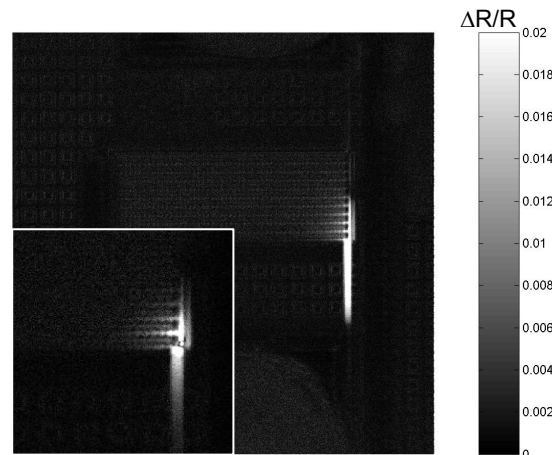


Figure 4: defective structure (135x135 μm). Inset : zoom (42x42 μm) on an image obtained on the same sample 20 minutes later : the shape of the hot spot has changed due to intense heating and source-to-drain leakage. Resolution: 350 nm (FWHM width of the smallest details). These active regions are 6 μm below the Si_3N_4 surface of the sample.

Two transistor arrays including patterns critical for defect formation have been constructed and then characterised using our thermoreflectance microscope. However, since this technique measures heating associated to defects, it does not discriminate dielectric breakdown and actual source-to-drain leakage. Both types of defects, buried

under 6 μm of intermetal and encapsulation dielectric were clearly detected with a spatial resolution of 350 nm. This is close to the ultimate resolution limit imposed by diffraction at approximately $\lambda/2\text{N.A.}=324$ nm, where $\lambda=518$ nm is the illumination wavelength and N.A. is the numerical aperture of the microscope objective (0.8 in our case). These two parameters set the resolution of the system, provided that the optics and the pixel size of the camera are sufficient to avoid further alteration.

In order to understand the physical processes that occurred in these samples and validate these measurements, post analyses (delayering) were conducted at ST Microelectronics. It appears that no breakdown occurred in non defective structures, as expected. In defective structures, two different phenomena appear to have caused the heating measured here: In one case, source to drain leakage was indeed observed. Another sample showed an oxide breakdown, possibly caused by static discharge, while a third sample had suffered from both effects. Since all these phenomena yield similar measurements, it is difficult to discriminate them. New structures with thicker oxide layers, which should be less subject to oxide breakdowns, have been made and are being characterised by thermoreflectance.

4. HIGH POWER TRANSISTORS (THALES)

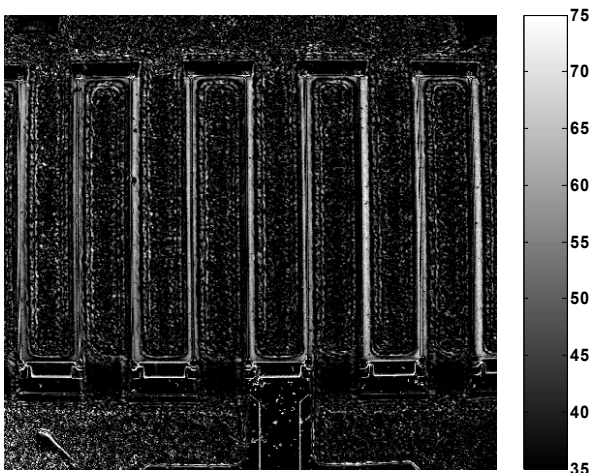


Figure 5: Thermal image of a GaAs power transistor (Thales) with $V_{\text{gate}}=V_{\text{source}}=0$ and V_{drain} modulated between 0 and 2V. After calibration ($dR/dT=7.10^{-4}$ K $^{-1}$), the colorbar gives the temperature on GaAs in K. The heating is clearly visible in the source-drain region.

In high power transistors, thermal management problems are crucial. New materials with better thermal properties, associated to thick metallic layers enabling a better evacuation of heat have improved the performances of these transistors. The source-to-drain recess is a

specially critical region where most of the heating is produced. However, since the metal layers are very thick, this region is actually a relatively deep (several tens of microns) and narrow (typically 1 to 10 μm wide) recess. Scanning probe measurements are impossible with conventional probes since they cannot reach the bottom of this recess. One of the purposes of Microtherm was to develop probes for this purpose [5]. Optical measurements are also difficult since artefacts and resolution degradation occur in this confined geometry.

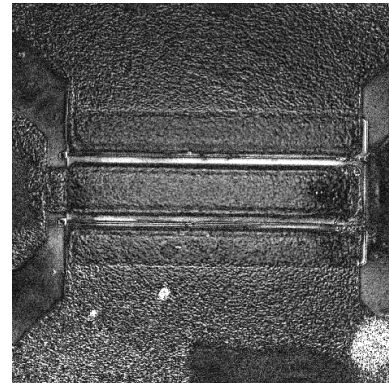


Figure 6 : Thermal image of a GaAs transistor (Thales) obtained with a high frequency V_{drain} signal ($f=500$ MHz), modulated intermittently at $f=2.5$ Hz.

We have measured the temperature of the active regions of these transistors using the two modes described in the inset of figure 1. The image of figure 5 was obtained on a transistor containing 9 intertwined gate, drain and source fingers, with a low frequency modulation of the drain voltage. At $F=7.5$ Hz, the temperature which is obtained is very similar to that of a device operating in DC regime. Figure 6 shows a simpler transistor with only 2 active regions. In this case, V_{drain} was modulated at a high frequency $f=500\text{MHz}$, sent in periodic bursts with a repetition frequency of $F=7.5\text{Hz}$. The photoreflectance is synchronized with this low repetition frequency, since the sampling rate of the camera is chosen at $4F=30$ Hz. In this case, the temperature variation which is measured is not the high frequency component which is actually very small at frequencies above a few 10 MHz as shown in earlier works [6]. We measure a temperature variation associated to the low frequency modulation F , which is therefore close to the DC temperature component of a circuit working at high frequency F . Similar experiments were conducted at frequencies up to 2GHz, but there is no practical limit to this frequency, since it is relatively easy to apply a low frequency chopping to any high frequency signal.

5. ACKNOWLEDGMENT

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