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## ELECTRO-THERMAL-MECHANICAL ANALYSIS OF A HQUAD PACKAGE FOR HIGH CURRENT AND HIGH POWER APPLICATION

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### ABSTRACT

The reliability for high electrical current densities through the first level interconnections using wire bonding was studied theoretically. First an analytical model was developed to give a first insight in the temperature rise in wire bonds under a certain electrical currents. Then a delicate 3D FEM model was built to employ the full electrical-thermal-mechanical coupling simulation. The thermal performance, temperature rising and stress distribution in the package were presented. The influence of wire material properties, diameter, and other adjacent materials (such as die attach, mould compound) are discussed. Based on our study, for a particular package solution HQUAD-64 requiring 3.3 A per wire, the best wire material would be copper. Beside, diameters of wires are playing important role. Wires with 25 $\mu\text{m}$  diameter are not capable to withstand for a long time, even when copper wires are used. While for using 50 $\mu\text{m}$  diameter wires, the maximum wire temperatures decreases by a factor 50 to 100 to reasonable but still high temperatures.

### 1. INTRODUCTION

The extension of existing smart power technologies towards higher current/power handling capabilities is a challenging and demanding task. A strong motivation for research in this field is the larger market segment for motor drivers that require current levels between 5 and 10 A. Under such high current loading, the reliability become a big concern: packages and interconnections are not yet capable of driving higher current levels; the higher current density, the higher junction temperature, the more chance for thermal-mechanical and electromigration failures of the interconnection and consequently the shorter the lifetime. So a better understanding is needed among the relationship between current density, operation temperature, and thermal resistance within a certain packaging.

At present stage high current packaging approaches are still using multiple wire bonds. The reliability of high current wire bonding is strongly related to the current density per cross-sectional area of the interconnection ( $\text{A}/\text{cm}^2$ ) and the operation temperature. Since the currently used wire is gold with a typical diameter of about 30 $\mu\text{m}$ [1], whether or not this configuration is still reliable for high current loading is unknown. The overall objective of this work is to demonstrate both analytical and Finite Element modeling techniques to understand the electrical-thermal-mechanical performance of high electrical current densities through the first level interconnections using wire bonding.

As a specific study case, HQUAD-64 package is chosen here for demonstration. This package consists of a silicon die, attached to the copper leadframe by using die attach material, and in a later packaging stage encapsulated in a mould compound. Wire bonding realizes the connection between the chip and the leads, while a highly conductive pad connects the leads to the PCB, which makes it suitable for power applications. An illustration for HQUAD-64 is shown in Fig. 1.

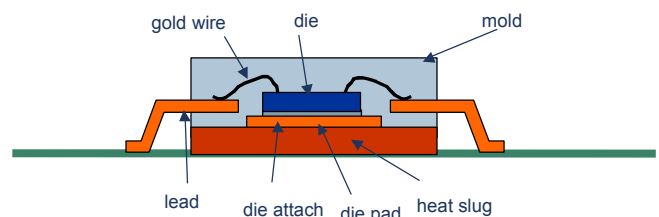


Fig. 1 cross section of the HQUAD-64 package

### 2. ANALYTICAL MODEL

A one-dimensional analytical model was developed to give a first insight in the temperature rise in wire bonds under a certain electrical current [2]. In this model, an infinitesimal section of the wire is represented in Fig. 2. Using the energy balance for the wire, as shown in Equation 1, means that the heat flux coming in from left

plus the heat generated by the current always equals to the heat flux coming out to the right and heat taking away to the surroundings by means of convection. Boundary conditions are different temperature at both ends of the wire and a uniform heat transfer coefficient along the full area of the wire. All input parameters for this analytical model are listed in Table 1.

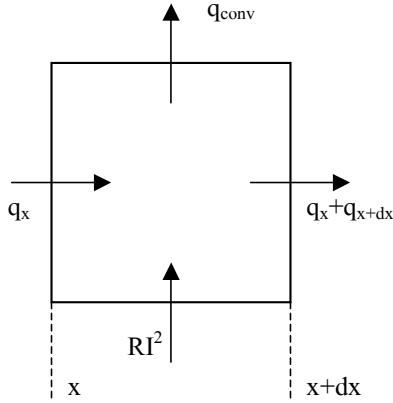


Fig.2: Simplified representation of the wire bond in the analytical model

Table 1: Analytical model input parameters

Parameters	Definitions	units
$q_x$	Heat flux at position x	W/m <sup>2</sup>
$A_d$	Cross sectional area	m <sup>2</sup>
$R$	Electrical resistance	$\Omega$
$I$	Electrical current	A
$P$	Perimeter of wire	m
$k$	Thermal conductivity	W/mK
$T$	Temperature	K
$\rho$	Electrical resistivity	$\Omega\text{m}$
$h$	Heat convection coefficient	W/m <sup>2</sup> K

Energy balance equation for an infinitesimal section of the wire with dx length:

$$q_x A_d + RI^2 = q_{x+dx} A_d + q_{conv} P dx \quad (1)$$

where

$$R = \frac{\rho \cdot dx}{A_d}$$

$$q_{conv} = h(T - T_{amb})$$

$$q_{x+dx} - q_x = \frac{dq}{dx} dx$$

turns out that

$$\frac{dq}{dx} dx \cdot A_d + h(T - T_{amb}) \cdot P \cdot dx = \frac{\rho \cdot dx}{A_d} \cdot I^2$$

thinking of heat flux as a function of temperature [3],

$$q_x = -k \frac{dT}{dx}$$

we have temperature T as a function of position x for the wire, as equation 2,

$$\frac{d^2 T}{dx^2} - \frac{hP}{kA_d} T = -\frac{hP}{kA_d} T_{amb} - \frac{\rho}{k} \left( \frac{I}{A_d} \right)^2 \quad (2)$$

The following equation needs to be solved:

$$\frac{d^2 T}{dx^2} - FT = G \quad (3)$$

$$\text{with } F = \left( \frac{hP}{kA_d} \right)$$

$$G = - \left( \frac{hP}{kA_d} T_{amb} + \frac{\rho}{k} \left( \frac{I}{A_d} \right)^2 \right)$$

The general solution for (3) is

$$T(x) = C_1 e^{\sqrt{F} \cdot x} + C_2 e^{-\sqrt{F} \cdot x} - \frac{G}{F} \quad (4)$$

Filling in the boundary conditions, where we assume that the local temperature distribution on leadframe and chip is homogeneous, then

$$x = 0 \text{ then } T = T_{chip}$$

$$x = L \text{ then } T = T_{lead}$$

$$T_{chip} = C_1 + C_2 - \frac{G}{F}$$

$$T_{lead} = C_1 e^{\sqrt{F} \cdot L} + C_2 e^{-\sqrt{F} \cdot L} - \frac{G}{F}$$

or

$$C_1 = T_{chip} + \frac{G}{F} - C_2$$

$$C_2 = \frac{(T_{chip} + \frac{G}{F}) e^{\sqrt{F} \cdot L} - \frac{G}{F} - T_{lead}}{e^{\sqrt{F} \cdot L} - e^{-\sqrt{F} \cdot L}}$$

The analytical model is used to make an interface where the maximum temperature in the wires is given after filling in the geometry, material properties and boundary conditions (see Fig. 3). The results of the analytical model show that the maximum temperature is in the middle of the wire, and that the maximum temperature is related to the square of the current and the square of the length of the wire. The main reason is that the produced heat has to be removed through the wires to the both ends.

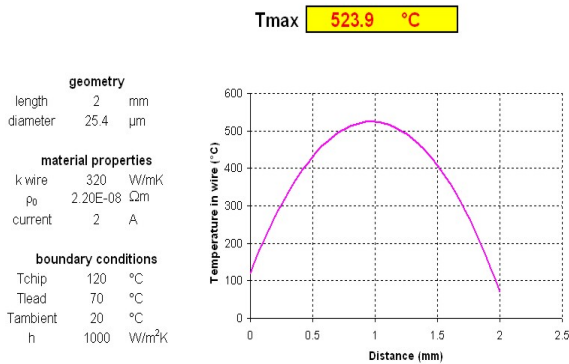


Fig. 3 Interface for calculating the maximum temperature in the wires

A finite element model of the simplified wire is used to verify the analytical results. Fig. 4 shows one of the simulation results. Electro-thermal finite element modelling of the wire confirms the results of the analytical model.

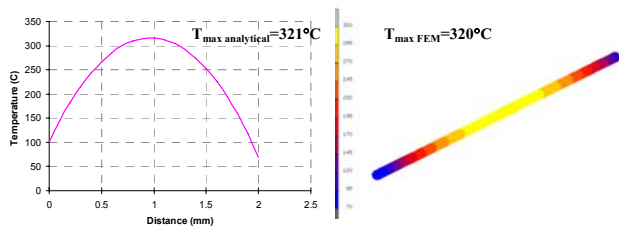


Fig. 4 Finite element model results for a 1 mil Au wire,  $T_{lead} = 70^{\circ}\text{C}$ ,  $T_{amb} = 20^{\circ}\text{C}$ ,  $h = 1000 \text{ W/m}^2\text{K}$ , length 2 mm, 1.5 A,  $T_{chip} = 100^{\circ}\text{C}$

### 3. FINITE ELEMENT MODELLING

A fully three-dimensional electro-thermal-mechanical FE model was created for the HQUAD-64 package. The commercial FEM code is Msc. Marc. Due to the symmetric, only one fourth of the model is simulated. This model consists of all the parts presented in Fig. 1; the chip is attached by a thin adhesive layer on a copper lead frame, which is soldered directly to the PCB with highly conductive pad. Six wires are constructed from a thin aluminum layer on the chip to the copper leads. Bonding wires and the chip are embedded in the mold compound materials. The FE model is presented in Fig. 5(a), and in Fig. 5(b), the mold compound was removed to reveal more details about the structure. As can be seen here, the mesh for the whole model is precisely controlled, which ends up only with 64000 elements -

fine mesh for places expecting high temperature gradient, like wire, copper lead frame, while comparatively rough mesh for the area where low temperature gradient is expected, like PCB.

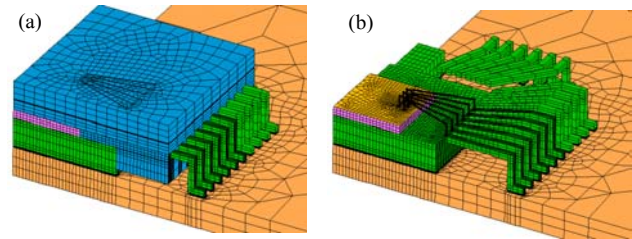


Fig.5 (a) FE model for HQUAD 64 package (b) when mold compound was removed for clarity

All the required material properties for the calculation are listed in Table 2. The most popular material for bonding wire are pure Au, doped Al and Cu, which were all considered in the calculations for comparison. Due to the limited wire diameter, the ohmic resistance of the wire is playing important role in the total resistance of the whole package, thus influences the temperature distribution. Therefore to achieve reasonable results, the temperature dependent relationship for electrical resistivity has to be considered, as shown in Fig. 6.

Table 2 material properties in the calculation

		$K$ W/mK	$c$ J/kgK	$\rho$ Kg/m <sup>3</sup>	$r$ $\Omega$ m	$E$ GPa	CTE ppm/K	Yield stress MPa
Wire	Au	320	130	19300	2.2e-8	78	14.2	150
	Cu	391	385	8920	1.8e-8	120	17.6	170
	Al	235	920	2700	2.6e-8	70	23.1	-
Chip	Si	150	699	2330	-	169	2.6	-
	Leadframe	Cu	391	385	8920	-	123	17.6
Solder	SnPb	50	226	7300	-	30	25.5	30
Overmould	0.8/3	1200	1300	-	-	18	17	-
PCB	20(xy), 0.2(z)	1000	1000	-	-	18	17	-

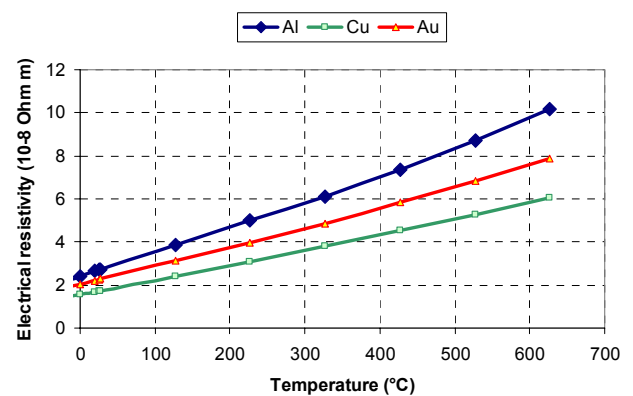


Fig. 6 Temperature dependent relationship for the resistivity of Au, Cu and Al

Boundary conditions in the simulation include a total current of 10A applied to 3 wires (3.3A per wire), while the other 3 wires are grounded. At the same time, the active surface of chip has constant heat dissipation as 2.5 Watts. The bottom temperature of the PCB is kept constant at 0°C. Msc. Marc allows having the coupling between electrical current that causes Joule heating, thermal heat power dissipation and the mechanical stresses that is induced by mismatched coefficients of thermal expansion between different materials and thermal gradients. When joule heating was calculated, resulted temperature distribution is used as the loading for the thermal mechanical calculation.

#### 4. MODELLING RESULTS

Material properties and diameters for bonding wires, properties for mould compounds, and die attach conductivity are the variable parameters in our simulation. In the following section, a study case was made for HQUAD-64 with a fix configuration, and its results are used to compare with results from other parameters. As a reference, bonding wire is 50µm in dimension, made of Au,  $k_{\text{compound}}=0.8\text{W/mK}$ , and  $k_{\text{die attach}}=50\text{W/mK}$ .

##### 4.1. Electro-thermal-mechanical modeling

The temperature distribution for the reference model is presented in Fig. 7. Regarding the temperature in the wires, similar results as for the analytical model are found. The maximum temperature is in the middle of the wire. Most of the heat has to go through both ends of the wires, while some go to overmould encapsulation. This temperature distribution results in stress concentration because of the different thermal expansion coefficient. The thermal-mechanical calculation gave the stress distribution on the wires, as shown in Fig. 8. The maximum stress is located also in the middle of the wire.

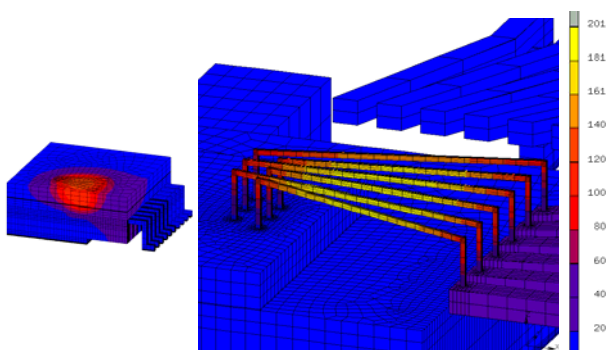


Fig. 7 Temperature distribution in HQUAD package (50µm, Au) (unit: °C)

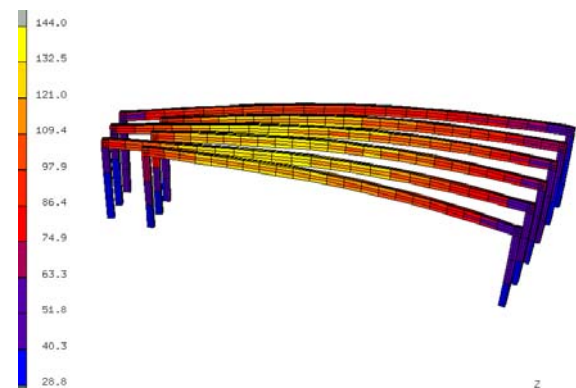


Fig. 8 Stress distribution in HQUAD package(50µm, Au) (unit: MPa)

##### 4.2. Parameters study for bonding wires

Changing from 50µm to 25µm in diameters for bonding wires results in a dramatic change in the maximum temperature, for Au, Al, and Cu, as shown in Fig. 9. This is because wire resistances increase in a factor of 4 when wire diameters decrease half, while the heat would even increase much more. The temperatures presented here for 25µm case are theoretical values, which could not happen in reality since they are already above the melting temperature of the materials. However, these values indicate that bonding wires' diameters can not be very small in order to keep the resistance of wires low in case that their lengths are limited. Moreover, to judge the material based on obtained maximum temperature, the best choice as wire material is copper, the worst is aluminum and somewhere in between the gold wire. The main reason is the electrical resistivity that is lowest for copper and highest for aluminum.

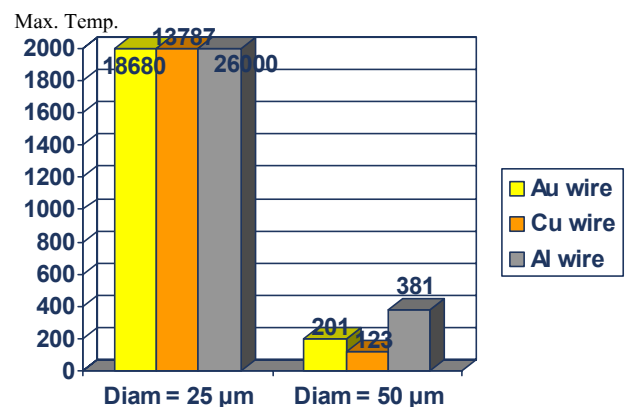


Fig. 9 Maximum temperature distribution in HQUAD package for 50µm and 25µm bonding wires. (unit: °C)

When looking at the maximum von mises stress in the wires, as shown in Fig. 10, Al gives the highest values, while the stresses for Au and Cu do not show much difference. It is due to the effect of different CTE. A simple analytical calculation was presented in Table 3. It implies that mechanical properties influence the stress, not only the temperatures.

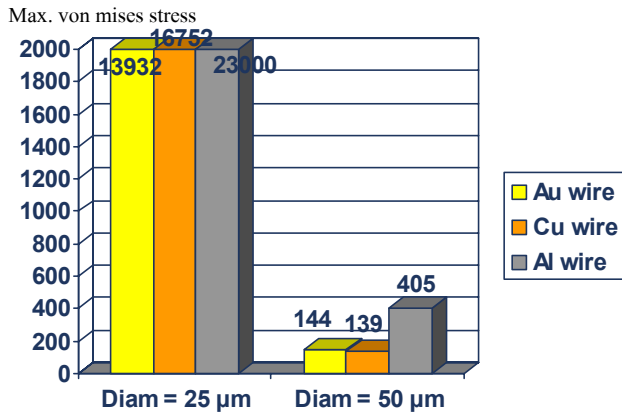


Fig. 10 Maximum von mises stress in HQUAD package for 50µm and 25µm bonding wires. (unit: MPa)

Table 3 Impact of CTE on the maximum stress

	Au wire	Cu wire	Al wire
ΔTemperature	201°C	123°C	381°C
Von Mises stress (FEM)	144MPa	139MPa	405MPa
CTE <sub>wire</sub>	14.2	17.6	23.1
	ppm/°C	ppm/°C	ppm/°C
ε <sub>th</sub> =CTE <sub>wire</sub> *ΔT	0.0028(-)	0.0020(-)	0.0088(-)
σ <sub>th</sub> =CTE <sub>wire</sub> *ΔT*E <sub>wire</sub>	219MPa	250MPa	616MPa

### 4.3. Influence of mould compound material

As the heat transfer from wires to the mould compound, the material properties of mould compound plays an important role. Using an overmould with higher thermal conductivity (> 3 W/mK) can decrease the temperature significantly. In Fig. 11, the maximum temperature in the wire was shown for k<sub>mould compound</sub> = 3 W/mK case.

Another study was done by changing the mechanical properties for mould compound. When the thermal conductivity keeps at 0.8W/mK, the Young's modulus change from 18Gpa, CTE 17ppm/C to 28Gpa CTE 7ppm/C, the maximum stress change from 164MPa to 144MPa.

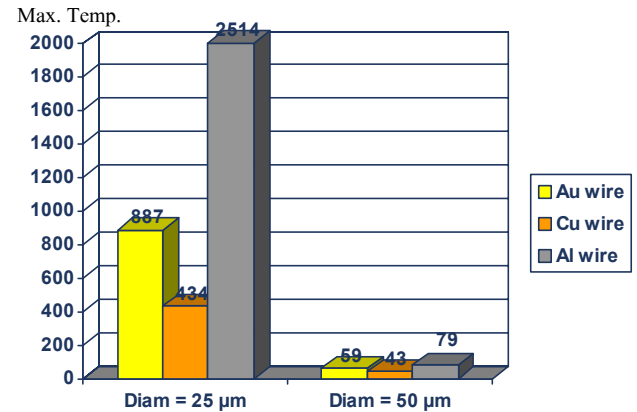


Fig. 11 Maximum temperature distribution in HQUAD package for 50µm and 25µm bonding wires. (k<sub>mould compound</sub>=3W/mK) (unit: °C)

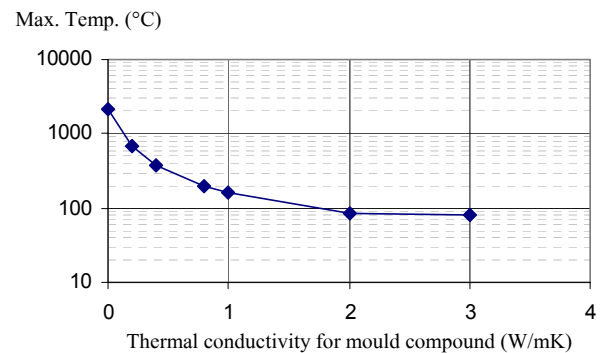


Fig. 12 Maximum temperature as a function for the thermal conductivity coefficient of mould compound

### 4.4. Influence of die attach

Thermal resistance R<sub>th</sub>(K/W) of the package is calculated with formula below,

$$R_{th} = \frac{T_{max} - T_{ref}}{P} \quad (5)$$

When chip dissipation power *p* and reference temperature *T<sub>ref</sub>* are known, the thermal resistance *R<sub>th</sub>* of the whole package can be calculated through Equation 5 by giving the maximum temperature *T<sub>max</sub>* in the package. In the calculation case shown in Fig. 13, the conductive layer between the chip and leadframe is 10µm thick, and its thermal conductive coefficient is 50W/mK (same as in the reference model). The thermal resistance is 0.14K/W when the maximum temperature 0.36°C is divided by the power 2.5Watts. Changing the thermal conductive coefficient of die attach to 0.5W/mK, the temperature distribution is present in Fig. 14. The thermal resistance for that case is much higher then, as 0.67W/K.

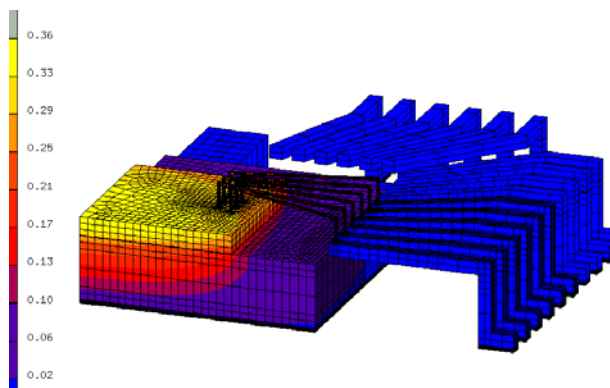


Fig. 13 the temperature distribution in the case that only chip power 2.5 Watts was applied ( $K_{\text{die attach}}=50\text{W/mK}$ ) (unit: °C)

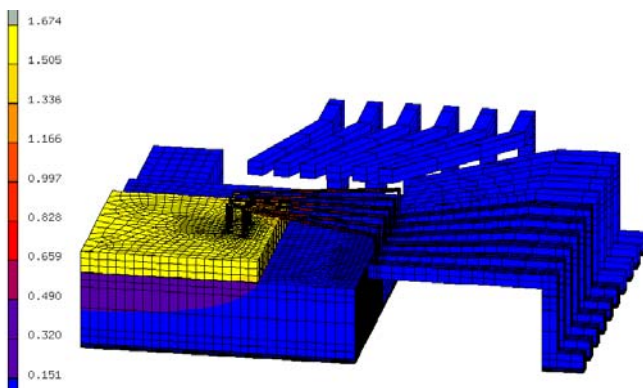


Fig. 14 the temperature distribution in the case that only chip power 2.5 Watts was applied ( $k_{\text{die attach}}=0.5\text{W/mK}$ ) (unit: °C)

## 5. CONCLUSIONS

For the reliability study for high electrical current densities through the first level interconnections using wire bonding, the influence of wire material properties, diameter, and other adjacent materials (such as die attach, mould compound) are discussed. The maximum temperature and the maximum von mises stress on the wire are presented. As expected, the best choice as wire material is copper, the worst is aluminum and somewhere in between the gold wire. The main reason is the electrical resistivity that is lowest for copper and highest for aluminum. For this particular package solution requiring 3.3A per wire, it was shown that wires with 25  $\mu\text{m}$  diameter are not capable to withstand a long time, even when copper wires are used. When using 50  $\mu\text{m}$  diameter wires, the maximum wire temperatures decreases by a factor 50 to 100. But using larger diameter wires would of course increase the cost for wires. So an optimal design for the wire bonding is

needed. Another way to decrease the temperature in the wire is to use the mould compound with high thermal conductivity.

Experimental work is on going to find out the failures because of high current loading on bonding wires, and the comparison between experimental work and simulation will be done in the near future.

## 6. ACKELEDGEMENT

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