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THERMAL MODELING OF POWER HYBRID MODULES

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ABSTRACT

Accurate prediction of temperature variation of power semiconductor devices in power electronic circuits is important to obtain optimum designs and estimate reliability levels. Temperature estimation of power electronic devices has generally been performed using transient thermal equivalent circuits. In this paper we have developed a simplified thermal model of the power hybrid module. This model takes into account the thermal mutual between the different module chips based on the technique of superposition.

1. INTRODUCTION

Design of power electronics systems involves numerous trade-offs as is common in most engineered systems. It proceeds through a careful selection process for various parameters and technologies starting with the electrical design and culminating in manufacturing process design. The electrical design phase results in the selection of power electronic circuit components, which is relatively mature and well established. However, rendering well-conceived electrical designs into reliable and low-cost products suitable for any application requires a substantial amount of additional engineering effort. The physical design proceeds further beyond the electronic circuit design, accounting for magnetic devices, current densities, dielectric isolation requirements, semiconductor power losses, thermal management methods, thermo-mechanical stresses, die-attach processes, electromagnetic interference, etc. Aforesaid factors that affect the design are coupled through complex interrelationships. Design activity encompasses several engineering domains including magnetic, electrical, mechanical, thermal, material processing, and manufacturing sciences.

In this paper we studied the thermal behavior of the power hybrid modules. The study lead to correct the junction temperature values estimated from the transit thermal impedance of each component operating alone. The corrections depend on the mutual thermal coupling between the different chips of the hybrid structure. It was noticed that the classic analysis of thermal phenomena in

these structures, independently of powers dissipated magnitude and boundary conditions, is not correct.

In the first part of the paper we have studied the thermal interactions between the module devices. Thermal 3D finite elements simulations have been made to observe the thermal influences between the different components of the module. These results will be compared with those obtained experimentally. An experimental technique, have been developed to estimate the thermal influences, caused by the different chips of the hybrid structure. This technique is based on the measure of IGBT and DIODE thermo-sensitive parameters.

In the second part of the paper we have developed a simplified thermal model of the power hybrid module. This model takes into account the thermal mutual between the different module chips based on the technique of superposition. It is obtained by the finite element method (FEM) and implemented in the MATLAB simulator. A 3D numerical simulations were made in order to shows the accuracy of the proposed thermal model.

2. THERMAL INTERACTIONS IN HYBRID STRUCTURES

In this paragraph, the thermal influence between the different components will be studied. A 3D finite element simulation are investigated to observe the evolutions of thermal influence according to the power dissipated in the component and according to the boundary conditions on the case of the module. The obtained results have been compared with these obtained by experiments.

A thermal investigation was done with the Semikron module SKM 75GB 123D (75A/1200V) presented in fig. 1. The studied module is an inverter leg having two IGBT and two diodes. The physical system is the superposition of six principle materials characterized by its thickness (W), its thermal conductivity (K) and thermal capacitance (ρCV) [1-3]. The program COSMOS/M [4] is used as a suitable 3D numerical simulation tool for the calculation of the temperature fields and the thermal influence between the different components. This software is based on calculations with finite element method. The top area of the device is divided into 91×31 cells permitting to discretise the (0.9×0.9) cm² active area of the IGBT

chip into 81 (9×9) elementary cells and the (0.6 × 0.6) cm² active area of the DIODE chip into 36 (6×6) elementary cells. In the case of studied devices (vertical structure), power is assumed to be dissipated at the top surface of the chip. In the perpendicular axis on this surface, the discretisation step is variable, it is low in the most active parts of the module and greater in the lower layer (case). All the thickness of the module is divided into 60 elements. The final structured mesh has 51884 elements and 57290 nodes.

At power feeding into the chip, the heating flow spreads out vertically to the module baseplate and also laterally from the heating source. So, a mutual coupling of the different chip happens inside the module. It can be seen that the thermal influences between components can exist when the adjacent devices operate together.

This thermal interaction depends mainly on:

- The dissipated power value in the different components.
- The silicon chip disposition.
- The boundary condition at the heat spreader.

a) Numerical photo of the studied IGBT module (SKM75GB123D).

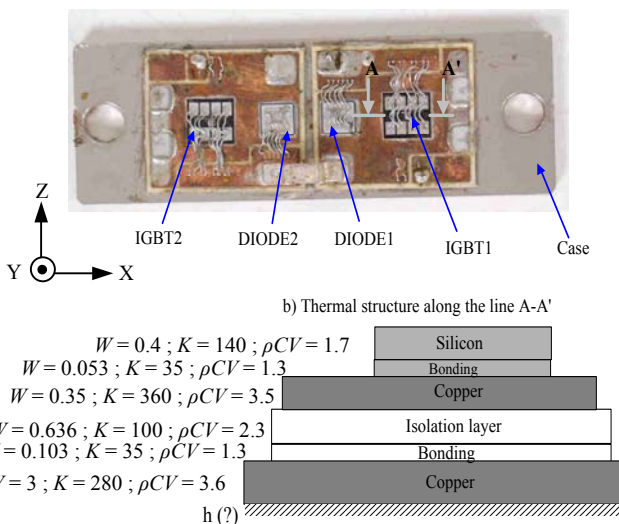


Fig. 1. Geometrical description and thermal structure of the studied IGBT module.

(W : in mm; K in $W.K^{-1}.m^{-1}$; ρCV in $J.K^{-1}.cm^{-3}$).

In figure 2 we have shown the possible thermal influence between the different components of the studied module. These influences are:

- Between the components in the top side of the circuit and the others in the bottom side.
- Between the components in the right side and the others in the left side of the circuit.

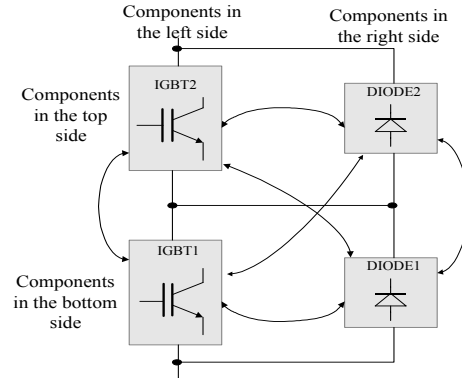


Fig. 2. Different thermal influences between the module components. \curvearrowright : Symbol of eventual thermal influence.

The developed experimental technique for estimating the thermal influences, caused by the different chips in the hybrid structure, is based on the measure of the IGBT and the DIODE thermo-sensitive parameters [5-7].

The component under the dissipated power causes the heating of its neighborhood. The measure of the thermo-sensitive parameter of the other components under this influence is performed. Figure 3 shows the experimental circuit used to measure the thermal influences between the components in the top side and in the bottom side of the circuit represented in figure 2. Indeed, when the switch *INT* is in position (1), component 1 is traversed by an important current (heating phase), and component 2 is off. In the steady state, the case temperature is measured by a thermocouple, the switch *INT* commutes to the position (2) and the thermo-sensitive parameter of component 2 is measured according to the circuit (voltage source: (V_1), resistance: (R_4) and component 2) conditions. If component 2 is the IGBT or the DIODE, a saturation current parameter measurement and a drop voltage measurement are performed respectively. Using calibrations characteristic, the thermal influence value between components is deduced [6].

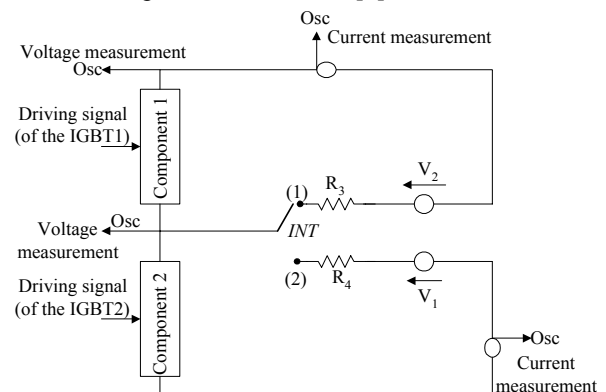


Fig. 3. Experimental circuit used to measure the thermal influences between the components in the top side and in the bottom side of the inverter (figure 2).

Figure 4 shows the thermal influence evolution of the IGBT1 on DIODE1 according to the power dispersed in the component and according to the boundary conditions at the case of the module. These results are obtained by experiments and by 3D numerical simulations. A good agreement between the two types of evolutions is observed. We notice that the equivalent resistance of the heat sink ($R_{\text{hea-IGBT1}}$) represents the thermal resistance between the case, just below the component under test, and ambient air (IGBT1 in the case).

The thermal influences between the different components are measured and are approximated a simple polynomial function, for example: In the case of thermal influence of the IGBT1 on DIODE1 (or IGBT2 on DIODE2):

$$\Delta T_{\text{IGBT1 on DIODE1}} = 0.96 * P_{\text{IGBT1}} * R_{\text{hea-IGBT1}} - 0.08 * P_{\text{IGBT1}} \quad (1)$$

Where P_{IGBT1} dissipated power in the IGBT1.

With $R_{\text{hea-IGBT1}} > 0$ (temperature of the case > temperature ambient). We notice that the magnitude of the thermal influence between neighbouring devices in the module structure is not negligible even for a low dissipated power magnitude. The good agreement between 3D numerical simulations and the experimental results proves that the simulated structure of the studied module is correctly modeled in the COSMOS/M simulator and the results obtained from these numerical simulations can be considered as a reference in our study.

Thermal influence ($\Delta T_{\text{IGBT1 on DIODE1}}$) in (K)

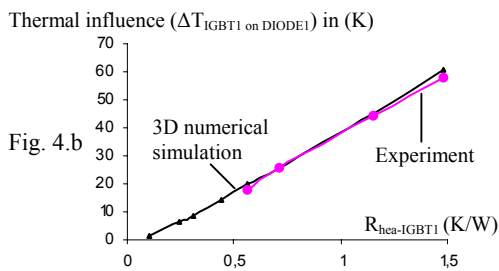
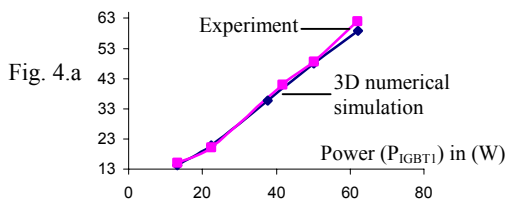


Fig. 4. Thermal influence evolution caused by the IGBT1 on the DIODE1 as a function of the dissipated power (fig. 4.a) and the boundary conditions (fig. 4.b).

Where $R_{\text{hea-IGBT1}}$ (K/W) represents the thermal resistance between the case, just below the component under test (in the case IGBT1), and ambient air and P_{IGBT1} dissipated power in the IGBT1 (W).

In figure 5 we have shown the effect of the boundary conditions, at the module base plate, on the effective thermal resistance of each device. These characteristics are deduced for different device dissipated power and performed with 3D numerical simulations. The devices thermal resistances increase when the dissipated power and the heat sink equivalent resistance increases.

From the characteristic of figure 5, the thermal resistance can be approximated by the following simple polynomial function as follows:

$$R_{\text{th-IGBT1}} = (1.34 * 10^{-3} * P_{\text{IGBT1}} * R_{\text{hea-IGBT1}}) + 0.28 \quad (2)$$

$$R_{\text{th-DIODE1}} = (3.19 * 10^{-3} * P_{\text{DIODE1}} * R_{\text{hea-DIODE1}}) + 0.6 \quad (3)$$

Where $R_{\text{th-IGBT1}}$ and $R_{\text{th-DIODE1}}$ represents the thermal resistance of the IGBT1 and the DIODE1 respectively ($R_{\text{th-IGBT1}}$ and $R_{\text{th-DIODE1}}$: in K/W). P_{DIODE1} dissipated power in the DIODE1 (W).

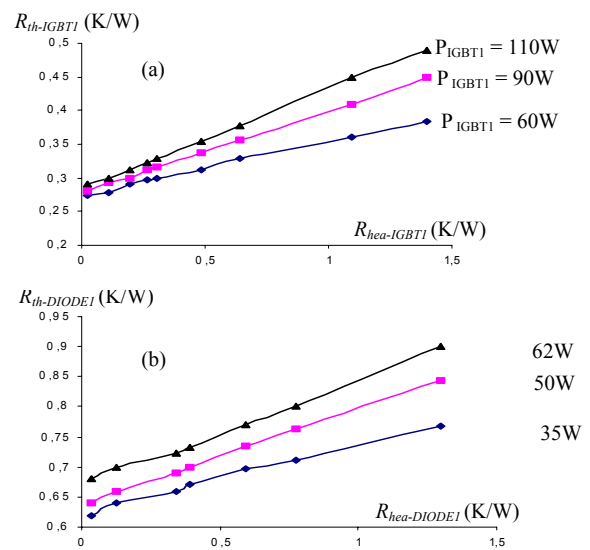


Fig. 5. Junction to case thermal resistance evolution, according to the component dissipated powers and the case boundary conditions, obtained by 3D numerical simulations ((a): for IGBT, (b): for DIODE).

3. THERMAL MODELING OF THE POWER HYBRID MODULE

3.1. State of the art

Because most of the semiconductor device models are implemented in circuit simulators, thermal circuit networks are the practical models for electrothermal simulations. Literature proposes some approaches to construct thermal networks equivalent to a discretization of the heat equation. For example the finite difference method (FDM) and the finite element method (FEM) are proposed. In the case of vertical power devices, where the thickness L_S is small compared to other dimensions, it is commonly considered that heat is generated at the top surface of silicon and flows uniformly along the x -axis (perpendicular to the silicon surface). So, the top surface

is considered to be a geometrical boundary of the device at $x = 0$, where the input power $P_0(t)$ is assumed to be uniformly dissipated. In our case we have chosen the (FEM) technique to develop the thermal model of the hybrid structure. Each material is represented by a simplified 1D thermal model. For the isolation and baseplate layer a modification have been introduced on the 1D model to take into account the thermal mutual between the different components.

The thermal model of the silicon material can be represented by the equivalent electrical circuit [8-9] shown in figure 6.

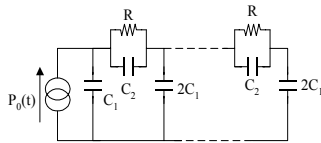


Fig. 6. The thermal model of the silicon material.

3.2. The superposition method

The physics of heat transfer is expressed by the general heat-conduction equation and governs the temperature distribution and the conduction heat flow in a solid having uniform physical properties. The Laplace transformation theory that can be used to solve this differential equation includes the superposition theorem, the Duhamel integral theorem, as part of its formalism. The idea of superposition is that known heat conduction solutions for specific heat transfer problems can be superimposed to yield a valid solution for more complex problems of interest. This principle of linear superposition of heat conduction solutions is an extremely powerful tool which is infrequently applied to thermal testing [10-11]. As a simple example of linear superposition, consider the case of a linear conductor bar with internal heat sources, insulated every where except at the ends where a fixed temperature is imposed. The temperature distribution within this linear conductor is shown in figure 7.a (top) where only a single heat source operates. With a different heat source operating, a second solution can be easily be generated as shown in figure 7.b (middle). Using the method of linear superposition, the solution for the bar with the two heat sources operating simultaneously can be created by simply adding the temperature fields and the heat fluxes. The significant capability offered by this method is that single heat source thermal solutions which are relatively simple to generate, can be superimposed to generate solutions for more complex problems which are relatively difficult to solve with by the direct approach. The method of linear superposition can easily be applied to thermal resistance characterization and measurement of components with multiple, independent heat sources where the heat transfer is dominated by solid conduction. Consider the case of the linear bar conduction shown in figure 7. Physically,

this example represents a bar with internally embedded heat sources. The sides of the bar are insulated such that heat can only escape the bar from the uninsulated end faces which are both exposed to an infinite heat sink of temperature T_0 . The reference temperature for this simple example is the infinite heat sink temperature, i.e., $T_{ref} = T_0$. Superimposing figures 7.a and 7.b, the temperature of point 1 equals the temperature rise of point 1 with the heat source at point 1 operating alone plus the temperature rise of point 1 with the heat source at point 2 operating alone. This is expressed:

$$T_1 = (T_{11} - T_0) + (T_{12} - T_0) + T_0$$

$$T_2 = (T_{21} - T_0) + (T_{22} - T_0) + T_0$$

For example where the single-source temperature are defined:

T_{11} = temperature of point 1 with heating from point 1

And the superimposed temperatures are:

T_1 = temperature of point 1 due to heat from both point 1 & point 2

T_2 = temperature of point 2 due to heat from both point 1 & point 2.

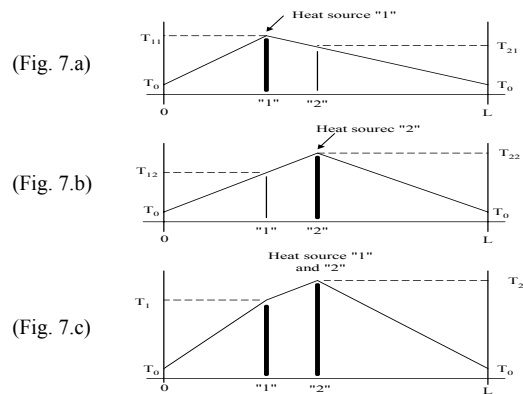


Fig. 7. Illustration of superposition concept.

3.3. The thermal model of the power hybrid module

Really, the heat transfer in the substrate and the case is not completely one-dimensional. Since silicon and copper thickness are considered very small comparing to the other material thickness, the heat spreading angle (α) is taken into account only for the isolation and the baseplate material in the simplified structure shown in figure 8. The angle (α) can takes any value from zero to 90° according to material parameters of the layer, dissipated power magnitude and boundary conditions in the case. This angle influences the values of the heat dispersion surfaces S_1 and S_2 and consequently the thermal resistances and the heat capacitances of the two layers. The model parameters of the element between two nodes k and $k+1$ will be calculated with an averaged surface (figure 9). The two surfaces $S_{I(k, k+1)}$ (for isolation layer) and $S_{B(k, k+1)}$ (for the case material) are given by the following expressions

$$S_{I(k,k+1)} = \pi \times \left[\sqrt{\frac{S_0}{\pi}} + \left(\frac{L_1(2k+1)}{2m} \right) \operatorname{tg}(\alpha) \right]^2 \quad 0 \leq k \leq m-1 \quad (4)$$

$$S_{B(k,k+1)} = \pi \times \left[\sqrt{\frac{S_0}{\pi}} + \left(L_1 + \frac{L_2(2k+1)}{2n} \right) \operatorname{tg}(\alpha) \right]^2 \quad 0 \leq k \leq n-1 \quad (5)$$

Where

m : number of nodes in the isolation layer and n : number of nodes in the baseplate. The averaged value of the used surface of the element between the node k and $k+1$ in the isolation layer of example is given by

$$S_{I(k,k+1)} = \frac{S_{I_k} + S_{I(k+1)}}{2} \quad (6)$$

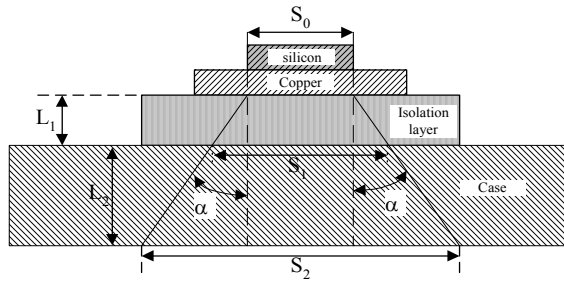


Fig. 8. Heat spreading angle (α).

In figure 10 we have shown the effect of the diffusion angle α on the effective thermal resistance of each device. From the characteristic of figure 10, the thermal resistance can be approximated by the following simple polynomial function as follows

$$R_{\text{th-IGBT}} = -15.7 \cdot 10^{-2} \cdot \alpha + 36.4 \cdot 10^{-2} \quad (7)$$

$$R_{\text{th-DIODE}} = 21 \cdot 10^{-2} \cdot \alpha^2 - 80 \cdot 10^{-2} \cdot \alpha + 1.1 \quad (8)$$

Using (2), (3), (7) and (8), the expression of the diffusion angle α for the IGBT1 according to the dissipated power and the boundary conditions on the case is given by

$$\alpha = \frac{-1.3 \cdot 10^{-3} P_{\text{IGBT1}} \cdot R_{\text{hea-IGBT1}} - 9 \cdot 10^{-2}}{15.6 \cdot 10^{-2}} \quad (9)$$

$$\text{For the DIODE1 } \alpha = \frac{80 \cdot 10^{-2} - \sqrt{\Delta}}{42 \cdot 10^{-2}} \quad (10)$$

$$\text{Where: } \sqrt{\Delta} = 0.64 - 2.67 \cdot 10^{-3} \cdot P_{\text{DIODE1}} \cdot R_{\text{rad-DIODE1}} + 0.4 \quad (11)$$

Using (4), (5) and (9), equations the surfaces $S_{I(k,k+1)}$ and $S_{B(k,k+1)}$ expression, for the IGBT1, are given by.

$$S_{I(k,k+1)} = \pi \left[\sqrt{\frac{S_0}{\pi}} + \left(\frac{L_1(2k+1)}{2m} \right) \operatorname{tg} \left(-\frac{1.3 \cdot 10^{-3} P_{\text{IGBT1}} \cdot R_{\text{rad-IGBT1}} - 9 \cdot 10^{-2}}{15.6 \cdot 10^{-2}} \right) \right]^2 \quad (12)$$

$$S_{B(k,k+1)} = \pi \left[\sqrt{\frac{S_0}{\pi}} + \left(L_1 + \left(\frac{L_2(2k+1)}{2n} \right) \right) \operatorname{tg} \left(-\frac{1.3 \cdot 10^{-3} P_{\text{IGBT1}} \cdot R_{\text{rad-IGBT1}} - 9 \cdot 10^{-2}}{15.6 \cdot 10^{-2}} \right) \right]^2 \quad (13)$$

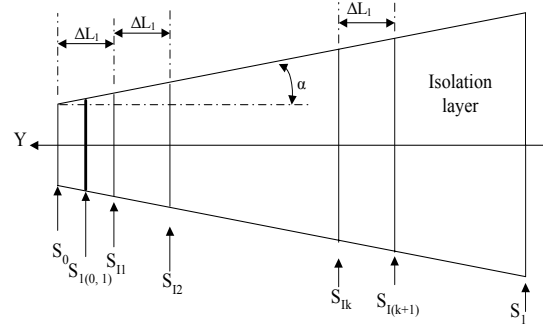


Fig. 9. Discretization of the isolation layer.

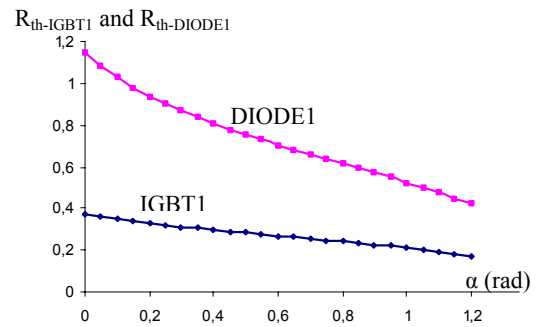


Fig. 10. Variation of the thermal resistance according to the angle α .

The superposition technique is used to develop the simplified thermal model of the hybrid structure. The method simply requires that for each independent heat source present, one test must be performed. During each test, junction temperatures for all devices must be measured. Figure 11 pictures the circuit networks corresponding to the IGBT1 thermal model used to estimate the thermal behavior of the IGBT1 in the module. For the isolation layer characterized by the parameters K_I , ρCV_I , L_I , S_0 and S_I , the thermal networks components between the note k and $k+1$ are given by

$$C_{2I(k,k+1)} = -\frac{\rho CV_I S_{I(k,k+1)} L_I}{6(m-1)}; R_{I(k,k+1)} = \frac{L_I}{K_I S_{I(k,k+1)}(m-1)}$$

The capacitance expression at the note (k) is given by

$$C_{1I(k)} = -\frac{\rho CV_I S_{I(k)} L_I}{2(m-1)}$$

The used IGBT1 thermal model order is equal to 12 (3 for silicon, 3 for copper, 3 for isolation and 3 for baseplate). In order to introduce the effect of the thermal mutual between the different components, current sources P_{inf1} , P_{inf2} and P_{inf3} are considered. These sources are deduced from the temperature increase on the IGBT1 due to the heat induced by all the other devices.

The source P_{inf3} is introduced at the interface between the silicon and the copper materials because the IGBT1 and

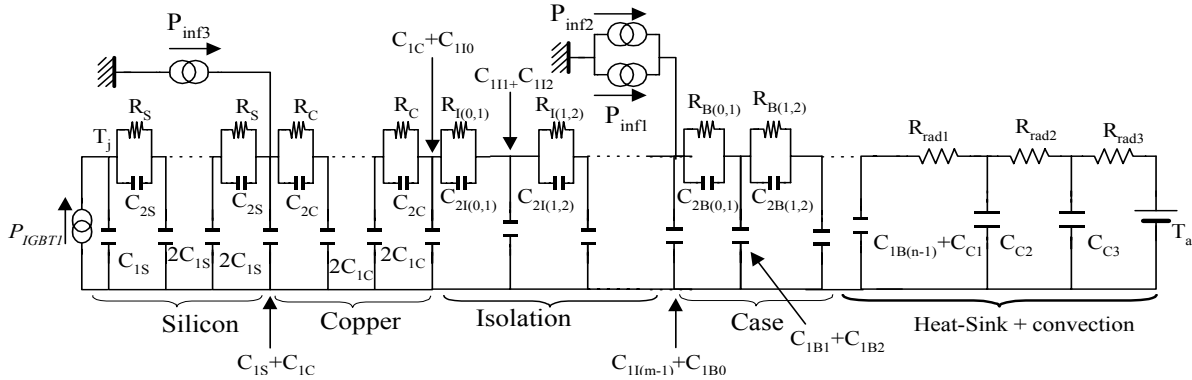


Fig. 11. The proposed thermal model of the module.

the DIODE1 (IGBT2 and DIODE2) ships are bounded on the some copper area in the case of the studied module. All module components have only the baseplate as a common material. When the studied module operates in a chopper condition, only two devices (an IGBT and a Diode) dissipate power. Applying the superposition method, the dissipated power (P_{inf1}) is given by $P_{inf1} = \frac{\Delta T_{DIODE2 \text{ on } IGBT1}}{R_1}$ (14)

Where $R_1 = \sum_{k=0}^{n-1} R_{B(k,k+1)} + (R_{rad1} + R_{rad2} + R_{rad3})$ (15)

When the studied module operates in an inverter condition, two IGBT and two Diode's dissipate power. Three powers will be dissipated. The dissipated power (P_{inf2}) is given by $P_{inf2} = \frac{\Delta T_{IGBT2 \text{ on } IGBT1}}{R_1}$ (16)

The dissipated power (P_{inf3}) is given by $P_{inf3} = \frac{\Delta T_{DIODE1 \text{ on } IGBT1}}{R_2}$ (17)

Where $R_2 = \sum_{k=0}^{n-1} R_{B(k,k+1)} + \sum_{k=0}^{m-1} R_{I(k,k+1)} + z * R_c + (R_{rad1} + R_{rad2} + R_{rad3})$ (18)

z : is the number of elements in the copper material.

3.4. Results and discussion

The thermal model of the different components are implemented in the MATLAB simulator [12]. In order to estimate the junction temperature of the IGBT's and the DIODE's. Figure 12 shows the evolution of the maximal junction temperature in the IGBT as a function of the boundary conditions in the case for different dissipated powers magnitude. These results are obtained by 1D thermal model and by 3D numerical simulations in the stated state conditions. A good agreement between the two types of evolutions is observed. We notice that the takes into account of the thermal mutual phenomena allowed a junction temperature correction. The temperature correction value can be more graters if the magnitude of the dissipated power increases and if the number of the active devices in

the module increases (module operates in an inverter condition).

$R_{equ-heat-sink}$ is the heat sink resistance corresponding to the equivalent thermal resistance between the module case and the ambient air (= 306K). The temperature at the interface between the module baseplate and the heat-sink is considered homogenous in the proposed 1D model. These assumptions have been verified by 3D numerical simulations.

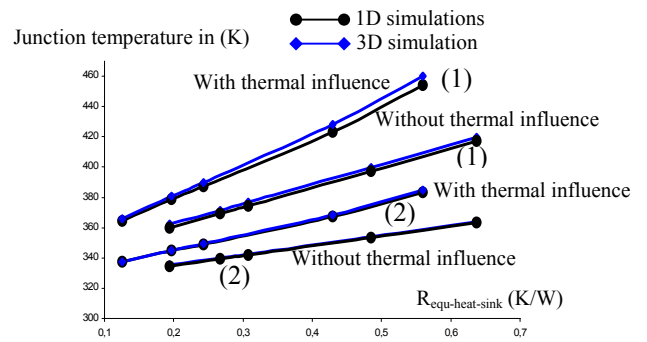


Fig. 12.a

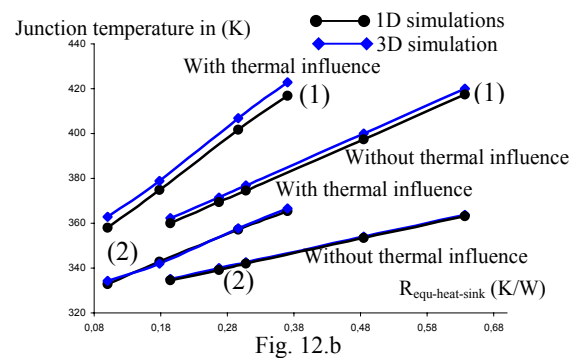


Fig. 12.b

Fig. 12. Evolution of the maximal junction temperature in the IGBT as a function of the boundary conditions at the module case. (Fig. 10.a: The module operates in a chopper condition; Fig. 10.b: The module operates in an inverter condition). ((1): $P_{IGBT} = 110W$ and $P_{DIODE} = 62W$; (2): $P_{IGBT} = 60W$ and $P_{DIODE} = 35W$).

Figure 13 and figure 14 shows the transient temperature evolutions at the junction and at the module case, when the module operates in a chopper condition. A good agreement between the results obtained by 1D thermal model and by 3D numerical simulations is observed. We notice that the simulation cost of the proposed 1D model is very small ($1/10^4$) compared to the simulation cost of the 3D numerical simulations. This can reduce considerably simulation time of a complete electrothermal analysis of the module.

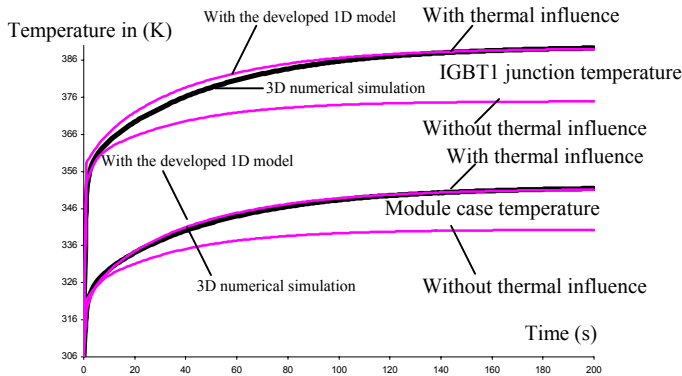


Fig. 13. Evolution of the junction temperature and the module case temperature (in IGBT1) ($P_{IGBT1} = 110W$; $P_{DIODE2} = 62W$; $R_{equ-heat-sink} = 0,25K/W$).

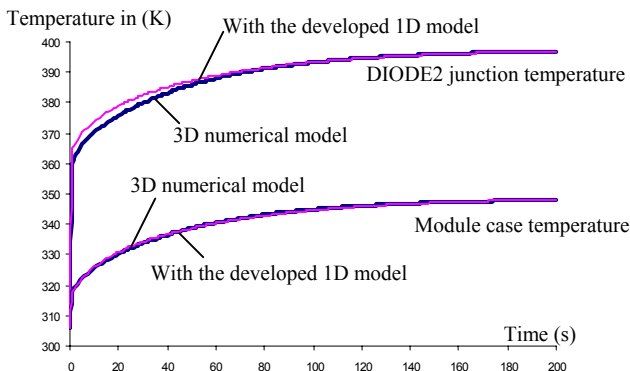


Fig. 14. Evolution of the junction temperature and the module case temperature (in DIODE2) ($P_{IGBT1} = 110W$; $P_{DIODE2} = 62W$; $R_{equ-heat-sink} = 0,25K/W$).

4. CONCLUSION

Thermal investigation in a hybrid structure have been done. In this type of structure lateral flour of the heat is important and thermal influences between the different components is not negligible. This thermal interaction depends mainly on the components dissipated power and the boundary condition at the heat spreader. An experimental technique have been developed to measure junction temperature increase due to the thermal mutual.

A simplified 1D thermal model have been developed. This model takes into account the thermal mutual between the different module chips based on the technique of superposition. The proposed model is compatible with circuit simulators. This model is obtained by the finite element method. The obtained those are in good agreement with these obtained with the 3D numerical simulations with the proposed model the electrothermal analysis of the multi-chip structure becomes more easy to implement especially in the case of circuit simulations.

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