DIFFERENTIAL TEMPERATURE SENSORS IN 0.35μm CMOS TECHNOLOGY

E. Aldrete-Vidrio, D. Mateo, J. Altet

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Eduardo Aldrete-Vidrio, Diego Mateo, and Josep Altet

Electronic Engineering Department, Universitat Politècnica de Catalunya, Barcelona, Spain
{aldrete, mateo, pepaltet}@eel.upc.edu

ABSTRACT

Measurements of the thermal profile evolution obtained by built-in temperature sensors at the surface of an IC can be used to test and characterize digital and analog circuits, being a potential alternative when these circuits are embedded (e.g., in a SoC) and they present a critical observability of their electrical nodes. It has been proved elsewhere [3] that a differential sensing strategy is suitable for such temperature measurements. In this paper, two different differential temperature sensors, active and passive, designed and fabricated in a 0.35µm standard CMOS technology are presented and characterized. Active sensors are based on differential amplifiers using lateral parasitic bipolar transistors acting as transducer devices. Passive sensors are based on integrated thermopiles. Each consists of the series connection of 8 thermocouples (16 strips) but different materials: poly1-poly2 and poly1-P+ implant.

1. INTRODUCTION

Temperature at the surface of a silicon IC is a physical magnitude whose evolution depends on the activity of the circuits embedded in the semiconductor die. There is a direct relation between the power dissipated by devices and the IC surface thermal map. Therefore, as the power dissipated by each device depends on its specific working conditions (e.g., operating point, input values, topology figures of merit of circuits as gain and non-linearities, etc.), it is possible to perform the circuit test through temperature measurements. For instance, in [1,2] abnormal hot spots appearing on the silicon surface are related to changes in the topology of analog and digital circuits due to the presence of structural defects, and the temperature is being used as a test observable of ICs (thermal testing).

Temperature sensors can be used to track the power dissipated by devices placed in the silicon die. They precise a very selective sensitivity: they need high sensitivity to small changes in temperature provoked by a change of the power dissipated by the circuit under measure, but they require a very low sensitivity to changes in temperature provoked by external elements, such as ambient temperature. This is achieved with a differential sensing strategy [3]: differential sensors are sensitive to changes of the difference in temperature at two points of the silicon surface.

Besides built-in thermal testing presented in [2] and [3], some applications of build-in differential temperature sensors involve defect localization, and electrical characterization. For instance, in [4] the distance between monitoring point and the defect has been determined with amplitude thermal measurements. To obtain the exact location of the defect, three different monitoring points are needed. In an early work [5], the possibility to characterize the electrical performance of high frequency analogue blocks into a system on chip (SoC) by thermal measurements has been proposed.

Prior realizations of active differential temperature sensors can be found in [2], where two sensors manufactured in a 1.2µm BiCMOS technology are experimentally reported. Simulated analysis of active CMOS temperature sensors can be found in [6,7]. A passive differential temperature sensor based on thermopiles can be found in [8]. Thermocouples were made with poly-metal couples in a 0.6µm AMS bulk micromachining process. Embedded transducers fabricated whit silicon CMOS compatible technologies offer the possibility of providing low cost applications. Fabrication of such devices can avoid semiconductor foundries integrating new material layers and processes in their standard microelectronics flow, where the circuits to be tested and/or characterized are implemented.

The objective of this paper is to present two (active and passive) fully CMOS compatible differential sensing strategies fabricated in a 0.35µm CMOS process. Active sensors are based on differential amplifiers, using lateral parasitic bipolar transistors acting as transducer devices. To the best of our knowledge, this paper reports the first experimental data of pure active CMOS differential temperature sensors. Passive differential sensors are thermopile-based, made of poly1-poly2 (both n-type) and poly1-P+ implant thermocouples connected in series. Thermopile senses the temperature gradient in the substrate surface and generates an output voltage by Seebeck effect. Thus it is possible to characterize the Seebeck coefficient of couple materials used from the 0.35µm standard CMOS technology.

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The paper is organized as follows: section 2 summarizes the main figures of merit of active differential temperature sensors and presents the different topologies reported in this paper. Sections 3 and 4 report the measurements of the active differential temperature sensors. Section 5 deals with the thermopile-based temperature sensors. Finally, section 6 concludes the paper.

2. TOPOLOGIES AND FIGURES OF MERIT OF ACTIVE SENSORS

Figure 1 shows two different topologies of a differential temperature sensor. Depending on the nature of its output voltage, the sensor can be classified in: a) monopolar or b) differential. In Figure 1, the square represents the location of the temperature transducer devices, S_1 an S_2, i.e., the points of the IC layout where temperatures T_1 and T_2 are measured.

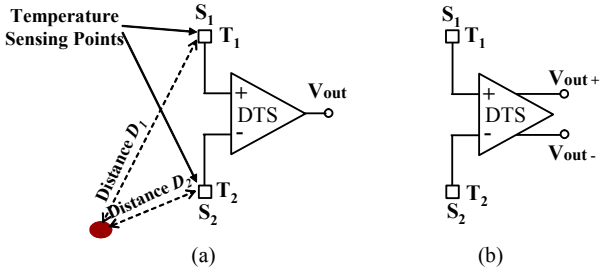


Figure 1: Symbol of two Differential Temperature Sensors (DTS): a) monopolar output, and b) differential output.

Ideally, the output voltage of the sensor circuit is only sensitive to the temperature difference (T_1-T_2). However, the output voltage of differential sensors can be shown to be:

$$\Delta V_{out} = S_{dT}(T_1 - T_2) + S_{cT}\frac{T_1 + T_2}{2} \qquad (1)$$

where S_{dT} is the sensor's differential sensitivity and S_{cT} is the sensor's common sensitivity. Ideally, the common sensitivity should be 0.

The experimental setup for the sensor sensitivity measurements is as follows. As indicated in Figure 1, a heat dissipating device is placed at a distance D_1 from S_1, and a distance D_2 from S_2.

The temperature difference generated at the temperature sensing points is provoked by the device power dissipation. Therefore, the sensor sensitivity can be expressed as a variation of the sensor output voltage versus the power dissipated by the heating device, its means [V/W]. In such a case, the distance between sensor transducers and heat dissipating devices is a very important data.

3. DIFFERENTIAL TEMPERATURE SENSOR WITH MONOPOLAR OUTPUT

The schematic of the implemented differential thermal sensor circuit (DTSC) with monopolar output is shown in Figure 2.

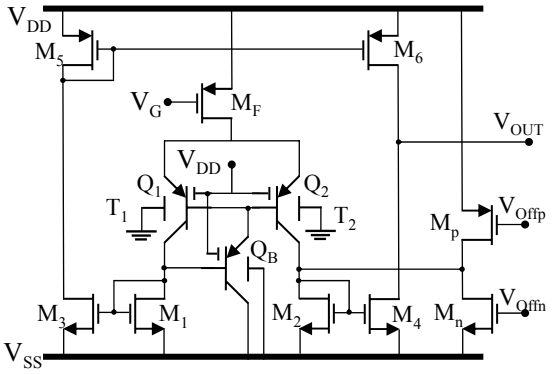


Figure 2: Schematic of the monopolar output differential temperature sensor.

It consists of a symmetrical CMOS transconductance amplifier (OTA) structure [9]. In this case, the temperature transducers devices (TTDs) are two lateral bipolar transistors Q_1 and Q_2 that are inherent in the existing CMOS digital technology, since they have the same temperature behaviour with respect to standard bipolar technologies [10,11]. Their operating temperatures are T_1 and T_2, respectively. The emitter area ($2x2\mu m^2$) of the CMOS-compatible lateral bipolar transistor is a fixed constant and predefined by the process technology. Two calibration transistors, M_p and M_n, acting as current sources have been added. They are capable of compensating by externally adjusting the DC operating point for both random and systematic thermal offset, and the possible mismatching between transistors. The biasing and output circuitry is setting by the other transistors in the circuit.

The operation principle and analysis of the DTSC is the same as that proposed in [3]: when no change in temperature is present between transistors Q_1 and Q_2, half of the current level determined by transistor M_F, flows trough Q_1 and M_1, with the other half flowing through Q_2 and M_2. Therefore, the output voltage variation, ΔV_{out}, is zero. A differential of temperature between Q_1 and Q_2 will cause currents imbalance in the input branches. The output stage converts this currents imbalance into output voltage. As a result, an output voltage variation with a significant gain is produced.

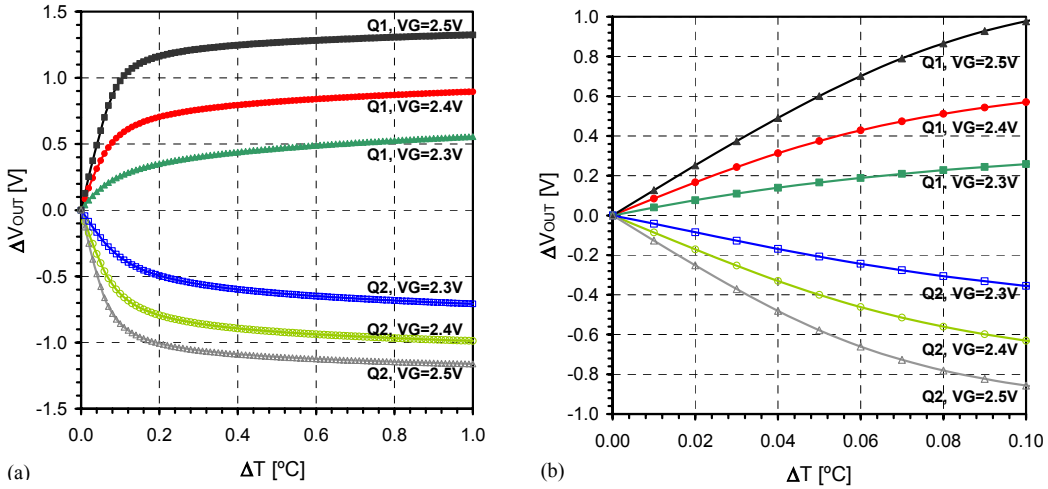


Figure 3: Output voltage variation ΔV_{out} as a function of temperature increase in Q_1 (Q_2) while Q_2 (Q_1) remains at nominal temperature (27°C).

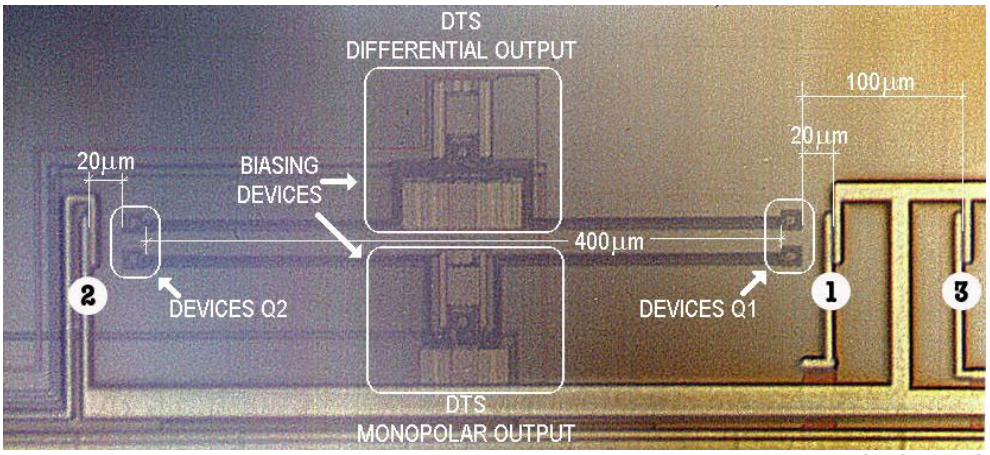


Figure 4: Photograph of built-in temperature sensors and 3 of the 4 heat sources (①, ② and ③).

Figure 3.a shows HSPICE simulated results of the static output voltage variation when the temperature of transistor Q_1 is increased by 1ºC with respect to the nominal temperature (27ºC), while Q_2 remains at room temperature, and vice versa. Different values of biasing voltage V_G have been analyzed. Figure 3.b shows a zoom-in over the temperature range before the output voltage saturates. If the nominal parameters of the devices are used throughout the analysis a voltage sensitivity of approximately -8 V/ºC can be reached when V_G = 2.4V, corresponding to a common mode gain of 1.88 mV/ºC (V_{DD} = 3.3V, V_{SS} = 0V, $I_{MF} \cong$ 3µA).

The DTSC and four identical heat sources (HSs) consisting of a MOS transistor connected in diode configuration have been fabricated in a 0.35µm CMOS standard process technology from AMS. Figure 4 shows a photograph of the sensor and heat sources. The layout was done such that the TTDs are placed at a relative large distance from each other, e.g. 400µm. Three of the heat sources are located at 20µm, 100µm and 220µm from Q_1, or at 420µm, 500µm, and 620µm from Q_2 (right side of Figure 4) and the fourth one is located at 20µm from Q_2, or at 420µm from Q_1 (left side of Figure 4).

DC power dissipated by each hest source as a function of its bias voltage can be externally set up. Their power dissipation range goes from 0 to 11mW. Once an individual heat source is activated, the temperature at the silicon surface around the device increases; this temperature increase is measured by the DTSC. Figure 5 shows the measured values of the static output voltage variation of the sensor as a function of the power dissipated by each activated heat source. Curves A have been obtained when only the heat source located at 20µm from Q_1 is activated. When only the heat source located at the same distance from Q_2 is activated, Curves B can be generated. Once the thermal steady state is reached, the output voltage measurement is taken. Table I summarizes the voltage/power [V/W] gain for different values of the bias voltage V_G.

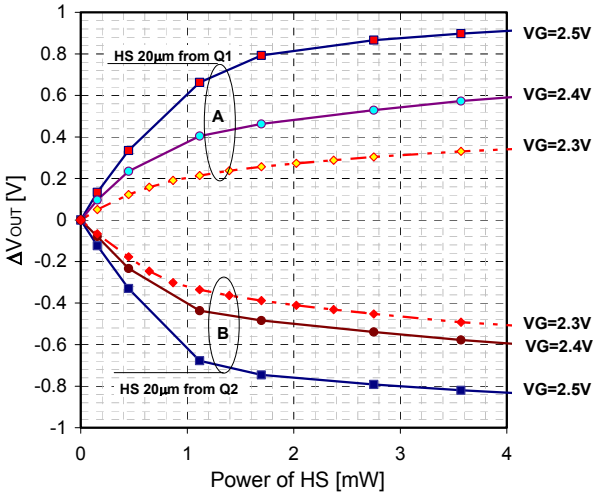


Figure 5: Measurements of ΔV_{out} vs. power dissipated by heat sources located at 20µm from Q_1 and Q_2, respectively. V_G = 2.3V, 2.4V and 2.5V.

TABLE I: Voltage/Power gain for different V_G bias voltages and active HS located at 20 µm from each TTDs.

V_G [V]	Q_1 [V/W]	Q_2 [V/W]
2.3	**237.3**	**-366.8**
2.4	**533.5**	**-518.5**
2.5	**618.5**	**-627.5**

In Figure 6, the voltage/power gains for different distances between the active heat source and Q_1 for V_G = 2.5V are plotted. The heat source located at 100µm produces a gain of 210 V/W in the sensor, whereas the most distant heat source produces a gain of 105 V/W. This fact illustrates the high sensitivity of this sensor to detect an active heat source in the same silicon substrate.

In Figure 7, the two equidistant heat sources (at 20µm) from Q_1 and Q_2 have been simultaneously activated. The voltage/power gains as a function of the bias voltage V_G are plotted. The measurements show that a lower biasing (means lower current and therefore higher output impedance of transistor current source M_F) cause a lower common sensitivity.

Figure 8 shows comparisons between measured and simulated values of the total bias current and the output voltage as a function of V_G. Good agreement between the simulated and measured bias current values has been showed. However, this is not the case for the output voltage where there is a major difference between values, which indicates the present of a thermal offset as a result of the distance between both TTDs in the sensor circuit (mismatching).

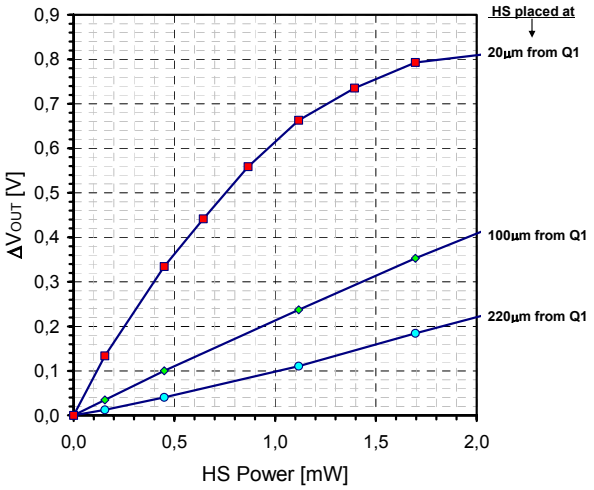


Figure 6: Voltage/Power gain plot for different distances between the active heat source and Q_1. V_G = 2.5V.

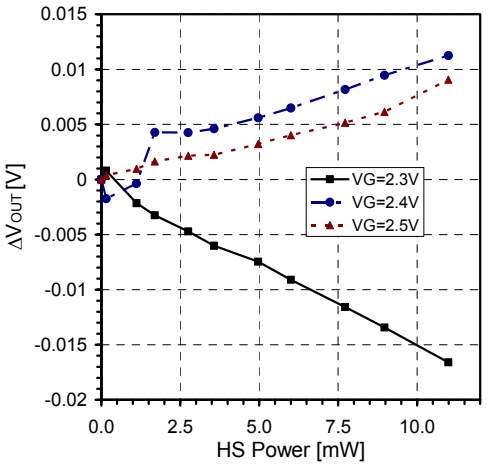


Figure 7: Output voltage as a function of the power dissipated at the same time by the equidistant HS's from Q_1 and $Q2$ as a function of the bias voltage V_G.

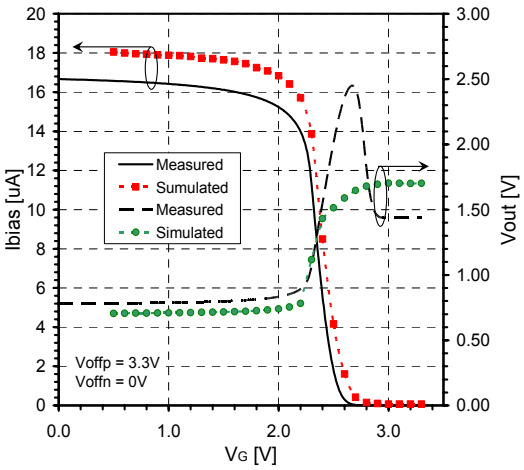


Figure 8: Total bias current and output voltage as a unction of the bias voltage V_G.

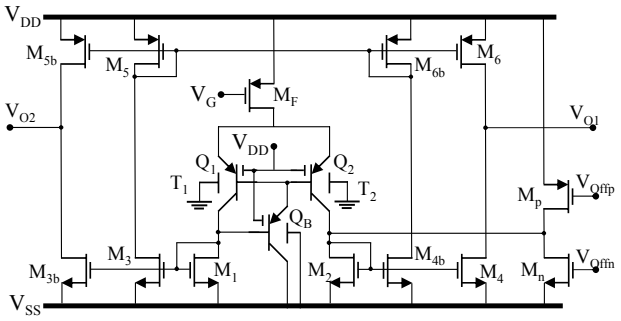


Figure 9: Schematic of the built-in fully DTS.

4. FULLY DIFFERENTIAL TEMPERATURE SENSOR

The first active fully differential temperature sensor (F-DTS) circuit to be reported in a fully CMOS technology is presented in this section. Figure 9 shows the schematic of the F-DTS. Operating principles are the same as the previous sensor. The F-DTS is based on a fully symmetric fully balanced OTA proposed in [12]. It can be described as a conventional three-current-mirrors single-ended OTA (see Figure 2), plus the additional branches formed by transistors M3b, M4b, M5b, and M6b. Thus, the OTA becomes fully differential, which has an improved dynamic range over its monopolar-ended counterpart. This is due to the properties of any differential structure, namely, better common-mode noise rejection, better distortion performance, an increased output voltage swing.

Figure 9.a shows the HSPICE simulation, where the differential output voltage variation as the temperature of sensing devices is increased by 1ºC is plotted. Figure 9.b shows the voltage sensitivity of the F-DTS compared with its monopolar-ended counterpart. It can be seen that the F-DTS has almost the same sensitivity of the DTS (≈ 8 V/ºC). However the F-DTS presents a larger linear region at the same operation conditions: V_{DD} = 3.3V, V_{SS} = 0V, $I_{MF} \cong$ 3µA and V_G = 2.4V.

The F-DTS has been fabricated using the same technology and following the same DTS circuit criteria. The set of heat sources is shared (see Figure. 4).

Figure 10 shows measured static differential output voltage variation of the F-DTS as a function of the power dissipated by each heat source individually activated: at 20µm, 100µm and 220µm from Q_1, or at 420µm, 500µm, and 620µm from Q_2, and one located at 20µm from Q_2, or at 420µm from Q_1 (see Figure 4). The voltage/power gains are given in Table II. The reduction in voltage/power gain is due to the operating point which cannot be correctly adjusted, since the calibration transistors (M_p and M_n) have been only added in one branch of the differential pair, and due to the loading effect.

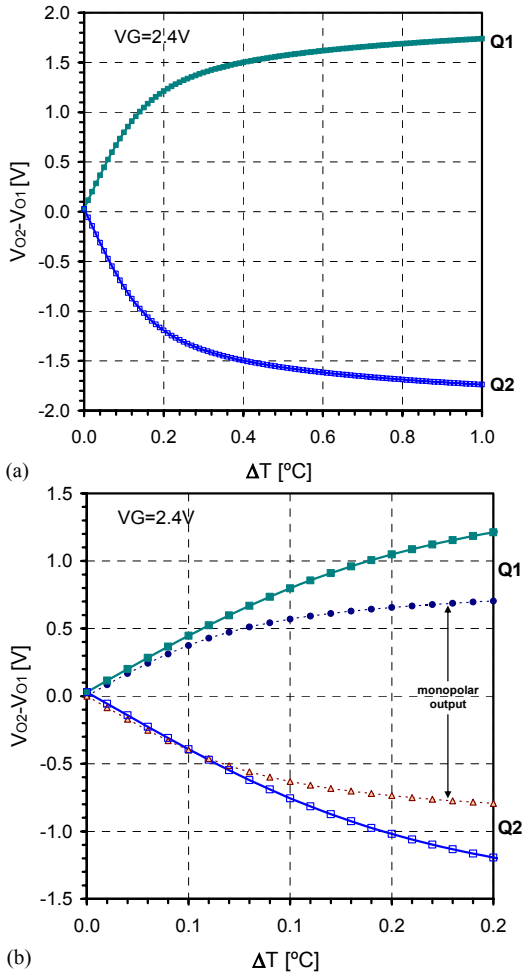


Figure 9: Differential output voltage as a function of temperature increase in Q_1 (Q_2) while Q_2 (Q_1) remains at nominal temperature (27ºC). V_G = 2.4V.

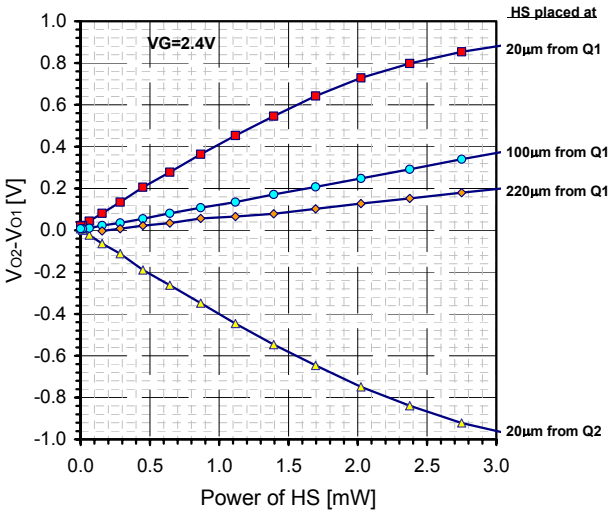
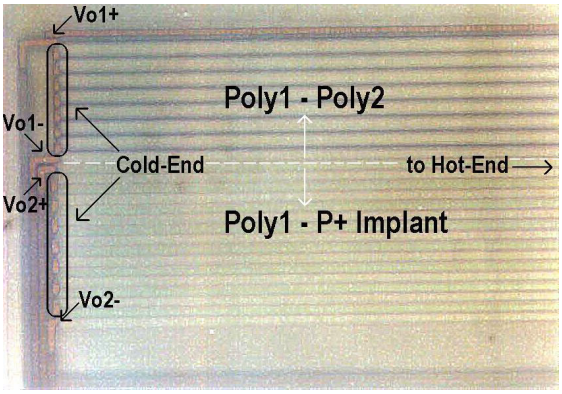


Figure 10: Measurements of the differential output voltage variation vs. power dissipated by the HS located at 20µm. from TTD Q_1 and Q_2. V_G = 2.4V.



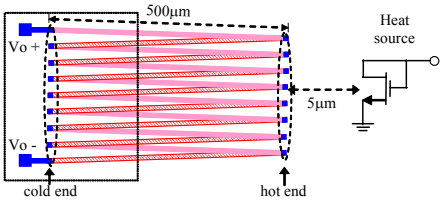


Figure 11: Photograph of the two implemented thermopiles (left) and Schematic diagram of a Thermopile (right).

TABLE II: Voltage/Power gain for V_G = 2.4V. HS located at 20 µm, 100 µm, and 220 µm from TTDs.

HS Distance [µm]	Q_1 [V/W]	Q_2 [V/W]
20	**383.3**	**-398.2**
100	**123**	
220	**62.7**	

The non-symmetry between the gains when the heat sources located to the same distance of Q_1 and Q_2 are activated is due to the sensor asymmetry: introduced by auto polarization scheme (transistor Q_B) and the compensation circuit.

5. THERMOPILES

The thermopile is a temperature sensor based on Seebeck effect. This effect results in the generation of a voltage between the ends of two joint materials (thermocouples) that have different Seebeck coefficients and are placed on a temperature gradient (see Figure 11). In order to be able to characterize the Seebeck coefficients of the 0.35µm CMOS technology, two thermopiles have been implemented and measured. Both thermopiles have the same structure but different materials.

The first one is made of a total of 16 stripes, 8 of Poly1 (n doped) and 8 of Poly2 (n doped), connected alternatively (8 thermocouples serially connected. See Figure 10, where the left part of both thermocouples is shown; the connections of the cold end are visible at the left of the photograph). The second thermocouple is made of 8 stripes of Poly1 and 8 of stripes of P+ implantation. All stripes are 500µm long (which is the distance between the hot and cold ends), and their width is the minimum allowed by the technology in each case (that is 0.65µm for Poly layers and 0.3µm for p+ implantation).

The temperature gradient is generated by a MOS transistor sized W/L = 20µm/0.35µm, connected in diode configuration and placed in what we call hot end of the thermopiles, which can dissipate up to 48 mW. From the plots shown in Figure 12 and 13, it can be observed that the sensitivity of the Poly1-Poly2 thermopile is 0.1 V/W, whereas it is 0.26 V/W of the Poly1-P+ one.

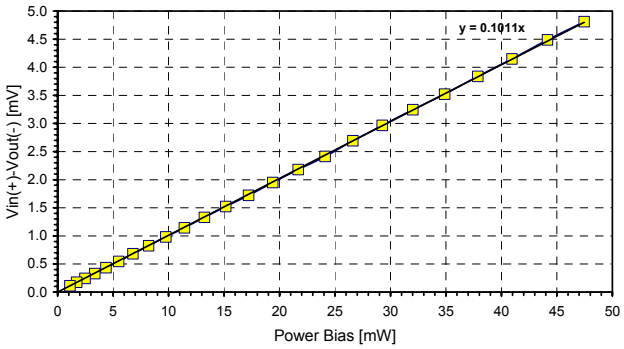


Figure 12: Output voltage of thermocouple Poly1-Poly2 as a function of the power dissipated by the MOS transistor.

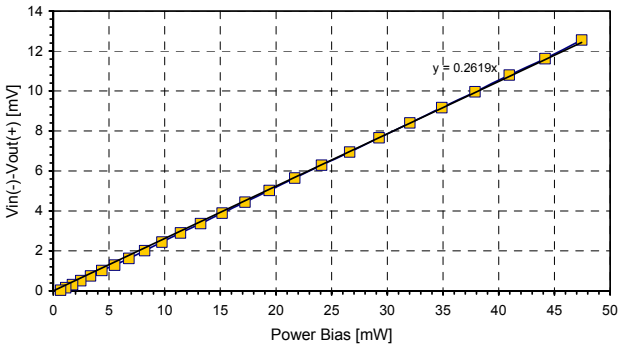


Figure 13: Output voltage of thermocouple Poly1-P+ as a function of the power dissipated by the MOS transistor.

6. CONCLUSIONS

In this paper we have presented two differential temperature sensing strategies manufactured in a 0.35µm CMOS technology. Two active temperature sensors use CMOS compatible lateral PNP bipolar transistors as

temperature transducers. The first one has a monopolar output, whereas the second one has a differential output. Static simulation and experimental results have been reported. Simulation analysis gives differential sensitivities of 8 V/ºC the monopolar and the differential sensors. When a heat source placed at 20 µm from one of the temperature transducers and 420 µm from the other, measurements have given differential sensitivities of 627.5 V/W and 398.2 V/W respectively, proving that CMOS differential temperature sensors can be used to track the power dissipated by devices placed in the same silicon substrate. In addition, sensitivities of two integrated thermopiles (passive differential sensors) made with standard CMOS materials have been reported. 0.1 V/W for Poly1-Poly2 and 0.26 V/W for Poly1-p+ materials.

ACKNOWLEDGEMENTS

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