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An Adaptive-Grain Thermal Simulation Method to Evaluate Effects of Spatio-Temporal Analysis Granularity upon The Thermal Behavior of VLSIs

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ABSTRACT

Recent advanced processors become more and more power-hungry and face adverse effects caused by the nonuniform thermal distribution generated by itself. The effects have not only an impact on the performance but also the logical and physical reliability. In the near future, circuit designers have to consider and estimate the effects during all design stages appropriately. In this paper, we propose an adaptive-grain thermal simulation on Very Large Scale Integrated Circuits(VLSIs), and by use of the proposal, we investigate and estimate the effects of changing analysis granularities on forming temperature profiles in digital circuits from the spatio-temporal viewpoint. Furthermore, from the simulations, focusing on the complication among some parameters; chip area, power, variation of power density distribution, etc., and the effects upon temperature profiles, we summarized the complication as a kind of curved surfaces. Consequently, we can say that the appropriate time resolution should be determined depending on required accuracy in terms of temperature, and tolerable computation cost.

1. INTRODUCTION

The power density of recent VLSIs increases rapidly as CMOS process technology evolution heads toward practical use of the nano-scale process technology. For example, at the present moment, the power density of high-performance microprocessors has already reached $50\text{W}/\text{cm}^2$ at the 100nm technology node, and it is said that next generation chips will soon reach $100\text{W}/\text{cm}^2$ at the technologies below 50nm[1]. As a result, the average temperature of the die also increases rapidly. Furthermore, local hot spots on the die usually have significantly higher power densities than the average, making the local temperatures much higher.

High temperature and hot spots have significant impacts on performance and reliability of VLSIs[2][3].

Accordingly, across the entire stages of a circuit design, circuit designers require detailed on-chip temperature profiles inevitably so as to accurately estimate temperature-dependent power, performance and reliability. Similarly, in order to precisely investigate effectiveness of Dynamic Thermal Management techniques(DTMs), it is essential that DTM designers hold spatio-temporal information about dynamic on-chip thermal behavior in more detail. For near future VLSI design, it is critical to find a way of properly addressing the temperature-related aspects of the design flow, and using temperature straightforward as a design policy in the entire design stages. Therefore, temperature-aware design has been becoming one of the major challenges in further updated design stages such as microprocessors, ASICs or System-on-a-Chip(SoC)[4][5].

In view of the current temperature-aware design and performance management, a lot of chip-architecture level thermal simulation methods have been proposed from the various points of view of spatio-temporal analysis granularity[6]-[9]. In general, as a design stage progresses, an extremely large amount of specific data can be obtained and available from the advanced design stage. It is very important for temperature-aware design methodology to be able to easily handle and apply the larger spatio-temporal data to more effective and accurate thermal simulation in compliance with the design stages. In order to realize it, it goes without saying that it is essential to have knowledge about the effects of various analysis granularities on thermal simulation, and find appropriate analysis granularity in advance. Unfortunately, all the methods mentioned above do not seem to be able to realize the effective and accurate thermal simulation throughout the temperature-aware design flow, because, to the best of our knowledge, no research has a discussion about the effects and accuracy of analysis granularity.

In this paper, for the purpose of addressing the problem, firstly, we define analysis granularity in view of thermal modeling and simulation. Then, we propose a simulation method which can deal with var-

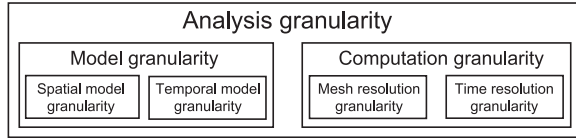


Figure 1: The constitution of the defined granularities.

ious analysis granularities. Finally, by use of the proposed method, we extensively investigate the effects on forming temperature profiles dependent on the analysis granularity and summarize the results comprehensively.

The rest of this paper is organized as follows. The next section describes a definition of analysis granularity and explains our proposed adaptive-grain thermal simulation method. Thermal modeling and numerical procedure exploited by the proposed are explicated in Section 3. Then Section 4 provides some simulation results of our specific simulation for several circuits and evaluates the results from the viewpoint of spatio-temporal granularity. Section 5 concludes the paper.

2. ANALYSIS GRANULARITY

As mentioned previously, we see that it is very important to estimate temperature at different granularities and at different design stages, especially early in the design flow. In this section, we define the keyword of analysis granularity in thermal simulations. When we simulate temperature behavior on a chip, we have to model the physical phenomena in order to reconstruct it on a computer, discretizing a continuous governing equation of the phenomena. We call the degree of target size “*analysis granularity*” along the series of the process. Chiefly the analysis granularity consists of two parts: *model granularity* and *computation granularity*. The model granularity means the minimum scale or size of a heat source we can deal with in an analysis. And, the computation granularity represents a kind of computational scale.

In our proposed approach, the concept of these two granularities is used as a kind of indicator which is a tradeoff between effectiveness and accuracy. Furthermore, each granularity is represented by two phases: spatial and temporal granularity. In summary, the model granularity is composed of spatial model granularity and temporal model granularity. Likewise the computation granularity consists of mesh resolution granularity and time resolution granularity. The relation among the granularities is shown in Fig.1 illustratively.

In the following subsections, model granularity and

computation granularity are explained in more detail respectively.

2.1. Definition of model and computation granularities

In the phenomena of heat conduction, the behavior is strongly affected by the strength and location of heat sources. Similarly, in thermal simulation, it is important to model heat sources appropriately in order to simulate the temperature behavior with accuracy. We classify model granularity into spatial and temporal model granularities from the spatio-temporal point of view.

In spatial model granularity, we assume that a logic gate, which is regarded as a cell in a standard cell design method, is the finest spatial model granularity as a basic heat source. We call the model granularity cell level. Also, the chip die is partitioned into functional blocks according to microarchitecture functionality and each functional block is considered as one heat source. In this case, the spatial model granularity is referred to as functional-block level. Considering a functional block is composed of a lot of cells, the functional-block level is coarser than the cell level. Likewise, we can assume sub-functional block level which has some number of cells arbitrarily. Accordingly, there can be some successive levels between the cell level and the functional-block level in spatial model granularity. In this paper, because we presume logic cells are basic heat sources, the relation of power between cell level and functional-block level is expressed as follows.

$$P_C = \sum_{i=1}^N P_{F_i} \quad (1)$$

where P_C is the power of a coarser heat source and P_{F_i} is that of a logic cell which is included in the coarser heat source. Fig.2 illustrates the relation and shows the definition of the model granularities. Similarly to the spatial model granularity, for the temporal model granularity we assume a basic time interval. Each logic cell generates heat/power depending on its type of logic and the switching activity. In fact, the power distribution is not only dependent on the cell connection topology but also the input vector at every clock cycle. Therefore, we regard one clock cycle interval as a basic time interval, which is the finest temporal model granularity in this paper. We can arbitrarily control the length of a coarser time window(TW_C) based on the basic TW_F (= 1 clock cycle). The power of a heat source in a coarser temporal granularity can be described in the following.

$$P_{avg} = \frac{\sum_{i=1}^M P_{cell_x} \times \alpha_i}{TW_C} \quad (2)$$

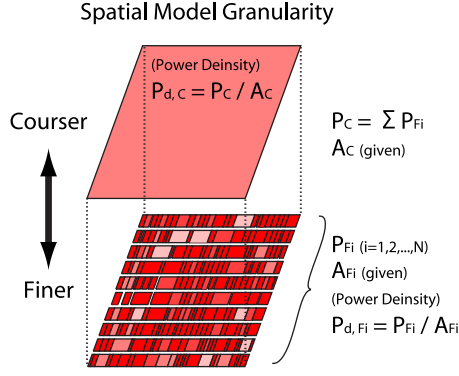


Figure 2: Illustration of the definition of spatial model adaptability.

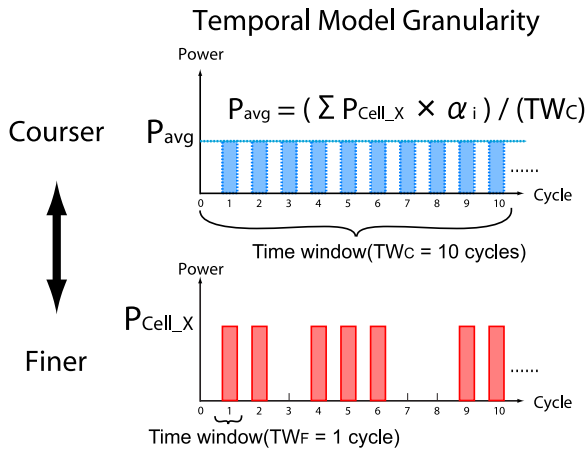


Figure 3: Illustration of the definition of temporal model adaptability.

where P_{avg} is the power of a coarser temporal heat source, P_{cell_x} is the power in a finer time window of $Cell_x$, M is the length of a coarser time window and α_i is the switching activity in i clock cycles. Fig.3 shows the relation visually.

Likewise, computation granularity has two components. One is mesh resolution as spatial granularity and the other is time interval as temporal granularity. These granularities are defined specifically in numerical computation conditions. In mesh resolution, every heat source that overlaps the area of a grid point serves as a power source feeding into that grid, and the grid point has the corresponding power value which is calculated based on the ratio of the heat source area to the total area of the heat source. For illustration of mesh resolution, we show three levels of mesh resolution in Fig.4.

In time interval resolution, a time interval represents the length of one time step of a numerical iter-

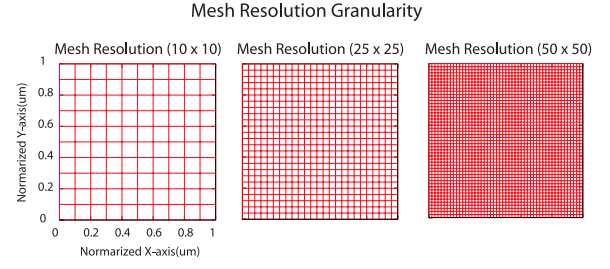


Figure 4: Mesh resolution granularity.

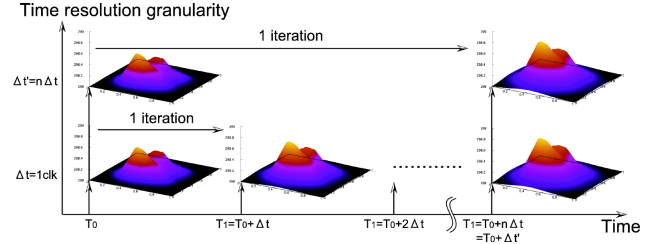


Figure 5: Time resolution granularity.

ation. Due to the correspondence of the total power between a coarser and a finer time window as shown in eq.(2), temporal model granularity have to be the same as the time interval resolution. Therefore, the temporal model granularity is inevitably affected by the time resolution(interval) resolution. Fig.5 shows the difference of time interval resolutions in numerical computation with using two different time intervals.

Note that changing these computation granularities directly affects forming temperature profiles in terms of computational truncation error.

3. ADAPTIVE-GRAIN THERMAL SIMULATION

In this paper, based on our previous work[9], we extend the functionality of the thermal simulation method in terms of spatio-temporal analysis granularity. The former simulator only focused on the cell level and clock-cycle level model granularity, which was referred to as “fine-grain” thermal simulation. The fine-grain thermal simulator requires two input data; cell level geometrical information and clock-cycle level switching information, which are obtained in temporal phase and spatial phase along a simulation flow respectively, as shown in Fig.6. In Fig.7, we illustratively show the relation between the fine-grain thermal simulator and two input data.

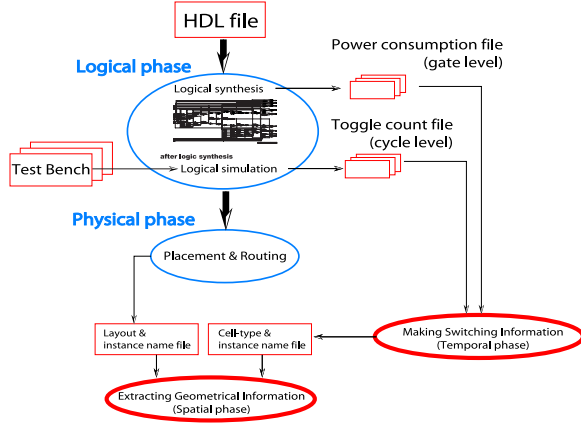


Figure 6: Simulation flow obtaining two main input data for the fine-grain thermal simulation.

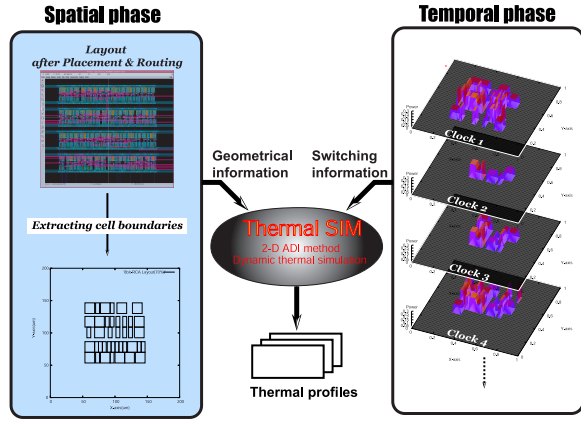


Figure 7: The relation between the fine-grain thermal simulator and the two input data.

Exploiting the cell level and clock-cycle level model information as the finest model granularity, we can deal with arbitrary model granularity. We call the extended simulation method “adaptive-grain” thermal simulation method. As a result, the extended thermal simulator has advantages of flexibly varying spatio-temporal analysis granularity. Specifically, the following sections provide the policy to realize the adaptability exploited by the proposed simulation.

3.1. Adaptability of model and computation granularities

The adaptability of heat source model with respect to model granularity is realized as follows; in spatial granularity, the heating value per unit area of a coarser heat source is to be the area-average of heating values of several finer heat sources covered with the coarser one; similarly, in temporal granularity,

a time window is defined. The time window means that a heat source generates uniform power during the given period. In a coarser-grain time window, the heating value per unit time of a heat source is regarded as the time-average of the sum of activating heating values of the heat source in finer-grain time window within the coarser-grain one.

Similarly to the model granularity adaptability, computation granularity has mesh and time resolution granularities. Both the mesh and time resolution granularity are explicitly determined by a numerical computation condition, i.e., the degree of spatial and temporal discretization.

The proposed adaptive characteristics are apparently very simple but enable us to realize high adaptability in different design stages. Due to the hierarchical characteristics which can model and comprehend complexity of specifying heat sources across design stages, accordingly, the proposed method has capability to freely change the granularities adaptively along design stages.

3.2. Thermal modeling

In order to estimate the impact of changing analysis granularity on forming temperature profiles, firstly, we focus on the finest analysis granularity, i.e., cell-level and clock cycle-level. Additionally, we assume that a target chip is as a thin plate almost composed of silicon base on the assumption that silicon is a relatively poor heat conductor and cannot spread heat efficiently compared with some other metal materials such as aluminum.

We simulate a chip using the following mixed 2-D/1-D strategies: (1) 2-D simulation is performed for the chip substrate, considering the fine granularity of the proposed method, and (2) packages and heat sinks are modeled as 1-D thermal resistances based on a well-known duality between heat transfer and electrical phenomena in order to reduce the computational complexity[2].

3.3. Numerical approaches

Focusing on our thermal model, the general 2-D heat conduction equation is transformed as follows:

$$\frac{\partial T(x, y, t)}{\partial t} = \kappa \left(\frac{\partial^2 T(x, y, t)}{\partial x^2} + \frac{\partial^2 T(x, y, t)}{\partial y^2} \right) + \frac{Q(x, y, t)}{\rho C_p} - \frac{h}{\rho C_p} (T(x, y, t) - T_{amb}) \quad (3)$$

where $T(x, y, t)$ is the time dependent temperature at any point, $\kappa = \frac{\lambda}{\rho C_p}$ is thermal diffusivity, ρ is the density of the material, C_p is the specific heat, λ is the thermal conductivity, $Q(x, y, t)$ is the heat energy generation rate, h is the constant derived from the effective heat transfer coefficient.

The equation is subjected to the following boundary conditions: the four sides and the top are set to be in the insulated condition (Neumann condition), i.e., $\frac{\partial T}{\partial x} = \frac{\partial T}{\partial y} = 0$, and the bottom is convective to room temperature with a heat transfer coefficient (Robin condition). The last term represents it, what we call Newton's law of cooling. Throughout our simulation, we assume ambient temperature is 298K (25°C).

We use the alternating-direction-implicit (ADI) method [2][10] to solve the differential equations. Basically, the ADI method is a process to reduce the 2- or 3-dimensional problems to a succession of 2 or 3 1-D problems. Then eq.(4) and the subjected boundary conditions discretized by the ADI method are effectively solved by an algorithm with linear time complexity.

4. EXPERIMENTAL RESULTS AND DISCUSSION

As mentioned above, to facilitate more practical temperature-aware design at each design stage and then make DTM techniques effective, it is significant for designers to have comprehensive knowledge about the effects of variation of analysis granularity on temperature profiles. Therefore, in the beginning, we investigate and evaluate the effects for some circuits with using our proposed thermal simulation method which has the ability to freely change spatio-temporal analysis granularity, and then try to find the appropriate spatio-temporal analysis granularity.

4.1. Simulation conditions

First, we need the switching and geometrical information to identify when and where heat sources are activated in the chip. In this simulation, we use standard cell design method for target chips. Therefore we can simply regard cells, which are provided as standard cells by CAD vendors, as logic gates. Then switching information is obtained in the phase of logical simulation, and geometrical information in the phase of placement & routing (P&R) respectively during implementing a target chip.

During the logical simulation, we make the toggle counting file for a given input vectors. The clock cycle-level switching information dependent on input vectors is derived from the difference between the files which depict the number of toggle counts on each cell by each clock cycle. The switching information file also has the power of each cell obtained by the CAD tool. After a placement and routing phase, we obtain the places and surface areas of heat sources.

We use two combinational logic circuits, an 8-bit ripple-carry adder (RCA) and an 8-bit carry look-ahead adder (CLA), and a 16-bit microprocessor

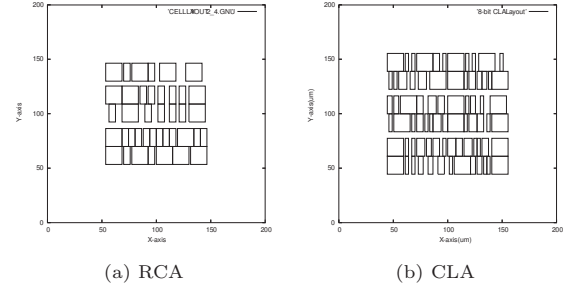


Figure 8: Layouts of an RCA and a CLA.

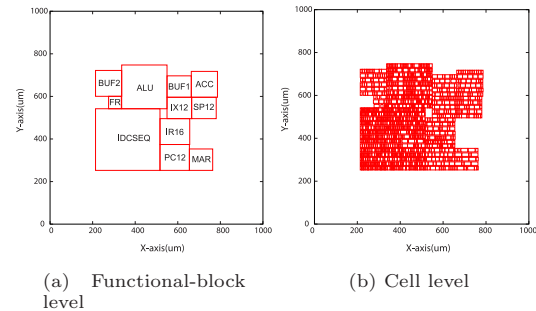


Figure 9: KITE layout.

KITE [11] [12] in order to make it clear that the proposed method has potentiality for investigating the impact of dynamical power distribution and cell-level layout changes from the spatio-temporal viewpoint.

The target circuits are written in VHDL. In the logic synthesis, using Design Compiler from Synopsys, Inc.,¹ we make their netlists together with the EXD's cell library subject to ROHM's 0.35μm CMOS technology, and then we obtain their circuit's layout information by using Milkyway and Apollo as a placement and routing tool.

Fig.8 shows the positions and area of every cell for two types of simple layouts: an RCA and a CLA. Fig.8(a) is an 8-bit RCA, and Fig.8(b) is an 8-bit CLA with the same area utilization percentage. Fig.9 presents a layout of 16-bit microprocessor KITE. In Fig.9(a) indicates the functional block level layout and cell level layout is shown in Fig.9(b).

We assume both of these circuits have the capability of operating at a frequency of 100MHz at a supply voltage of 3.3V and the simulation time interval Δt was one clock cycle time, or 10 nsec. Table 1 summarizes several properties of each target circuit. While 8-bit adders execute additions of 33000 random input vectors, KITE's execution program is the "Tower of Hanoi", which requires 33000 clock cycles to complete.

¹This work is supported by VLSI Design and Education Center (VDEC), The University of Tokyo with the collaboration with Synopsys Corporation."

Table 1: Properties of target circuits.

	Area(μm^2)	Power(mW)	# of Cells
RCA	93 x 93	1.06	40
CLA	111 x 111	1.67	76
KITE	573 x 495	1.08e3	1231

4.2. Comparison of thermal behaviors between the finest model granularity and the coarsest model granularity

In order to clearly demonstrate the influence of variation of model granularity, we compare temperature profiles simulated under different model granularities. On the one hand, we fixed the computation granularity. Here, the spatial computation granularity is 100×100 and the temporal one is 1 clock cycle time step. Specifically, each layout of 8-bit adders is included in the chip area or computational area of $200\mu\text{m} \times 200\mu\text{m}$, where the area is divided into a 100×100 square mesh and, therefore, has 10000 grid points in itself. In addition, KITE is in the chip area of $1000\mu\text{m} \times 1000\mu\text{m}$. Similarly, the area is meshed by 100×100 square grid.

We focus on the effect on the maximum temperature in terms of the difference between the cell level and clock cycle level, and the functional-block level and steady state model granularities. We call these model granularities “finest-grain” and “coarsest-grain” heat source model respectively. As a typical value, Table 2 shows each temperature difference between the two model granularities and errors due to coarser model granularity at 20000 clock cycles. Table 2 indicates that the error of KITE is more than twice as large as that of CLA, more than seven times larger than RCA. On the other hand, in 8-bit adders, the difference of maximum temperatures did not appear significantly because they had no remarkable difference between their power density maps made by different model granularities. This significant difference among these circuits suggests that the temperature difference induced by different model granularity was strongly affected by the chip area and the power density distribution.

In Fig.10, the transition of maximum temperature on the processor KITE is shown in terms of the finest-grain and the coarsest-grain heat source model. The upper curve $T(\text{cell}, \text{clk})$ was obtained with the finest model granularity and the lower curve $T(\text{fnc}, \text{std})$ were obtained with the coarsest model granularity. The difference between each max temperature was about 0.12°C and clearly observed as the effect of the spatial model granularity rather than temporal model granularity because $T(\text{cell}, \text{clk})$ showed little fluctuation caused by variation of power generation in the clock cycle level.

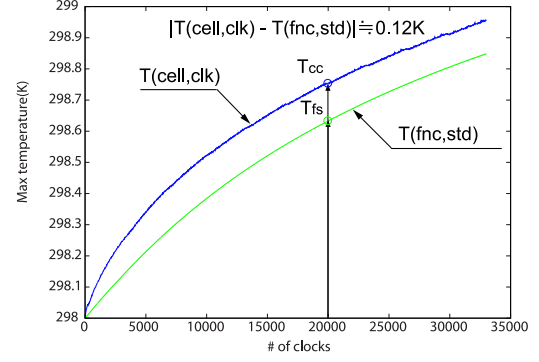


Figure 10: Comparison between max. temperatures of the finest- and coarsest-grain heat source models.

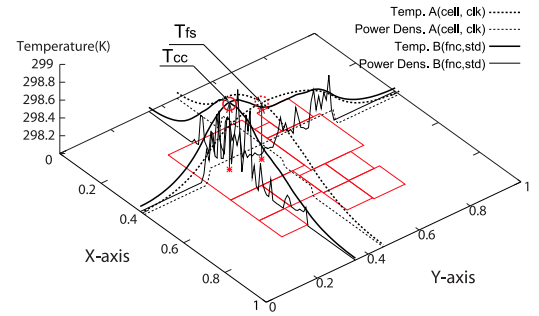


Figure 11: Comparison of temperature and power density distributions after 20000 clock cycles.

Furthermore, as shown in Fig.11, two maximum temperature points at 20000 clock cycles and each temperature and power density distribution along x- and y-axis are illustrated. These results present that the heat source with highest power density does not always make the maximum temperature point within itself, and the displacement is strongly affected by chip configuration and the power density distribution. From the following simulation, we focus on KITE since only KITE provides us with more diversified analysis granularities than the other target circuits.

4.3. Evaluation of complications between accuracy and cost-effectiveness

Evaluation here has two categories: accuracy, or error, and cost-effectiveness, or computational cost. In other words, “accuracy” indicates the degree of computational resolution, i.e., computation granularity. “effectiveness” indicates the degree of heat source modeling, i.e., model granularity.

In effectiveness evaluation, first, we inspect the effect induced by the variation of the spatio-temporal model granularity on temperature profiles, consider-

Table 2: Comparison of transition of max. temperature on each circuit.

	Temp. Diff.(K)	Error(%)
RCA	0.0185	0.00616
CLA	0.0678	0.0225
KITE	0.122	0.0465
@20000 clocks		

ing the change of maximum temperature. In this evaluation, cell level and clock-cycle level model granularity of a heat source model is regarded as the base line of the evaluation of effectiveness. Second, in accuracy evaluation, we estimate the effects of changing the degree of mesh/time resolution in numerical simulation on on-chip temperature profiles, revealing the sufficient mesh resolution to observe on-chip temperature behaviors.

4.3.1. Complications dependent on model granularity

In this simulation, we fixed computation granularity and considered that its mesh resolution was 100×100 and unit time interval was clock cycle level. On the contrary, in model granularity, we used our proposed simulator for KITE under the conditions of two types of spatial model granularity and six types of temporal one: cell and functional-block level in terms of the spatial granularity, and 1, 10, 100, 1000 and 10000 clock-cycle time window and time average (steady-state) in terms of the temporal one, respectively. As a the baseline of accuracy, the model granularity of cell level and 1 clock-cycle time window was chosen. We used relative error as the criterion to quantitatively compare the baseline model granularity with that of rough model granularity. The relative error is defined in terms of:

$$E_r = \frac{|T_{fine} - T_{coarse}|}{T_{fine}} \times 100(\%) \quad (4)$$

Also, we think of cost-effectiveness as the length of execution time. The simulator was implemented with C++ language and executed on a PC with a 3.4-GHz Pentium 4 processor and 3 GB of memory. The simulation results with respect to accuracy and cost-effectiveness were plotted in Fig.12. In addition, the evaluation was performed in three temperature profiles of 10000, 20000 and 30000 clock cycles, respectively.

As Fig.12 clearly shows, the finer temporal model granularity becomes, the better accuracy is obtained.

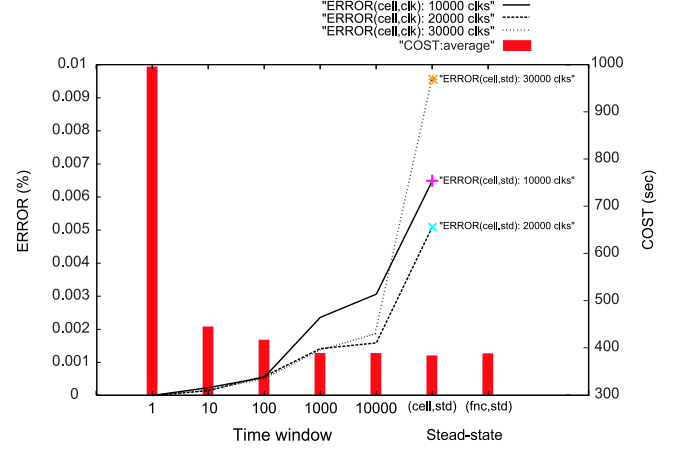


Figure 12: Complications dependent on model granularity.

Although the coarser temporal model granularity reduces computation cost, the increase of error would nullify the merit. The finest granularity provides high accuracy while the computation cost dramatically increased. These results suggest that there is an appropriate model granularity which offers reasonable accuracy and effectiveness at the same time. Note that the three error plots of functional-block level and time average were omitted since these values of error were around 0.07% and the value was much larger than others even the computation cost was about almost same.

4.3.2. Complications dependent on computation granularity

In contrast to the previous simulation, the model granularity were fixed at cell and clock cycle level, i.e., the finest granularity. On the other hand, in computation granularity, we executed our thermal simulation under the conditions of five types of spatial computation granularity and five types of temporal computation granularity: 10×10 , 25×25 , 50×50 , 100×100 and 200×200 mesh resolution, and 1, 10, 100, 1000 and 10000 clock cycle time interval. As a base line, the computation granularity had 200×200 mesh and 1 clock cycle time interval. Similarly to the previous error evaluation, here we used relative error. But, in this time, coarser grid mesh does not always have a corresponding grid point of finer grid mesh. Therefore, in coarser grid, all grid points corresponding to finer grid were obtained to be interpolated by use of linear Lagrangian interpolation scheme. Also, together with accuracy evaluation, we determined the execution time which indicates cost-effectiveness. As performed in the previous evaluation, based on three thermal profiles of 10000, 20000 and 30000 clock cy-

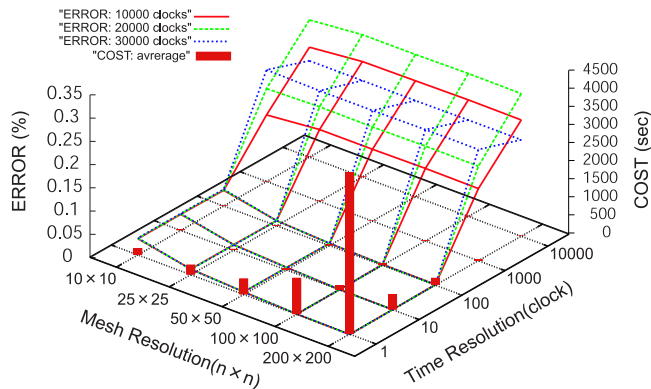


Figure 13: Complications dependent on computation granularity.

cles, we evaluated each profile. These results are shown in Fig.13, where we can see that over 100 clock cycle time interval the value of error suddenly rose. However, little change of error was along mesh axis in every time interval. The almost same phenomena happened to each temperature profile. On the one hand, the distribution of computation cost shows a similar relation to Fig.12 with regard to uprush of computation cost in finest computation granularity. These results suggest that time resolution has a much larger impact on error than mesh resolution although this phenomena might be strongly influenced by a dispersion of power density distribution and a chip area size.

5. CONCLUSIONS

In this paper, we have defined and classified analysis granularity, which should be considered in thermal simulation along circuit design stages. Then, considering our previously proposed fine-grain thermal simulator, we have presented the extended adaptive-grain thermal simulation method, which is able to handle not only the cell level and the cycle level granularity but also functional-block level and steady state granularity.

To have extensive knowledge about the effects of variation of analysis granularity in terms of accuracy and cost-effectiveness, we performed the proposed simulation for several target circuits and investigated the complication quantitatively. Consequently, the results suggest that the variation of analysis granularity strongly affects the error and the computation cost. Almost same tendency was observed through our simulation in view of model and computation granularity. In temporal analysis granularity, to some extent, time window or time resolution could be set

roughly, but over a threshold, error dramatically increases. Meanwhile, in view of spatial analysis granularity, the effects induced by the variation of spatial granularity could not be observed clearly. But, so far, we have investigated the complication under only a little number of target circuits. In the future, we will carry out our thermal simulation for several circuits in order to realize the effective and accurate thermal simulation method for temperature-aware design methodology.

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