RELIABILITY STUDY OF POWER RF LDMOS DEVICES UNDER THERMAL STRESS

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LEMI, University of Rouen, IUT Rouen, 76821, Mont Saint Aignan, France

ABSTRACT

This paper presents the results of comparative reliability study of two accelerated ageing tests for thermal stress applied on power RF LDMOS: Thermal Shock Tests (TST, air-air test) and Thermal Cycling Tests (TCT, air-air test) under various conditions (with and without DC bias, TST cold and hot, different extremes temperatures ΔT). The performances shift for some critical electrical parameters such as on-state resistance (R_{ds_on}) and feedback capacitance (C_{rs}) have been demonstrated under various tests. To better understand the parameter shift that appear after thermal stress, we used a physical simulation software (Silvaco-Atlas, 2D) to confirm qualitatively degradation phenomena.

1. INTRODUCTION

RF LDMOS is becoming increasingly important in communication sector, such as mobiles, portable computers and eventually base stations, which generated ongoing effort demand to improve performances. A device's lifetime is one of the criteria used to qualify a technology. The temperature is a critical parameter, particularly in RF power electronic devices. This element has a considerable influence on reliability and performances [1], can limit the lifetime of semiconductors and consequently plays an essential part in failure mechanisms [1,2]. For these reasons thermal shocks and cycling conditions are becoming important for RF LDMOS in many applications. It is well-known that if devices are repeatedly subjected to electrical and thermal overload over extended periods of time, shock and cycling phenomena may lead to device failure, leaving the load current unlimited and subsequently posing a serious risk of damage [3]. The objective of the presented work is a comparative reliability study of various thermal stress conditions, respecting to other studies in the literature. Our methodology consists in characterizing and modelling the device before and after ageing.

2. POWER RF LDMOS EXPERIMENTAL CHARACTERIZATION

It is essential to characterize power RF LDMOS in order to extract parameters before and after device stress. This step should allow us to correlate thermal stress to any parameter drift, or even to help identify a degradation phenomenon. A commercial Motorola RF LDMOS MRF21010LR has been used for this study. The main characteristics of this device are as follows: frequencies up to 2 GHz, output power of 10 Watts, breakdown voltage of 65V. I-V and C-V measurements were performed using the commercial software package IC-CAP.

The static mode (I-V) gives us an insight into the device behaviour in its various operating mode (linear, saturated…), and allows to quantify some important electrical parameters before and after device stress. These measurements were performed by an Agilent E5270 DC analyser with 20W power supply. These electrical parameters will be helpful in our reliability study to keep track of electric device degradation state. C-V profiles were performed using an HP 4194A impedance analyser to keep track capacitance states before and after stress.

3. THERMAL STRESS BENCH

In our experiments (figure 1), the devices are stressed with an applied high drain-source voltage (V_{ds}) of 40V and a gate-source voltage (V_{gs}) of a value to obtain a permanent drain-source current (I_{ds}) less than 20 mA (without a self-heating effect), that corresponds to the quiescent current at ambient temperature.

We used an ammeter to measure the I_{ds} current. The thermal stresses were performed with a THERMONICS T-2820 Precision Temperature Forcing System (PTFS); the system is designed for trouble-free temperature testing (TST and TCT) of electronic components. These equipments are easily monitored via the IEEE-488 remote interfaces and piloted by Labview software.

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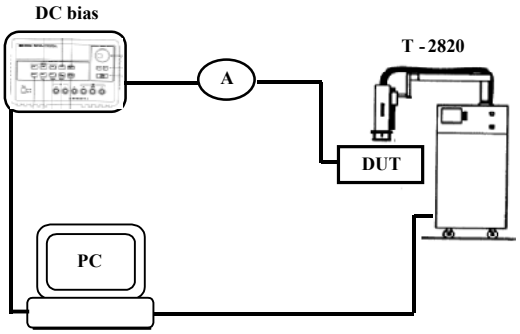

Figure 1: Synoptic of thermal stress bench

4. THERMAL STRESS CONDITIONS

This bench designed to apply both electrical and thermal stress to power RF LDMOS devices is currently implemented. Two kinds of thermal stress (TST and TCT with and without applied direct current bias) were performed. The system proposed is able to acquire the temperature over the area with high time resolution (rise and fall times less than 3s), and good temperature resolution (less than 1^0C). A cycle consists of starting at ambient room temperature (T_{amb}), proceeding to cold (T_{min}), then to hot (T_{max}), or alternately proceeding to hot, then to cold, without interruption (figure 2). For TST, the total transfer time from hot to cold (fall time) or from cold to hot (rise time) should not exceed 5 seconds. The dwell time should not be less than 10 minutes and the load should reach the specified temperature within 1 minute. For TCT, the total transfer time should not be less than 5 minutes (ramp: 30^0C/min) . The dwell time should not be less than 10 minutes and the load should reach the specified temperature within 2 minutes. For TST and TCT various conditions are investigated (Table 1) in order to establish an unequivocal conclusion on the comparison of the different tests. By means of these numerous conditions we will also be able to present the influence of extremes temperatures (ΔT) and quiescent current (I_{ds}) on power RF LDMOS devices.

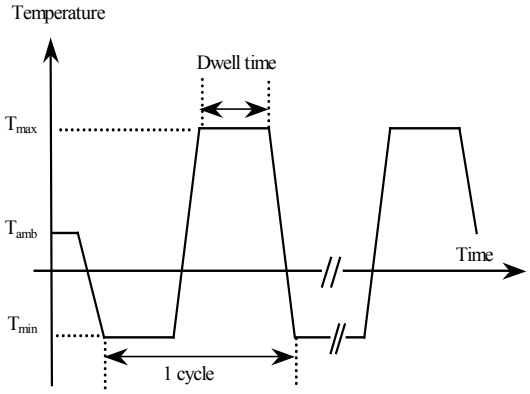

Figure 2: Typical temperature profile

Table 1: Summary of the various tests conditions with the same cycle number and dwell times

Test	Temperatures	ΔT	I_{ds} at T_{amb}
TST hot	T_{amb} / $+75^0$C	50^0C	3 mA
TST cold	T_{amb} / -25^0C	50^0C	3 mA
TST	-75^0C / $+150^0$C	225^0C	3 mA
	-75^0C / $+75^0$C	150^0C	
TCT	-75^0C / $+75^0$C	150^0C	Without DC bias
			3 mA
			6 mA

5. COMPARISON AND DISCUSION OF POSSIBLE FAILURE MECHANISMS

The preliminary results obtained highlighted shift of some electrical parameters. The failure criteria have to be confirmed and based on the increase or decrease of these parameters in accordance with the manufacturer's values. Figure 3 shows the temperature influence and the parameter R_{ds_on} degradation of TCT at different ΔT. The temperature plays a major role, more ΔT is large, more the shift is important. The rise of R_{ds_on} could be correlated to a decrease of channel current (I_{ds}) value. Figure 4 also shows the R_{ds_on} evolution with various values of quiescent current (I_{ds}). We notice that TCT without DC bias seems to be slower than TCT with DC bias. Therefore, the increase of this current and the correlation of thermal and electrical stress accelerates the parameters shift. The R_{ds_on} at 10V gate-source bias is increased from 1.14 Ohms to 1.22 Ohms in TCT with quiescent current (I_{ds}) equal at 3mA, indicating a shift by 7% but by 11% in TCT with current equal to 6mA.

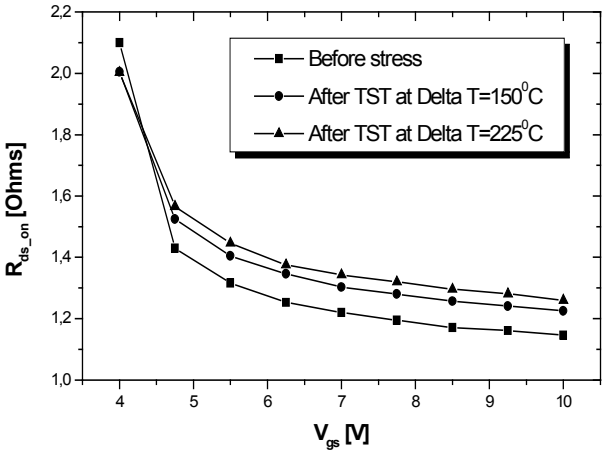

Figure 3: Variations of the R_{ds_on} at different ΔT, with V_{ds}=10mV

The proposed degradation mechanism, therefore, consists of hot carrier generated interface states (traps) and trapped electron charge which results in a build up of negative charge at the Si-SO_2 interface [4]. The location of this

charge is likely to be in the vicinity of the intersection of the impact ionization with the Si-SO_2 interface. This negative charge attracts holes depleting the charge in the LDMOS n-drift region [4] and increasing the R_{ds_on} device resistance.

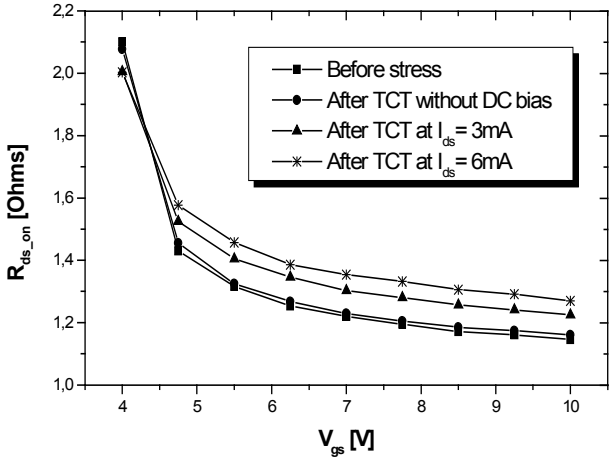

Figure 4: Evolution of the R_{ds_on} at various I_{ds} values, with V_{ds}=10mV

The feedback capacitance C_{rs} evolution after thermal stress is presented in figure 5. For this parameter the shift is more important in the TST cold than in the TST hot one. To our knowledge, no equivalent results have been reported in the literature. For instance, at 28V drain-source bias the shift is 0.50pF in TST cold but it is 0.53pF in TST hot.

Figure 6 presents the feedback capacitance C_{rs} degradation with various accelerated ageing tests. The obtained results show that this degradation with TST and TCT are approximately equal, indicating a similar degradation mechanism for these two ageing tests.

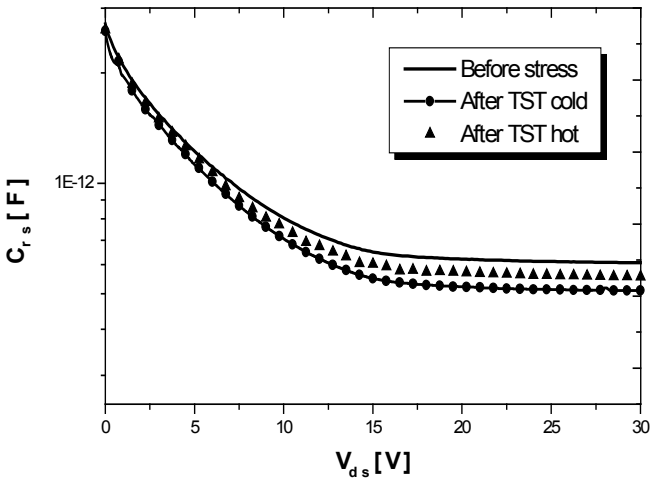

Figure 5: Comparison of C_{rs} between TST cold and TST hot, with Freq=1MHz

Moreau et al [3] have obtained the same conclusion. The C_{rs} at zero drain-source bias is reduced from 2.72pf to 2.50pf in TST, indicating a shift of 8%. Even at 28V bias, the C_{rs} is reduced from 0.57pF to 0.49pF (shift 14%). Table 2 shows the variations of obtained values for the different tests.

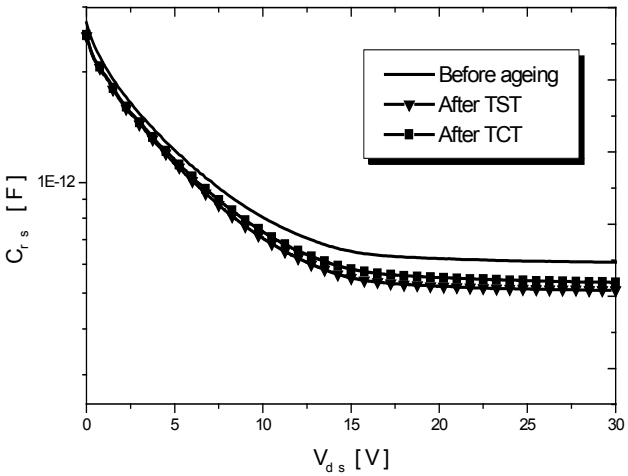

Figure 6: Evolution of C_{rs} after thermal stress, with Freq=1MHz

The origin of the observed shift could be related to the presence of very high electric field which increase carrier injection into the thermally grown silicon dioxide layer (SiO2) and into state interface Si/SiO_2 [5,6,7]. A detail of the lateral electric field distribution for power RF LDMOS transistor of the active silicon layer in channel and drift regions is shown in figure 7, one using a physical simulation software (Silvaco-Atlas, 2D).

This strong electric field causes the generation of charge states at the silicon-oxide interface [4,8]. Since the LDMOS is used in these conditions, where drain is biased with high voltage (meadows of the breakdown voltage) simultaneously with thermal excitation due to thermal cycling and shock (make easy the current flow), translated the correlation of thermal and electrical stress.

The hot carrier degradation effect is closely related with current density and with the total number of free electrons at the silicon-oxide interface, where most of the electrons are concentrated deep inside the drift region [4,6,9]. These results are proved by Silvaco-Atlas simulator (figures 8 and 9). In other words, the drain-source voltage increases the electric field in the drift region and near the oxide layer, increasing the temperature and enhancing the trapping process. Consequently the degradation rate is accelerated [6,10]. To reduce the possibility of electrons be trapping in the oxide-silicon interface, the current line must be moved away and the electric field must be decreased in this zone in order to improve the device reliability.

Table 2: Summary of the parameter values variations obtained after thermal stress

Parameter	Before stress	After stress						
		TST hot	TST cold	TST		TCT		
				$\Delta T = 150^0C$	$\Delta T = 225^0C$	I_{ds} = 0mA	I_{ds} = 3mA	I_{ds} = 6mA
R_{ds_on} (Ω) V_{gs}=10V	1.14	1.19	1.20	1.22	1.26	1.16	1.22	1.27
C_{rs} (pF), V_{ds}=0V	2.72	2.65	2.60	2.50	2.46	2.70	2.51	2.43
V_{ds}=28V	0.57	0.53	0.50	0.48	0.46	0.57	0.48	0.45

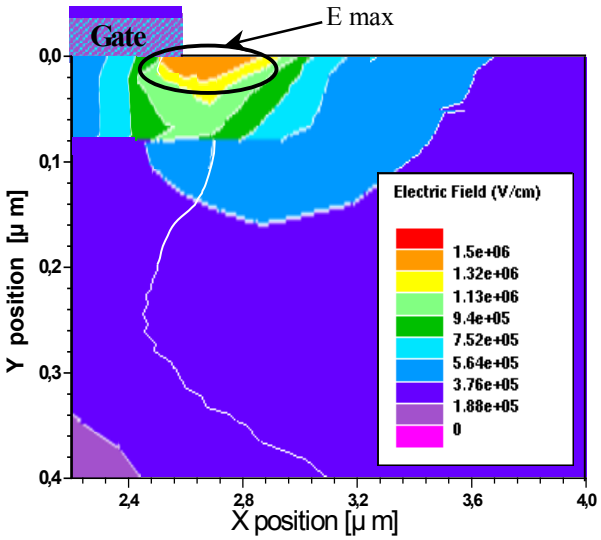

Figure 7: Simulated electric field contour of N-LDMOS, with V_{ds}=40V and V_{gs}=3.5V bias

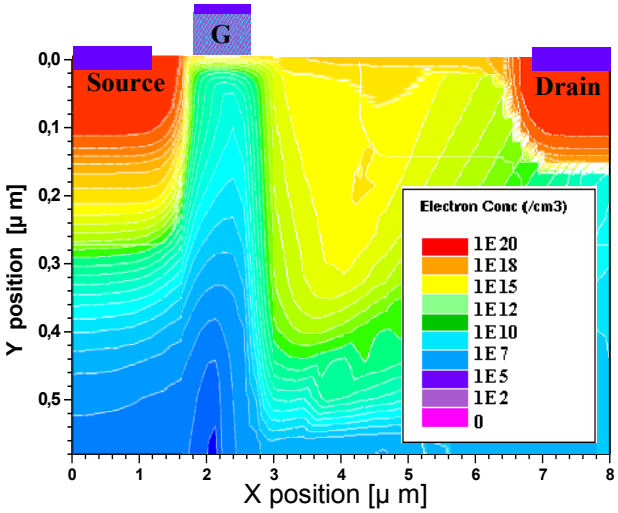

Figure 9: Electron concentration distribution of N-LDMOS, with V_{ds}=40V and V_{gs}=3.5V bias

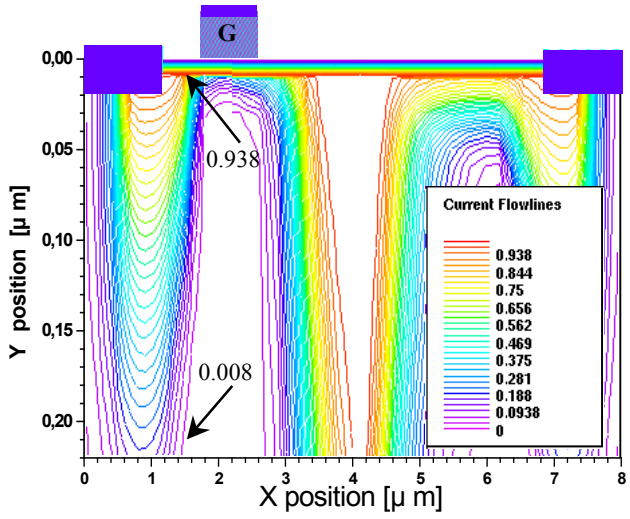

Figure 8: Simulated source to drain current flow lines of N-LDMOS, with V_{ds}=40V and V_{gs}=3.5V bias

6. CONCLUSION

The results obtained highlighted a shift of some electrical parameters as: on-state resistance (R_{ds_on}) and feedback capacitance (C_{rs}). In other words, the characteristics degradation of MOS transistors is not the same for all the parameters and for the different thermal stresses. We conclude, that TCT and TST seem to be equivalent because they apparently produce the same degradations. The TST cold test seems to induce faster degradation than the hot TST. The parameters shift is sensitive to extremes temperatures variation ΔT and quiescent current I_{ds}. The evolution of the device's principal parameters can be used to evaluate its reliability and lifetime, allowing correlation to be established between the electric parameter drift and the applied stress.

7. REFERENCES

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