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Two-Dimensional Temperature Fields in ASICs for Multiple Heat Sources of Arbitrary Power Dissipation Derived from Conformal Mapping Theory

Adam Augustin, Arno Kostka
Technical University of Darmstadt
Solid State Electronics Laboratory
Schlossgartenstr. 8
D-64289 Darmstadt, Germany
Email: augustin@iht.tu-darmstadt.de
kostka@iht.tu-darmstadt.de

Bartosz Maj
Continental Teves AG
Mixed Signal IC Development
P.O. Box 90 01 20
D-60441 Frankfurt, Germany
Email: bartosz.maj@contiteves.com

Abstract— The subject of this paper is the temperature distribution in ASICs generated by multiple rectangular stripe sources on the surface of the ASIC calculated with conformal mapping theory. All presented solutions are fully analytical, and contain geometrical and heat power parameters, only. The influence of these parameters and the temperature distribution strategies can therefore be examined directly and easily, as is e.g. necessary for placement optimization.

The solutions are applied to two examples with multifinger structures. In the first, the sources consist of power DMOS transistors that exhibit thin and long fingers. The results are compared with equivalent ANSYS simulations, and show a very good agreement. In the other example used in high frequency applications, the source length is shorter, making an appropriate correction for the three-dimensional effects necessary. For both applications, the temperature distribution is shown for different layers on top and inside the chip.

I. INTRODUCTION

In many applications, the interest in temperature distribution within semiconductor chips is focused on the upper surface of such devices, since the heat sources are positioned there and the highest temperatures are expected. When the sources are placed near to each other, a strong interaction between them can be noticed, which is mainly depending on the dissipated power density within the sources and the distance between them. Numerical approaches like the finite elements method make it difficult to vary the geometrical model parameters and process the calculations in a short period of time. An analytical model, which is developed in this paper with the help of conformal mapping techniques, offers here decisive advantages calculating the temperature, since all geometrical parameters are included in such models. So, the source interaction can be verified easily and fast.

Conformal mapping theory has been extensively used to calculate electro-magnetic fields [1], [2], and more

recently to determine carrier distributions. Connected with this, the electrical currents [3]–[6] in semiconductor devices, and capacitances of complicated geometries [7] have been determined. Though the physical description of thermal problems is based on the Laplace equation, too, the method of conformal transformation has not been used to calculate thermal problems, although some suggestions are made in [8], and in [1] presented in details. By choosing an appropriate conformal transformation, it can be guaranteed that all necessary mapping functions remain analytical, which is a big advantage for computation.

In previous work of the authors [9] the conformal mapping method was introduced to calculate steady state temperature fields on surfaces of ASICs. With the presented solutions it is possible to calculate the temperature field in the vicinity of a heat source with constant temperature positioned inside the chip or near the chip edge. The work presented in this paper improves the applicability to real world problems by allowing multiple heat sources with arbitrary power dissipations, on multi-layer substrates.

In high frequency and power applications, multifinger devices like bipolar or MOS transistors can be found very often. For example, in [10] and [11] the temperature distribution within such structures is discussed. For example, in [11] the temperatures for a multigate MESFET in a multi-layer structure are calculated. Because of the very complex numerical calculations, the solution had to be restricted to five layers and five fingers. By using the analytical solutions presented in this paper, such a restriction would not have been necessary.

The structure of this paper is as follows. In section II a short summary of the most important parts of the conformal mapping theory, needed in this paper, will be presented. In section III, solutions of the Laplace equation will be shown, which will be used in section IV, where

a suitable conformal transformation for the multi-source ASIC problem will be developed. In section V, results for two multifinger multi-layer problems will be presented and discussed. Finally, in section VI some concluding remarks will be made.

II. MATHEMATICAL BASICS

If the source geometry is of such a kind that a simplification into a two-dimensional problem can be made, the steady state differential heat conduction equation simplifies to a two-dimensional Laplace equation

$$\Delta P = \frac{\partial^2 P(x, y)}{\partial x^2} + \frac{\partial^2 P(x, y)}{\partial y^2} = 0 \quad (1)$$

and conformal mapping techniques can be used to solve it [8]. Using conformal mapping requires that all heat sources or sinks are positioned at the boundaries of the examined area, and the temperature distribution is not time dependent. This is the case for planar semiconductor devices used under static operating conditions.

The aim of the transformation of thermal problems with help of conformal mapping is to transform a given geometry (in the z -plane) which is not elementarily solvable, into a solvable geometry (in the w -plane) and to calculate the necessary parameters there. This procedure is described in detail in [9]; its most important parts are repeated here in the following section, for completeness and ease of understanding.

Conformal mapping

The geometries analysed in this paper are bounded by polygons, so that the Schwarz-Christoffel transformation can be applied [1], [8]. With the help of the Schwarz-Christoffel transformation it is possible to map the interior of a polygon in the z -plane into the upper half of the w -plane. In doing so, the polygon itself will be mapped on the real axis in the w -plane. The transformation which does this is obtained from the relation [1]

$$\frac{dz}{dw} = C \prod_{i=1}^N (w - w_i)^{-\gamma_i} \quad (2)$$

Integrating Eq. (2) one will obtain the wanted conformal mapping

$$f(w) = C \int \prod_{i=1}^N (w - w_i)^{-\gamma_i} dw + D \quad (3)$$

where $\pi\gamma_i$ are the interior angles of the polygon w_i are the points on the real axis into which the angular points transform C and D are constants, whereof D defines the point of origin in the z -plane. As one moves along the boundary of the polygon counter clockwise, all points inside the polygon are mapped onto the upper half of the plane. Additionally, in order to calculate all parameters of the conformal mapping, some of the relations of the geometry in the z -plane including the behavior of the

infinite points are needed. Especially, the angle $\pi\gamma_j = \pi$ represents a vertex at $z_j = \pm\infty$, or the intersection of two parallel lines with a distance of [1]

$$z_j'' - z_j' = -i\pi C \prod_{i \neq j}^N (w_j - w_i)^{-\gamma_i} \quad (4)$$

If additionally $w_j = \infty$, then the distance can easily be written as

$$z_j'' - z_j' = i\pi C \quad (5)$$

If N represents the number of the vertices of the polygon, then, with the points w_i and the integration constants C and D , one arrives at $N+2$ constants, whereof a maximum of three can be chosen arbitrarily. With three points chosen on the boundary of the polygon along with the arbitration, where these points will be mapped onto the w -plane, the conformal mapping is determined. The remaining $N-1$ constants can then be calculated through (4), (5) or other geometrical relations (e.g. symmetries) in order to solve the mapping problem completely.

The mapping of the polygon in the z -plane onto the upper w -plane is conformal at all points except at the vertices themselves. These vertices however, are isolated points of non-conformity and can be arbitrarily closely approached.

A function with continuous second partial derivatives which satisfies (1) is called a potential function. An interesting property of the complex potential function should be pointed out. It is true, with $z = x + iy$, for a complex potential function

$$P(x, y) = T(x, y) + i\Xi(x, y) \quad (6)$$

that if the real part T describes the temperature distribution, then the thermal flux is given by the imaginary part Ξ [1].

III. SOLUTION FOR ONE HEAT SOURCE OF ARBITRARY POWER DISSIPATION

Fig. 1 shows a typical situation for an ASIC with a heat source placed on the top surface. The solution will

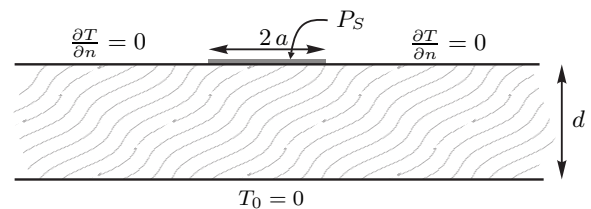


Fig. 1. Cross-section of an ASIC with one source of arbitrary power dissipation P_S , width $2a$, and infinite length (perpendicular to the figure plane)

be derived in two steps. In the first, a heat source placed on a semi-infinite area with boundary conditions as on the upper surface of Fig. 1 is treated. In the second, the solution for the original geometry including the lower

surface with $T_0 = 0$, will come out using an appropriate conformal mapping.

A. Solution for one heat source

For a finite heat source placed in an elsewhere adiabatic semi-infinite area, the complex solution of the Laplace equation (1) with $w = u + iv$ is given by [1]

$$P(u, v) = -\frac{P_S}{2\pi\lambda} \operatorname{arccosh}\left(\frac{w}{a}\right), \quad (7)$$

where λ denotes the thermal conductivity, and P_S denotes an arbitrary power dissipation per unit length dissipated inside the source with width $2a$ into the upper half of the w -plane. Fig. 2 shows a two-dimensional plot of solution (7). This solution satisfies the boundary conditions

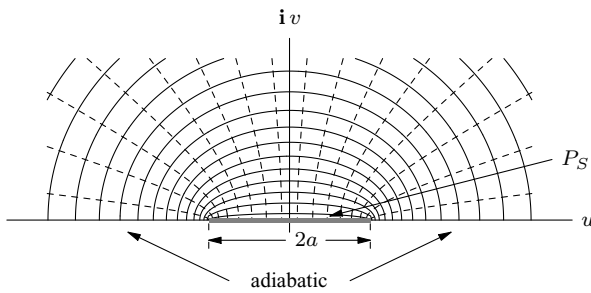


Fig. 2. Solution for a heat source of width $2a$ with arbitrary power dissipation, and constant temperature with the source. Solid lines are indicating the isotherms, dashed lines show the current flow

of adiabaticity outside and given total power dissipation P_S within the source. Analyzing solution (7) for the power dissipation density and the temperature variation within the source delivers the results that the temperature is constant and the heat flow density continuously increasing from the middle to source edges. In most applications, this is not the case, because the power dissipation there is homogeneously distributed over the entire source. In cases where this effect strongly influences the results, corrections for it have to be applied (see next section). On the other hand, where the power dissipation density within the source is not a critical fact, in some distance from the source, the solution (7) provides a good approximation to reality.

B. Corrections within the heat source

For a better approximation of constant flow density within the source, the temperature should decrease from the center to the edges. This was addressed by adding corrections to solution (7). In search for potential functions following such a boundary condition within the source, the function

$$P_A(u, v = 0) = -f \frac{P_S}{2\pi\lambda} \arctan\left(\frac{\sqrt{1 - (w/a)^2}}{(w/a)}\right) \quad (8)$$

provides help. With this, the distribution of the power dissipation over the entire heat source can be changed. This asymmetric function is another solution of Eq. (1)

with other boundary conditions: constant heat flow within the heat source, and constant temperature outside the heat source. When adding Eq. (7) and Eq. (8), a corresponding correction of the power P_S dissipated within the source can be made, whose amount is considered by an appropriate parameter f . The value of f is depending on two facts: the dissipated power P_S and the source width $2a$. Comparison with numerical results, and physical insight show that f rises as a rises and P_S falls.

Because of the asymmetric nature of Eq. (8), only the use of one half of this solution is useful. Therefore, a suitable conformal mapping, as presented in section IV is necessary to mask out the undesirable part of the solution. Because of this procedure (Eq. (8) together with a suitable map) the use of the sum is restricted only to the top surface of the chip in Fig. 1. This is the reason why $v = 0$ is suggested in Eq. (8).

C. Hetero-layer structures

Using the technique of equivalent-material substitution, a solution of a static problem can be used to describe multi-layer structures, too. Hetero-layer structures can be examined as one material if equivalent thicknesses are introduced depending on thermal conductivity.

$$d_{equivalent} = \frac{d_{mat}}{\lambda_{mat}} \lambda_{Si} \quad (9)$$

With these conversions it is guaranteed that the thermal resistance for each substituted layer stays the same as for the original material. The thermal conductivity λ_{Si} stands here for silicon as the replacing material. Obviously, using this procedure there are no limitations in number of layers.

D. Multifinger sources

The analytical solutions like Eq. (7) or Eq. (7) + Eq. (8), can be used to calculate temperature distributions for multifinger structures, too. Because of the linearity of the problem, the solutions for different sources must only be shifted to the right spots, and added up. Thus, the solution for n fingers of equal width ($2a$) and distance s can be written in the z -plane as

$$P_n(x, y) = \sum_{i=1}^n P(x + s \cdot (i - 1), y) \quad (10)$$

using the parameter s for the distance between the middle lines of the sources.

IV. A SUITABLE CONFORMAL MAPPING

When the solutions for symmetrical structures like that in Fig. 2 are already known (Eq. (7)), the finding of the mapping transformation together with its inverse is the main concern for the solution of the complete problem. If one is to arrive at analytical results in elementary form, the existence of an elementary inverse to the transformation is essential. Without it, the Laplace equation (1) can be solved, but the influence of the different parameters on the results can only be interpreted numerically.

To allow the use of the solutions presented in the previous section, the chip structure, shown as a cross-section in Fig. 1, must be expanded in such a way, that the polygon in the z -plane, which will be mapped onto the real axis of the w -plane, does not include boundaries with constant temperature (the lower surface). For this, the entire chip is mirrored on the bottom side ($y = d$ in Fig. 3) with a change in sign for temperature and powers. Because of the symmetry it is sufficient (and because of the asymmetry of Eq. (8) necessary) to examine only one half of the problem ($x \geq 0$ in Fig 3). The resulting geometry in the z -plane is shown in Fig. 3 together with the corresponding w -plane. The upper half of the structure in the z -plane represents the right half of the chip from Fig. 1.

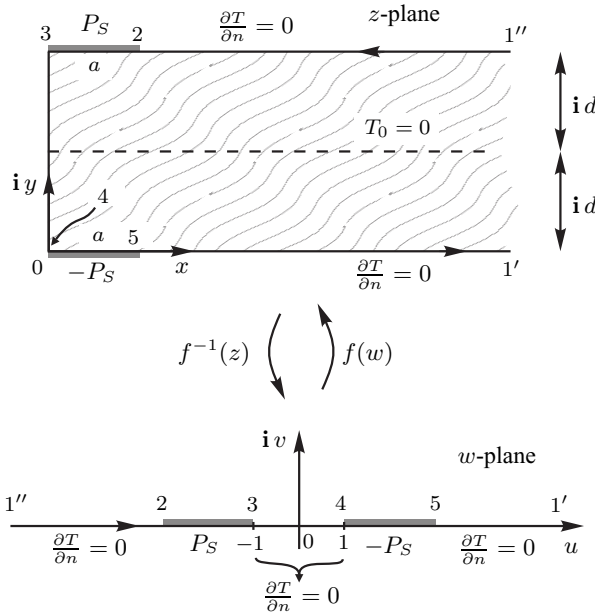


Fig. 3. z - and w -plane with all important points for the transformation

TABLE I

MAPPING OF ALL POINTS FROM FIG. 3. ITALIC HIGHLIGHTED POINTS ARE CHOSEN ARBITRARILY

i	1	2	3	4	5
z_i	$z_1' = \infty$ $z_1'' = \infty + i2d$	$z_2 = a + i2d$	$z_3 = i2d$	$z_4 = 0$	$z_5 = a$
γ_i	1	-	1/2	1/2	-
w_i	$w_1' = \infty$ $w_1'' = -\infty$	w_2 see Eq. (14)	$w_3 = -1$	$w_4 = 1$	w_5 see Eq. (14)

Table I summarizes all necessary information to determine the mapping function following the procedure described in section II. With Eq. (3) one gets [12]

$$z = C \int \frac{1}{\sqrt{w^2 - 1}} dw = C \operatorname{arccosh}(w) + D. \quad (11)$$

The constants C and D can be calculated using z_1 and z_3 , so that with $C = \frac{2d}{\pi}$ and $D = 0$ it arises for the transformation

$$z = f(w) = \frac{2d}{\pi} \operatorname{arccosh}(w) \quad (12)$$

and for the reverse function

$$w = f^{-1}(z) = \cosh\left(\frac{\pi z}{2d}\right). \quad (13)$$

For the unknown points w_2 and w_5 it follows now

$$w_5 = -w_2 = \cosh\left(\frac{\pi a}{d}\right). \quad (14)$$

A. Solution for the top surface

Now, the solution for the problem in the w -plane of Fig. 3 can be made using functions (7) and (8). The complete solution in the w -plane comes out by shifting (7) and (8) to their proper location:

$$\begin{aligned} P(w)_{top} &= -\frac{P_S}{2\pi\lambda} \operatorname{arccosh}\left(\frac{w + \frac{w_5+1}{2}}{\frac{w_5-1}{2}}\right) \\ &+ \frac{P_S}{2\pi\lambda} \operatorname{arccosh}\left(\frac{w - \frac{w_5+1}{2}}{\frac{w_5-1}{2}}\right) \\ &- f \frac{P_S}{2\pi\lambda} \arctan\left(\frac{\sqrt{1 - \left(\frac{w+1}{w_5-1}\right)^2}}{\frac{w+1}{w_5-1}}\right) \\ &+ f \frac{P_S}{2\pi\lambda} \arctan\left(\frac{\sqrt{1 - \left(\frac{w-1}{w_5-1}\right)^2}}{\frac{w-1}{w_5-1}}\right). \end{aligned} \quad (15)$$

The first expression stands for the positive left source, the second for the negative right source (both sources regarded as entire), the third term corrects the temperature distribution within the left source and the last term is correcting within the right source. For the asymmetric solution (8) the points w_3 and w_4 must be regarded as middle points of the sources. Therefore, the entire solution for the left part in the w -plane is a composition of half and full source solutions. The left source in the w -plane of Fig. 3 is representing the heat source on the chip in the z -plane, because the real part of Eq. (8) (stands for the temperature) for $v = 0$ is zero outside the sources, the last term in Eq. (15) can be neglected. Now, by inserting the conformal mapping (13) the solution for the original geometry will be obtained.

Formula (15) (with (13)) is usable only for the top surface of the chip ($y = 2d$ in Fig. 3) in the z -plane, because of the special treatment of Eq. (8). For the region inside the chips the solution is presented in the next section.

B. Solution within the chip

To obtain the solution for the region within the chip the correcting parameter f in Eq. (15) must be set to zero. This is necessary, because of the special treatment of the correcting function (8) by the conformal transformation (13). So, for the solution within the chip it follows

$$P(w)_{inside} = -\frac{P_S}{2\pi\lambda} \operatorname{arccosh}\left(\frac{w + \frac{w_5+1}{2}}{\frac{w_5-1}{2}}\right) + \frac{P_S}{2\pi\lambda} \operatorname{arccosh}\left(\frac{w - \frac{w_5+1}{2}}{\frac{w_5-1}{2}}\right). \quad (16)$$

Again, with Eq. (13) the solution for the original geometry in the z -plane will be obtained.

V. APPLICATION ON MULTIFINGER, MULTI-LAYER DEVICES

In many practical cases of power devices within ASICs, the length of the source is large compared to its width, and to the thickness of the chip, what then allows a two-dimensional representation of the temperature field below and beside it. For shorter length, and thicker chips two-dimensional solutions may be regarded as approximation.

In [9] the authors have presented an application of the conformal mapping technique on two examples. First, a temperature rise which will be detected by a sensor near a long heat source was examined. This typical kind of sensing is often used to monitor the temperature near expected hot spots within an ASIC with power DMOS-arrays. Second, calculations for heat sources near the chip edge where the influence of an adiabatic edge can not be neglected, were presented. The solutions presented in this paper can also be used to calculate the same problems, but with the deciding improvement that the controlling parameter, temperature within the sources, has been replaced by an arbitrary power dissipation, i.e. the boundary conditions for the heat sources are more realistic, now.

In the following sections, we analyze two examples of multifinger heat sources on chips regarded as multi-layer structures in some detail, using the solutions of section IV-A and IV-B, and comparing them with numerical ANSYS results.

A. Multifinger structures in power stages of ASICs

On an ASIC used in automobile applications for braking systems, there are placed a number of heat sources (up to twenty), all showing multifinger structures. The heat sources consisting of DMOS-arrays are used in electronic breaking systems to drive hydraulic valves controlling the vehicle deceleration.

A typical example of these sources is a heat source consisting of 16 fingers with $20 \mu\text{m}$ width and $2000 \mu\text{m}$ length. The distance between the fingers is $10 \mu\text{m}$, which results in $s = 30 \mu\text{m}$. The other data are: $T_{amb} = 375 \text{ K}$ and $P = 3.2 \text{ W}$ what leads to $P_S = 100 \text{ W/m}$ per finger.

TABLE II
LAYER STRUCTURE OF AN ASIC. EQUIVALENT THICKNESS IS CALCULATED USING SILICON

layer	conductivity W/mK at 375 K	thickness μm	equiv. thickness μm
silicon	120	350	350
die attach	4	25	750
lead frame	301	100	40
solder	50	100	240
heat sink	146	500	411

The layer structure of the examined ASIC is shown in Table II. The non-silicon layers are replaced by silicon of equivalent thicknesses calculated from Eq. (9). Because of the symmetry the right side of the heat source (eight fingers) is shown in Fig. 4, only. The figure shows the

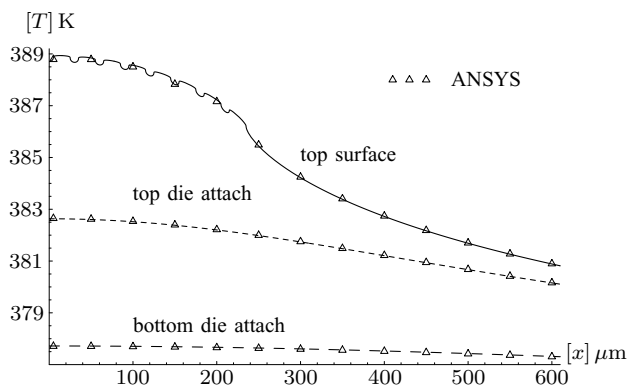


Fig. 4. Temperatur distribution for different layers compared to an equivalent ANSYS simulation (triangles) for infinite sources

calculated temperature distribution for different layers compared to an equivalent ANSYS simulation for 16 infinite fingers. The solid line indicates the temperature at the surface of the silicon calculated from Eq. (15) with $f = 0.6$. The dashed line (- -) shows the temperature on the bottom of the chip. The line with the smallest gradients (- · -) indicates the temperature on top side of the lead frame at the equivalent depth of $1100 \mu\text{m}$. As can be seen, the agreement between the two methods is almost perfect for each layer.

To see what happens on and under the sources directly, Fig. 5 illustrates the temperature distribution on the surface and in $5 \mu\text{m}$ depth (- -) compared to the ANSYS simulation. Generally, the behavior of the analytical curves is very near to the numerical data. At the edges of the sources the analytical data is not so smooth as ANSYS because of the slightly different boundary conditions.

For comparison, the temperature on top surface (fine dashed) is calculated for $f = 0$ (solution without corrections within the sources). The uncorrected curve shows a typical spiky behavior for composed solutions

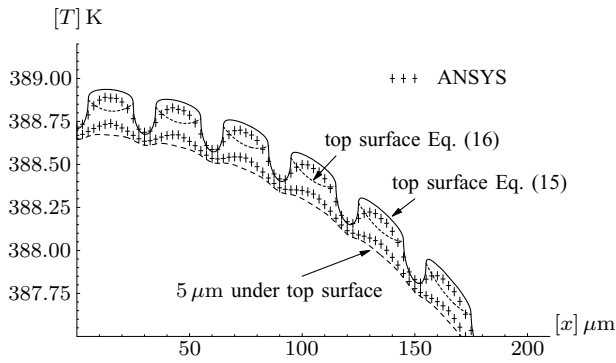


Fig. 5. Magnification of the temperature curve from Fig. 4 near the heat sources compared to an equivalent ANSYS simulation (crosses). Solid line indicates the temperature on the top surface of silicon calculated with Eq. (15). To show the influence of the correction function (8) within the sources, Eq. (16) is plotted for the top surface (fine dashed). Dashed line shows the layer at $5 \mu\text{m}$ under silicon top surface

of heat sources with constant temperature. Only by using the appropriate value for the correcting parameter f in Eq. (15), a smooth crossing from one source edge to the other can be achieved.

The temperature rise within the sixteen fingers amounts to 2 K, and the dips between the fingers to about 0.25 K, or 12 % thereof. Because of this, one could also take a smooth average for the overall result, which then does describe a wide source with approximately constant power density.

To realize how big the error is using the infinite source solutions for the description of the problem with finite source lengths ($L = 2000 \mu\text{m}$), an additional ANSYS simulation for the real finite fingers was made. The tem-

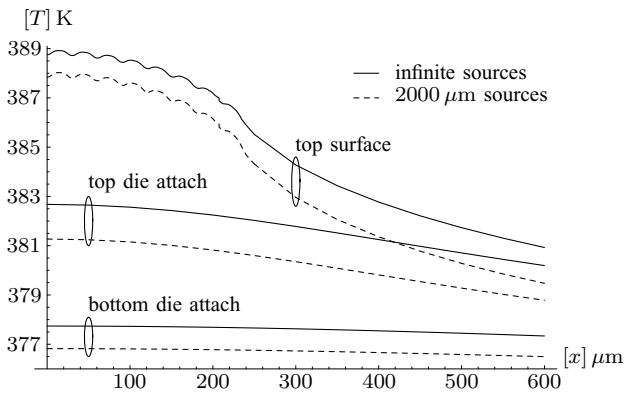


Fig. 6. Comparison of two ANSYS simulations for different layers as in Fig. 4. Solid lines stand for infinite fingers, and dashed temperature curves show the gradients in the middle of the finite sources with $2000 \mu\text{m}$ length

perature distribution of the finite sources is calculated for a cut in the middle of the sources, for better comparison and to avoid the influence of edge effects. Fig. 6 shows the results for the same layers as in Fig. 4. As could be expected, all temperatures of the infinite multifinger structure are a bit higher than for the finite sources, so

for this reason, the conformal mapping method can be used to calculate an upper limit. But, the gradients in each layer are well comparable (even almost equal). Shifting the calculated curves by an appropriate value, even an almost exact temperature distribution in each layer can be represented by the analytical solution.

B. Multifinger devices for high frequency applications

In [11], a multifinger HF device has been examined. The heat source consists of a multigate MESFET realized on a multi-layer chip. Under consideration of different, temperature dependent thermal conductivities for each layer material, the temperature distribution within the layer interfaces was examined. Table III shows the geometrical

TABLE III
GEOMETRICAL PARAMETERS OF A MULTIFINGER GAAS MESFET

parameter	value in [11]	value here
gate length (source width $2a$)	$1 \mu\text{m}$	$a = 0.5 \mu\text{m}$
unit gate width (source length L)	$100 \mu\text{m}$	infinite
gate to gate spacing		$40 \mu\text{m}$
number of gates		5

parameters for the multigate structure. The dissipated power used in [11] is $P = 1 \text{ W}$ in all five MESFETs together, which leads to $P_S = 2000 \text{ W/m}$ for one finger.

In our analysis, using material substitution, all layers listed in Table IV are replaced by n-GaAs (the active layer) of equivalent thicknesses calculated with Eq. (9). For the total thickness of the resulting single layer problem consisting of n-GaAs one obtains $1368.82 \mu\text{m}$. The chip is covered by epoxy mold compound which causes an adiabatic top surface of the chip.

Compared to the application of the previous section, the biggest difference in this section are the relative dimensions of the structures. Here, the distance between the short fingers is much larger than the width of a single finger, and three-dimensional effects appear stronger because of the smaller source length to chip thickness ratio. From all this, a rather different behavior should be expected.

Fig. 7 shows a cross-section ($70 \mu\text{m}$ high) of the region near the five heat sources with the calculated isothermals (solid) and thermal current flow lines (dashed). The shape

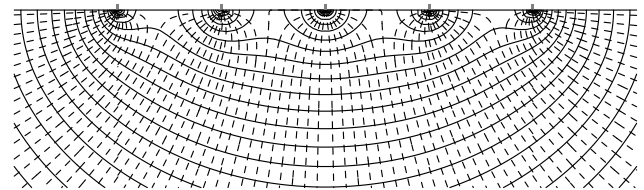


Fig. 7. Upper region ($70 \mu\text{m}$ high) near the five heat sources with isothermals (solid) and current flow lines (dashed)

TABLE IV
LAYER STRUCTURE OF AN EXAMINED DEVICE. ALL VALUES EXCEPT "EQUIVALENT THICKNESS" ARE TAKEN FROM [11]

layer	material	thermal conductivity W/mK at 300 K	thickness μm	equivalent thickness μm
metallization	gold	317	3	0.53
active layer	n-doped GaAs	56.16	0.34	0.34 (unchanged)
epi-bulk	undoped GaAs	57.95	100	96.9
die attach	epoxy mold compound	4	25	351
lead frame	aluminium oxide	36	500	780
heat sink	copper	401	1000	140.05

of the isothermals near the surface is undulating around the separated sources, and there are deep dips between the sources.

The results are displayed as solid curves in Fig. 8 and magnified in Fig. 9. The temperature dips here are extremely pronounced, and account for the major part of the temperature variation. The absolute temperature values come out about 70 K higher than in [11] because of the neglect of the large three-dimensional effect. Obviously, this does not much influence the relative values. The

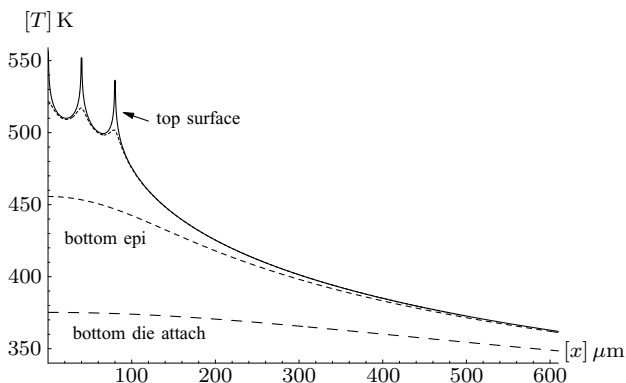


Fig. 8. Temperature distribution for different layers at $T_{amb} = 300$ K

differences between the maxima within the sources and the neighbouring regions are quite identical. Both values, as marked in Fig. 9 are equal to the results presented in [11], but calculated with a minimum cost of computational time. In this calculation, the factor f is not very relevant (< 0.1), or could be even taken to zero, because there is no significant temperature variation within the thin sources.

Also interesting is the temperature distribution for different depths of the structure. Fig 8 shows such curves, for the same layers as in [11]. The dotted curve shows the temperature in $5 \mu\text{m}$ depth, which can be seen more detailed in Fig. 9. Another temperature path (- -) at the bottom side of the epi-bulk at $97.77 \mu\text{m}$ equivalent depth is shown. The smallest gradients shows the curve (- -)

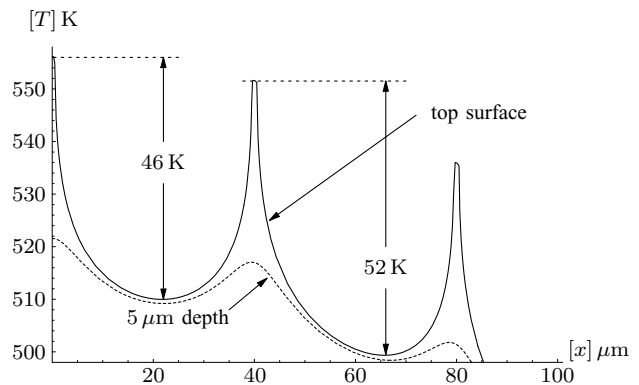


Fig. 9. Magnification of Fig. 8 near the heat sources. Solid line indicates the temperature on the top surface, dotted line shows the layer $5 \mu\text{m}$ under the surface

on the top surface of lead frame, at the equivalent depth of $448.77 \mu\text{m}$. All curves show the expected behavior.

VI. CONCLUSIONS

The work presented here introduces an easy to use and fast method to calculate the temperature in semiconductor chips. Holding on this, it doesn't matter, where or for which position within the chip the temperature has to be calculated, since all solutions are of analytical kind, and expressed in elementary functions. Because also the power dissipation can be found as a parameter, the solutions provide an improvement of [9]. The analytical kind of the solutions allows for a very easy and straight forward implementation into software projects.

Despite the two-dimensional character of the method, the solutions provide a good approximation for quasi two-dimensional problems, as could be verified by two different examples presented in section V. In the first example in section V-A, the method provides good results already for ratios $L/d \geq 1.1$ (with the source length L and chip thickness d), although the sources are finite. For shorter sources on the other hand, as seen in section V-B, the approximation is not so good with respect to absolute values, but it provides very realistic temperature distributions, and

exact temperature gradients on the top surface, which can be used to optimize the source distances with respect to all parameters, especially the power dissipation P_S , source width a and distance s between the sources. In any case, for finite source problems the solutions can always be used as upper limits with a minimum cost in computational time.

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