Hierarchical Variance Analysis for Analog Circuits Based on Graph Modelling and Correlation Loop Tracing

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Abstract

Process variations play an increasingly important role on the success of analog circuits. State-of-the-art analog circuits are based on complex architectures and contain many hierarchical layers and parameters. Knowledge of the parameter variances and their contribution patterns is crucial for a successful design process. This information is valuable to find solutions for many problems in design, design automation, testing, and fault tolerance. In this paper, we present a hierarchical variance analysis methodology for analog circuits. In the proposed method, we make use of previously computed values whenever possible so as to reduce computational time. Experimental results indicate that the proposed method provides both accuracy and computational efficiency when compared with prior approaches.

1. Introduction

As semiconductor manufacturers push the boundaries of the process technology, a steady trend has been shrinking the feature sizes. One direct result from the reduction in device sizes is the increasing importance of the role of process variations. As devices are scaled down to their physical limits, precise control over process parameters becomes nearly impossible, resulting in larger percentage variations in the parameters at each level of the design hierarchy.

Process variations affect the performance of analog and digital circuits alike, as performance parameters, such as gain, frequency of operation, or path delay, are directly influenced by process parameters. Thus, increased variations in process parameters will also increase variability in performance parameters at the circuit and the system level. An analysis of such parametric variations is needed for many problems in VLSI design, design automation, testing, and fault tolerance. There is an increasing need to incorporate process variations into the design flow from early design stages and understand which parts of the design are the most important contributors.

Since statistical tolerance analysis has been widely used for many applications in industry for several decades, a plethora of approaches have been developed for various application domains over the years. Evans [7] provides a detailed application background on state-of-the-art tolerance analysis approaches.

A popular variance analysis approach has been the collection of statistical data through simulating many instances of the circuit. The most well known and widely used sample-and-simulate technique is the Monte Carlo analysis. Taguchi's method [14] and modified Taguchi's method [6], which are based on deterministic sampling, have been proposed as more reliable alternatives to the Monte-Carlo analysis. However, the large number of *required* simulations (3^n) prohibits their use beyond a handful of parameters.

Due to its tractability, worst-case min-max analysis based on a sensitivity-weighted addition of tolerance windows has been intensively used in many fields [15]. Hierarchical analysis based on Monte-Carlo and sensitivity analyses has also been introduced as a compromise [9].

Recently, variance analysis of path delays has attracted much attention in the digital domain [1, 5, 11], where the problem typically involves three levels of hierarchy (transistor level, gate level, and path level) and a single parameter (delay). While computing the delay variance of a path, correlations among the gate delays have been taken into account through their covariances [5, 11]. In [11], sensitivity analysis is used to derive the relations between gate delays and process variables. However, instead of min-max analysis, the covariance of each pair of gate delay is computed based on the sensitivity information and this information is used to update the tolerance bounds computed under the independent assumption. A similar approach is taken in [5] while the covariances are assumed to be fixed between the gates and specified by the system designer. In [10], we have developed a theoretical basis for variance analysis of analog circuits. The approach in [10] is based on computation of correlation coefficients along a hierarchical path.

In this paper, we propose a variance analysis method that is specifically geared towards information re-use. We model the circuit representation as a tree and re-use the variance information at each hierarchical layer. The method takes advantage of identification of correlation loops in the hierarchical structure so as to avoid re-calculation of previously computed values. Such information re-use is extremely helpful during design iterations where only minor changes are made to the circuit.

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2. Hierarchical Variance Analysis

In analog circuits, a small number of transistors constitute building blocks (such as current mirrors, diff-amp pairs, etc.), several building blocks constitute modules (such as an OPAMP), and modules are connected in a network to build the circuits (such as a filter or an ADC). The relations among the circuit parameters at various levels can be defined either through approximate behavioral models, or through simulator-based models, such as the sensitivity analysis. Thus, there is inherently a hierarchical construct followed during the design process. The behavior of the circuit can be generalized as follows:

$$P_{i^{(r)}} = f_{i^{(r)}}(P_{1^{(i-1)}}, P_{2^{(i-1)}}, ..., P_{NP_{i-1}^{(i-1)}})$$

where $P_{i^{(r)}}$ denotes the ith parameter at the hierarchy Level-r, $f_{i^{(r)}}$ denotes its functional relation in terms of parameters one level down in the hierarchy, and NP_r denotes the number of parameters at the hierarchy Level-(r).

In general, the covariance analysis for the linear system with normally distributed inputs can be conducted hierarchically through chainwise matrix multiplications [4]:

Let $\mathbf{A} : \mathrm{R}^n \rightarrow \mathrm{R}^m, linear, and\ \mathbf{x} \sim N_n(\mu, \mathbf{\Sigma})$. *Then,* $\mathbf{Ax} \sim N_m(\mathbf{A}\mu, \mathbf{A\Sigma A}')$.

The coefficients of the matrix $\mathbf{A}$ can be formed by the sensitivities between adjacent levels since first order Taylor approximation always results in a linear relation between variances in adjacent levels. As a result, the covariance matrix can be propagated hierarchically.

Although the matrix multiplication approach can provide the variance and covariance information for each parameter, the following drawbacks limit its usage in hierarchical variance analysis for analog circuits.

- The covariance matrices only provide lumped information about the correlation between variables. It is hard to determine the contribution in variance for each lower level variable with respect to the top level variances. However, variation analysis in analog circuits requires the auxiliary information to help determine which critical sub-circuits to focus on during design iterations.
- The covariance matrix approach lacks the flexibility to trade off the computational complexity and the accuracy. As the number of variables in each level increases, time complexity becomes the major concern in variance analysis.
- In the covariance matrix based approach, each time the hierarchical construct is changed, all the affected values need to be recomputed. This need for the complete recomputation arises from the inability to destruct the components of the variance of each parameter. During the design iterations, an analog circuit is modified multiple times and the resulting hierarchical construct can be slightly different from the previous one. It is desired to save some computational effort on the unchanged part of the hierarchical construct.

In order to overcome these challenges, we propose a hierarchical approach where structural information on the circuit is tracked to enable information re-use during design iterations. In our earlier work [10], we have derived expressions for computing the variances of parameters at each hierarchical level of the circuit:

$$\sigma^2_{P_{j^{(i)}}} = \sum_k (S^{P_{j^{(i)}}}_{P_{k^{(i-1)}}})^2 \sigma^2_{P_{k^{(i-1)}}} + \sum_{i^{(0)}}^{r^{(0)}} \sum_{i^{(1)},j^{(1)}}^{r^{(1)}} \cdots \sum_{i^{(n-2)},j^{(n-2)}}^{r^{(n-2)}} \cdot \sum_{\substack{i^{(n-1)} \\ \neq j^{(n-1)}}}^{r^{(n-1)}} \left(S^{P_{i^{(n)}}}_{P_{i^{(n-1)}}} ... S^{P_{i^{(1)}}}_{P_{i^{(0)}}} \right) \left(S^{P_{i^{(n)}}}_{P_{j^{(n-1)}}} ... S^{P_{j^{(1)}}}_{P_{i^{(0)}}} \right) \sigma^2_{P_{i^{(0)}}} \quad (1)$$

where,

$$S^{P_{j^{(k)}}}_{P_{j^{(k-1)}}} = \left. \frac{\partial P_{j^{(k)}}}{\partial P_{j^{(k-1)}}} \right|_{\left(\mu_{P_{1^{(k-1)}}}, \mu_{P_{2^{(k-1)}}}, ..., \mu_{P_{r^{(k-1)}}} \right)}$$

represents the first order sensitivity of a Level-k parameter $P_{i^{(k)}}$ to a Level-$(k-1)$ parameter $P_{i^{(k-1)}}$. Section 4 presents a detailed discussion of this mathematical expression. In this work, we concentrate on a graph based interpretation and an efficient implementation of this processing scheme. We use a tree model for the hierarchical structure of the circuit. We focus on a layered variance analysis in which tracing to lower levels is avoided if the necessary information has been processed previously.

3. Modelling the Circuit Behavior and Parameter Correlations

Top-down design flow in analog circuits allows for a well-structured hierarchical representation of the circuit behavior. In our circuit model (illustrated in Figure 1), the lowest level of the hierarchy consists of process (e.g. the oxide thickness, the dopant concentration) and layout (e.g. the transistor width, the transistor length) parameters. The next

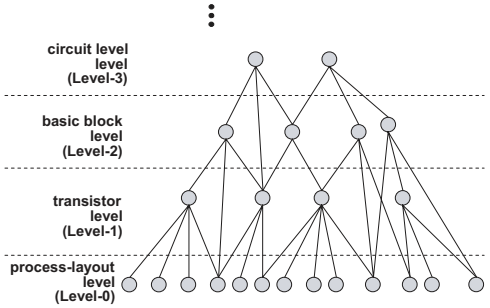


Figure 1: Hierarchical graph model of the circuit behavior

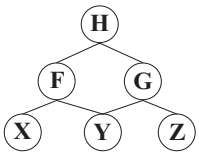


Figure 2: Correlated intermediate variables can be identified through functional dependency on Level-0 parameters

level of hierarchy consists of DC parameters such as the bias current, followed by small signal parameters, such as the transconductance and the output resistance. The nodes in the circuit graph in Figure 1 correspond to the parameters. An edge between two nodes indicates a functional dependency. The weight of that edge is assigned as the sensitivity between the two parameters. We call these weights *correlation coefficients*.

For the relations between process and layout parameters (Level-0 parameters) and DC parameters (Level-1 parameters), we use the SPICE circuit simulator and perturbation-based sensitivity computation. For the relations among the parameters at higher levels of hierarchy, we use analytical models. Such analytical models have been derived and used by circuit and system designers [13, 8], and extensively in analog design automation [3, 2].

Once the hierarchical circuit model is constructed, the variances of parameters at levels above Level-0 need to be computed. At a first glance, this computation step involves nothing more than computing the variance of a response function using the variances of its input parameters. However, as the parameters at intermediate hierarchical nodes are correlated, simple statistical analysis is not sufficient for accurate computation.

3.1. Adjacent level correlations

In this work, we process the correlation between two same-level parameters through their dependency on lower-level parameters. This dependency is determined using the hierarchical structure of the circuit representation and the correlation coefficients. A correlation between two Level-i parameters exists if they have functional dependency on at least one common lower level parameter.

As an example, consider the hierarchy in Figure 2. The correlation between F and G is due to their dependence on the Level-0 parameter, Y. Thus, for two parameters to be correlated, there has to be a path from both of them to at least one common Level-0 parameter. In prior work, correlations among intermediate parameters are handled using covariances that are either obtained through simulations [5] or assumed given [11]. (Simulation-based derivation of covariance is primarily limited to 3 levels of hierarchy.) In this work, we aim at efficient processing of these correlations using the circuit representation.

4. Layered Processing of Variances

The variance of Level-1 parameters can easily be computed using the sensitivity information since there is no correlation among Level-0 parameters. However, for the parameters at Level-2 and above, correlations need to be taken into account. Without loss of generality, consider a partial circuit graph given in Figure 3. Parameter $P_{i(j)}$ at Level-i can only be processed after processing of all parameters at Level-$(i-1)$ that $P_{i(j)}$ has functional dependence on. The processing of parameter $P_{i(j)}$ involves the following steps:

- Calculation of the variance based only on the variances of parameters at Level-$(i-1)$ on which $P_{i(j)}$ has functional dependency. This step corresponds to the first term in Equation 1 and only involves the parameters one level down in the hierarchy. For parameters at Level-2 and above, correlations need to be taken into account.
- Calculation of the *correlation correction term* (CCT) for the variance of $P_{i(j)}$. This step corresponds to the remaining term in Equation 1 and involves all parameters at Level-$(i-1)$ and all the parameters at Level-0 that cause the correlation. Although straightforward as a mathematical expression, direct implementation of this step can be time-consuming since the circuit graph needs to be traversed through Level-0 multiple times for each parameter being processed.

4.1. Loop tracing for CCT calculation

In order to avoid processing of the same information multiple times, we aim at using the connectivity information in the circuit graph in a more efficient manner. Let us first make several definitions:
Definition: A path between two parameters at distinct levels of hierarchy constitutes a *correlation path*.
Definition: For a parameter at Level-i, all parameters at lower levels that can reached through two distinct paths constitute its *correlation parameters*.
Definition: Two distinct paths between a parameter at Level-i and one of its correlation parameter constitute a *correlation loop*.

Equation 1 indicates that for a parameter, $P_{i(j)}$, and each of its Level-0 correlation parameters, the correlation paths

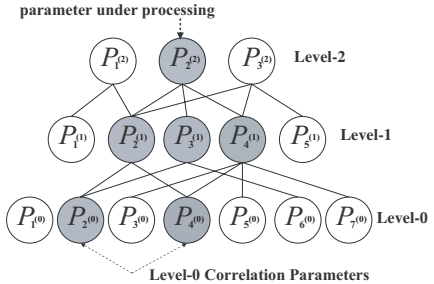


Figure 3: Determination of correlations and processing of variance information in a hierarchical manner

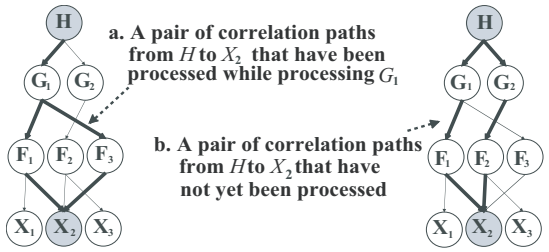


Figure 4: A partial circuit graph to process the CCT in the variance of H due to the correlation parameter X_2

need to be traced down to Level-0 in pairs. Equation 1 also requires that parameters at (Level-$(i-1)$) in these path pairs be distinct. The reason for this condition is illustrated in a partial circuit graph shown in Figure 4. There exist more than one correlation paths between the parameter under processing, H, and the Level-0 parameter, X_2, making X_2 a Level-0 correlation parameter for H. As Equation 1 suggests, the correlation paths need to be processed in pairs. The pair of correlation paths shown in Figure 4a have already been processed while processing the parameter, G_1, thus should be omitted. However, the correlation paths shown in Figure 4b have never been processed, thus should be included in the analysis.

The correlation paths shown in Figure 4a clearly include a loop excluding the parameter under processing (H). We call such loops convergent loops. The paths in Figure 4b demonstrate a non-convergent loop. Thus, the implementation of Equation 1 on the circuit graph suggests identification and processing of non-convergent loops (correlation loops) in the circuit graph.

4.2. Correlation through an arbitrary level

Correlation loops need not always go through Level-0 parameters. While one can still use Equation 1 and the aforementioned loop-based technique, it is advantageous in terms of computational efficiency to use the information at higher levels of the hierarchy. In order to achieve this goal, one can re-write the CCT term in Equation 1 by introducing the variances of the intermediate level parameters:

$$CCT = \sum_{i^{(n-2)}=1}^{r^{(n-2)}} W_{P_{i^{(n-2)}}}^{P_{i^{(n)}}} \sigma^2_{P_{i^{(n-2)}}} + \cdots + \sum_{i^{(0)}=1}^{r^{(0)}} W_{P_{i^{(0)}}}^{P_{i^{(n)}}} \sigma^2_{P_{i^{(0)}}} \quad (2)$$

where

$$W_{P_{i^{(k)}}}^{P_{i^{(n)}}} = \sum_{i^{(k)}=1}^{r^{(k)}} \cdots \sum_{\substack{i^{(n-1)}=1 \\ \neq j^{(n-1)}=1}}^{r^{(n-1)}} \left(S_{P_{i^{(n-1)}}}^{P_{i^{(n)}}} \cdots S_{P_{i^{(k)}}}^{P_{i^{(k+1)}}} \right) \left(S_{P_{j^{(n-1)}}}^{P_{i^{(n)}}} \cdots S_{P_{i^{(k)}}}^{P_{j^{(k+1)}}} \right)$$

is defined as *remainder correlation weight* between a Level-i parameter $P_{i^{(n)}}$ and a Level-k ($k \leq i-2$) parameter $P_{i^{(k)}}$. It is called *remainder* since the complementary part of the correlation coefficients has already been taken into account.

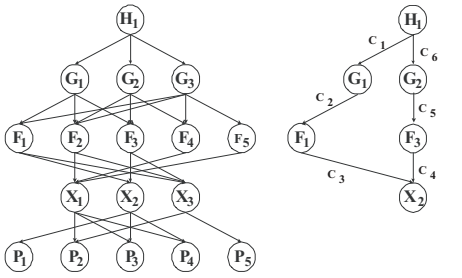


Figure 5: A four-layer hierarchical structure

Equation 2 suggests that a correction loop may exist between the parameter under processing and another parameter at an arbitrary level of hierarchy. Such loops need to be handled in the same way loops through Level-0 are handled. For example, in a five-layer hierarchical structure as shown in Figure 5a, the *remainder correlation weight* $r_{X_2}^{H_1}$ corresponds to the correlation loop through H_1 and X_2, as show in Figure 5b. In this case, the remainder correlation weight relating H_1 and X_2 will be $r_{X_2}^{H_1} = C_1 \cdot C_2 \cdot C_3 \cdot C_4 \cdot C_5 \cdot C_6$.

To calculate a *remainder correlation weight*, one needs to identify the loops in the partial tree corresponding to the *remainder correlation weight* and sum up the corresponding products of *correlation coefficients* along the loops.

4.3. Data structure and implementation issues

For VLSI systems with many hierarchical layers, it is likely that the connectivity information will be sparse, since independent variables at one corner of the die are not likely to affect parameters on another corner of the die. Moreover, in the computation of the correction terms, the connectivity information is processed many times. Thus, an efficient data structure for the representation of the connectivity information is a bi-directional tree structure where each node may have multiple children and multiple parents.

The partial circuit graph between a parameter under processing and one of its correlation parameters resembles a directed control flow graph in the sense that it has a single start and a single end point. Identification of loops in control flow graphs is a well investigated topic in compiler research. In [12], the loop identification is conducted in almost $O(k)$ time, where k is the number of edges in the control graph (the worst case time complexity is $O(k^2)$).

The correlation path information provides valuable insight during design iterations. First, the correlation paths provide a means for determining the relative contribution of each sub-circuit. Second, unmodified correlation paths need not be processed during design iterations. Third, for large circuits, we can compare the relative importance of the sensitivity paths and only retain a set of important sensitivity paths at each hierarchical level.

Although the storage of these sensitivity paths may lead to space overhead, the overhead is actually quite small in

practice since, for each path, we only need to record the index of the variables the path visits at each level. Also, dynamic programming techniques can be utilized when propagating these paths in a bottom-up manner along the hierarchical construct.

5. Comparison of computation time and accuracy with prior approaches

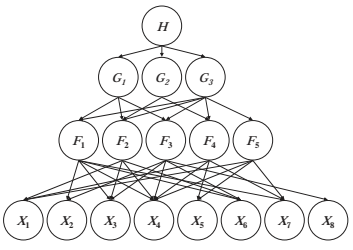
Two experiments have been conducted to evaluate the computational time and accuracy of the proposed hierarchical analysis approach. In this section, we provide comparisons with the Monte Carlo analysis, Taguchi's method, the min-max method, and the covariance based method given in [11].

Example 1: A four-layer non-linear hierarchy

Figure 6 shows an illustrative four-layer hierarchical construct with non-linear functional relationships between two adjacent layers. To evaluate the computational time and accuracy of the proposed method, means and variances of all the variables in the hierarchical construct are calculated using both the proposed method and various widely used statistical analysis approaches: the Monte Carlo analysis with both a large sample size and a small sample size, Taguchi's method, sensitivity-based min-max analysis, and covariance based analysis. (Covariance is assumed to be user given in [5], and is assumed to be based on a constant correlation of 0.3 between each pair of intermediate layer variables in [11]. To enable comparison, the same 0.3 correlation based analysis is used.) In the proposed method, the correlation coefficients are modelled with the first order Taylor series approximations around the nominal. The standard deviation of Level-0 parameters is given as 3.3%.

The computational time, the accuracy for the Level-3 parameter, H, and the accuracy for the Level-2 parameters (G_1 - G_3) have been summarized in Table 1. The 50K-sample Monte Carlo (MC) method is chosen as the base case for all accuracy comparisons.

The poor accuracy of the min-max and covariance-based approaches in conducting the hierarchical analysis for analog circuits limits their usage even though they can be done with relatively small computational efforts. These results



$F_1 = X_7X_2 + X_2^2 + X_2X_3\frac{X_6}{X_4}$
$F_2 = X_1^2 + X_3X_6 + X_4^2$
$G_1 = F_1F_2 + F_3^2$
$F_3 = X_2X_6 + X_3X_4 + X_8^2$
$G_2 = F_2^2 + F_4^2$
$F_4 = X_1X_8 + X_4^2 + X_5X_7$
$G_3 = F_4F_5 + F_2F_3 + X_1^2$
$F_5 = X_1^2 + X_7^2 + X_4^2/X_5$
$H = G_1^2 + G_2G_3$

Figure 6: A system of hierarchy with non-linear functional relations between two adjacent layers

confirm that the covariance-based approaches developed for digital timing analysis [11, 5] may not be easily extended to analog circuits where correlations may substantially vary between each pair of intermediate level parameters. Assuming a fixed correlation for all intermediate parameter pairs is effective in timing analysis since propagation delay is the only parameter and delays through various gates will have similar correlations as they consist of the same (or similar) transistor combinations. In the analog and mixed-signal circuits, however, this condition does not hold any more, thus a constant correlation modelling approach results in much higher errors.

Example 2: A differential amplifier circuit

Figure 7 shows a current mirror load MOS differential amplifier circuit that consists of 3 NMOS and 2 PMOS transistors. The corresponding hierarchical construct is shown in Figure 8, where Av corresponds to the low frequency gain. In this example, six process variables ($W, L, V_{to}, U_o, \lambda, T_{ox}$) for each of the five transistors are chosen as independent Level-0 parameters with given variances. Level-1 parameters consist of DC parameters (I_D,V_{DS},V_{GS}). The small-signal model parameters (g_m, g_o) constitute the set of Level-2 parameters, since they are usually expressed as functions of DC parameters. The top level (Level-3) of the hierarchy consists of the performance parameters of the circuit, such as gain (A_v) and cut-off frequency (f_c). In this experiment, only the variance of the gain is investigated. The variances of other performance parameters can be obtained in the same manner. As in the previous example, correlation coefficients between Level-1 and higher level parameters are derived using first order Taylor Series approximations around the nominal. Unlike the previous example, the correlation coefficients between Level-0 and Level-1 are obtained through a perturbation based approach. The standard deviation of Level-0 parameters is assumed to be 0.67%.

The goals of this experiment are (a) to evaluate the impact of approximate modelling (1st order approximation in this case) on more complicated functional relations, (b) to compare the proposed method to other state-of-the-art approaches for a practical circuit, (c) to illustrate the possibil-

Parameter / Method	G_1 $\%\epsilon$	G_2 $\%\epsilon$	G_3 $\%\epsilon$	H $\%\epsilon$	Time s
MC-50K	-	-	-	-	2.5×10^3
MC-1K	0.9	3.5	0.1	0.5	46.5
Taguchi's	0.4	4.6	0.4	0.1	328.3
Min-max	22.4	3.9	1.4	39.6	0.5
Covariance	11.0	9.6	1.3	21.6	0.8
Proposed	0.8	0.2	1.3	0.6	0.8

Table 1: Comparison for the accuracy of variance computation. Monte Carlo analysis with 50K samples is taken as the base. Taguchi's method requires 3^8 (6561) samples.

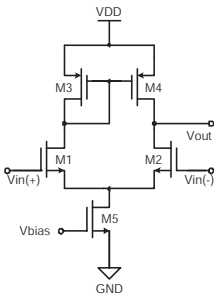


Figure 7: A differential amplifier circuit

ity of combining the analytical derivation and the perturbation based computation of correlation coefficients.

Table 2 shows the accuracy and computation time comparison for the parameters at Level-1 and above for various approaches. A 12K-sample Monte Carlo simulation is taken as the base case for all comparisons. Taguchi's method is excluded from the experiment as the required sample size (3^{30}) prohibits its use in this circuit with 30 Level-0 parameters. While tracking the results of the Monte Carlo simulation within 10% error, the proposed method only takes a fraction of computation time required by it. On the other end of the spectrum, the proposed analysis is highly accurate compared to the min-max or covariance approaches with only a small increase in computation time. Thus, even though the functions governing the relations between variables in adjacent layers are much more complicated compared to the first example, a similar conclusion can be drawn from this example. The proposed method provides both computational efficiency and accuracy.

6. Conclusion

In this paper, we present a hierarchical method to analyze the impact of process variations on circuit parameters. We model the hierarchical structure of the circuit as a tree wherein relations among circuit parameters are modelled as weighted edges. We start from Level-1 parameters and process each parameter at higher levels. Through identification of correlation loops, we avoid reprocessing of the same information to save time. The information reuse is particularly important during design iterations. In order to enable such reuse, we keep track of the correlation paths in the system and process only the updated information.

Two experimental cases have been used to evaluate the efficiency of the proposed approach: a highly non-linear hierarchy of random functions, and a 5-transistor differential amplifier circuit. The results indicate that the proposed analysis provides almost the same computational efficiency as the simple min-max approach, and fixed-covariance based approach while providing much higher accuracy (9% for the proposed approach for the top-level parameter compared to 1585% for the min-max analysis and 414% for the fixed covariance approach [11].).

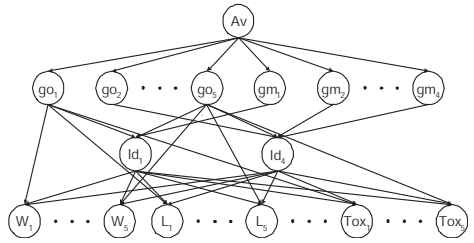


Figure 8: Hierarchical graph for the differential amplifier

σ	MC-12K	Min-max	Covariance	Proposed
$\%\epsilon\ I_{D_1}$	-	681.1	-0.3	2.0
$\%\epsilon\ I_{D_4}$	-	698.9	-0.3	2.0
$\%\epsilon\ g_{m_1}$	-	1641.3	470.0	3.1
$\%\epsilon\ g_{m_2}$	-	1639.1	468.5	3.6
$\%\epsilon\ g_{m_3}$	-	1623.8	465.5	2.6
$\%\epsilon\ g_{m_4}$	-	1610.8	459.8	1.5
$\%\epsilon\ g_{o_1}$	-	695.8	6.9	2.3
$\%\epsilon\ g_{o_2}$	-	651.9	1.0	-3.4
$\%\epsilon\ g_{o_3}$	-	695.0	6.8	2.1
$\%\epsilon\ g_{o_4}$	-	625.2	-2.6	-6.7
$\%\epsilon\ g_{o_5}$	-	574.6	-7.1	3.0
$\%\epsilon\ A_v$	-	1585.4	414.3	9.4
Time(s)	5.0×10^4	1.7	1.7	2.4

Table 2: Results for Example 2. Monte Carlo analysis with 12K samples is taken as the base case.

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