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# Resizing Methodology for CMOS Analog Circuits

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## ABSTRACT

This paper proposes a CMOS resizing methodology for analog circuits during a technology migration. The scaling rules aim to be easy to apply and are based on the simplest MOS transistor model. The principle is to transpose one circuit topology from one technology to another, while keeping the main figures of merit, and the issue is to quickly calculate the new transistor dimensions. Furthermore, when the target technology has smaller minimum length, we expect to obtain a decrease of area. This methodology is applied to both linear and non-linear examples: an OTA and a ring oscillator. The results are compared on three CMOS processes whose minimum length is 0.8  $\mu\text{m}$ , 0.35  $\mu\text{m}$ , 0.25  $\mu\text{m}$ .

**Keywords:** Analog design reuse, resizing, CMOS technology

## 1. INTRODUCTION

Nowadays analog design flow is much less developed than digital counterpart. That's why analog design flow is a very important way to explore. The resizing of the design is an essential tool for the reuse of analog circuits.

The main goals of a resizing methodology are to keep performances of the original design but also to reduce area and power consumption during a technology migration.

In this work we define a CMOS resizing methodology for analog design reuse, especially during a technology migration.

The paper is organized as follows. First we summarize the state of art of the resizing. Then we explain our methodology. We apply it on two different circuits, linear ones: OTAs and non-linear ones: ring oscillators, with three CMOS processes.

## 2. STATE OF ART

### 2.1 Summary of the resizing works

Recently, several works have been proposed in the reuse of analog blocks, and including resizing. The work of C. Galup-Montoro and M.C. Schneider [1], [2] proposed an analytical approach of MOS transistor resizing and several strategies depending on the type of the original circuit. In this work, the used model of MOS transistor is the ACM model [3] and application circuits are OTAs.

This method was extended in [4], adding experimental results from a complete Miller OTA, and including additional performance aspects of analog circuits. And it was also extended in [5], [6], using a tuning procedure based on optimization loop.

The main drawback of these works is the increase of chip area in the OTA examples.

Some EDA companies [7] have recently started to offer tools and services aimed at reuse and technology migration. [7] and [8] based their approaches on an optimization loop and intensive SPICE simulations in order to check and suitably modify circuit parameters to obtain the specified performances.

All of those works validated their results with an application on one OTA. That's why, for a better comparison, our example for the linear application is an OTA which has nearly the same performances than the one used in the other works.

### 2.2 Methodology of C. Galup-Montoro and M.C. Schneider [1]

The methodology of C. Galup-Montoro and M.C. Schneider is based on resizing rules from the ACM (Advanced Compact Model) transistor model. This model is based on the EKV [9] model but it doesn't take in account the

interpolation equations for linking the weak and strong inversion mode. Equations of NMOS transistor in saturation mode in the ACM model are given by:

$$I_D = I_S i_f \quad (1)$$

Where  $I_D$  is the drain current,  $I_S$  is the saturation current and  $i_f$  is a normalized current associated with the level of inversion at the source of ht transistor that verifies (3).

$$I_S = \frac{\mu_n n C_{ox} W U_T^2}{2L} \quad (2)$$

Where  $C_{ox}$  the oxide capacitance,  $U_T$  the thermal potential,  $W$  the width of transistor,  $L$  the length of transistor,  $\mu_n$  the mobility,  $n$  the slope factor.

$$\frac{(V_G - V_{T0}) - V_S}{n} = U_T (\sqrt{1+i_f} - 2 + \ln(\sqrt{1+i_f} - 1)) \quad (3)$$

Where  $V_G$  and  $V_S$  are the gate and source voltages,  $V_{T0}$  the threshold voltage.

From (1), (2) and (3), the gate transconductance  $g_m$  to drain current ratio is given by:

$$\frac{g_m}{I_D} = \frac{1}{n U_T} \frac{2}{(\sqrt{1+i_f} + 1)} \quad (4)$$

From these equations, the redesign rules are obtained. For a migration from a technology 1 to a technology 2, some scaling factors are defined:

$$\begin{aligned} V_{DD2} &= V_{DD1}/G_V & C_{OX2} &= C_{OX1} \cdot G_{COX} \\ L_{MIN2} &= L_{MIN1}/G_L & V_{E1} &= V_{E2} \cdot G_E \\ \mu_2 &= \mu_1/G_\mu \end{aligned}$$

Where  $V_{DD}$  is the supply voltage,  $L_{MIN}$  is the minimum transistor length of the technology and  $V_E$  is the Early voltage.

The scaling factors are determined for keeping the stage gain-bandwidth product, the maximum signal to noise ratio and the transistor's transition frequency.

Two scaling strategies are analyzed: the channel length scaling ( $L_2 = G_L \cdot L_1$ ) and the constant inversion level scaling ( $i_{f2} = i_{f1}$ ).

Table. 1. Resizing rules of the two strategies

Parameters	Constant inversion level scaling	Channel length scaling	
		WI	SI
L	$G_\mu^{-0.5}$	$G_L^{-1}$	
W	$G_v^2 G_{ox}^{-1} G_\mu^{-0.5}$	$G_v^2 G_{ox}^{-1} G_L$	
		WI	SI
$I_D$	$G_v^2$	$G_v^2$	$G_\mu G_v^2 G_L^{-2}$
$i_f$	1	$G_\mu G_L^{-2}$	$G_\mu^2 G_L^{-4}$
Gain DC	$G_E$	$G_E G_L^{-1}$	$G_E G_L G_\mu^{-1}$
Surface		$G_v^2 G_{ox}^{-1}$	$G_v^2 G_{ox}^{-1}$
Consumption		$G_v$	$G_\mu G_L^{-2} G_v$

Where  $\sqrt{1+i_{f2}} - 1 = \frac{G_{\mu}}{G_L^2}(\sqrt{1+i_{f1}} - 1)$ , WI is the weak inversion and SI the strong inversion.

From this methodology, an OTA is resizing from a technology 3  $\mu\text{m}$  to a 1.2  $\mu\text{m}$  and 0.35  $\mu\text{m}$ . Results from simulations validate it but we can notice some drawbacks. First the results are only from simulations, and for some technologies with small minimal length, the figures of merit are not keeping during the migration technology. And finally, the most important drawback is the increase of the chip area during a decrease of supply voltage. Indeed if  $G_v^2 G_{ox}^{-1} > 1$ , the area will be bigger than the original area.

### 2.3 Work of Acosta, Silveira and Aguirre [4]

This work is based on the previous methodology, and it tries to extend it. This work adds some performance parameters not covered in [1]. The idea is to study the behaviour of the slew rate of a common source MOSFET and the pole frequency of a current mirror. Considering the scaling rules, it is possible to predict the values of these performances.

The redesign of a micropower Miller OTA was calculated, simulated and experimentally tested on silicon from the technology 2.4  $\mu\text{m}$  to 0.8  $\mu\text{m}$  and 0.35  $\mu\text{m}$ . The results experimentally support the validity of this redesign technique. Concerning the Slew Rate, results prove that it decreases and this does not really agree with what we expect in terms of performance. Regarding the current mirror frequency response, this methodology keeps this figure of merit.

To conclude this work, a possible add of a tuning procedure could reduce some drawbacks (area and decrease of some figures of merit) of the original methodology.

### 2.4 Work of Savio, Colalongo and Kovacs-Vajna [5][6]

This methodology is also based on [1]. The main goal of this work is to add a tuning procedure to the original methodology. Indeed, the work [1] is only validated with a few technologies, the parasitic effects are not taking on account, and for several applications the DC gain voltage is not preserved during the technology migration.

Then a tuning procedure based on an optimization loop and intensive SPICE simulations could suitably modify circuit parameters to obtain the specified performances. An OTA is resizing and its DC gain voltage decreases, but with this procedure, the gain is keeping.

To conclude, this methodology improves the original one because the DC gain is preserved and the power consumption decreases. However the area drawback of [1] is still here and during a technology migration, we expect to decrease the area when the target technology has a smaller minimum length than the original one. Then this issue has to be developed to reduce the chip area.

## 3. DESCRIPTION OF THE PROPOSED METHODOLOGY

### 3.1 Principle of the methodology

The proposed resizing guidelines could be summarized in three steps:

Step 1: Definition of the figure(s) of merit to be preserved

Step 2: Calculation of the technological scaling factors

Step 3: Decision on some strategic aspects and computation of the new transistor sizes

The last computation step relies on MOS transistor model equations. In the present work, the Level 1 MOS transistor model is carried out and gives correct estimations. Naturally, it is possible to use more accurate equations like those of BSIM3V3 to determine the scaling rules and then the new sizes of transistors.

### 3.2 Definition of the scaling factors [10]

The scaling factors are defined in Table 1, considering a migration from a technology 1 to a technology 2.

The first three factors are calculated from known technological parameters (Step 2).

The goal is to evaluate the factors  $K_L$  and  $K_W$ .

Table. 2. Definition of the scaling factors

Parameters	Scaling factors
Supply voltage : $V_{DD}$	$K_V = V_{DD2} / V_{DD1}$
Oxide capacitance : $C_{OX}$	$K_{OX} = C_{OX2} / C_{OX1}$
Mobility : $\mu_0$	$K_\mu = \mu_{02} / \mu_{01}$
Effective gate voltage : $V_{EG} = V_{GS} - V_T$	$K_{EG} = V_{EG2} / V_{EG1}$
Bias current : $I_{bias}$	$K_I = I_{bias2} / I_{bias1}$
Length of the transistor : $L$	$K_L = L_2 / L_1$
Width of the transistor : $W$	$K_W = W_2 / W_1$

We notice that the scaling factors' values are depending on the type of transistors (NMOS or PMOS).

### 3.3 Focus on the third step of the methodology

The third step of the methodology is the most important. Indeed, we choose the strategy of redesign and then to choose the equations which will be used to determine the scaling factors. This choice of the strategy is wondering by the designer and depending on the goals and the system specifications, a strategy is emerging.

Here are the main equations, derived from Level 1 MOS transistor model, which are carried out in the next paragraphs:

-the drain current in the saturation region

$$I_D = \frac{\mu_0 C_{ox} W}{2L} V_{EG}^2 \quad (5)$$

-the average drain-to-source resistance [11], [12]

$$R_N = \frac{V_{DD}}{\frac{\mu_{0N} C_{OXN} W}{2} \frac{V_{DD} - V_{TN}}{L}} \quad (6)$$

$$R_P = \frac{V_{DD}}{\frac{\mu_{0P} C_{OXP} W}{2} \frac{V_{DD} + V_{TP}}{L}} \quad (7)$$

Those equations are an estimate for the resistance between the drain and source of the MOSFET during switching.

-the simplified gate capacitance

$$C_G \approx W L C_{OX} \quad (8)$$

Those equations have been chosen for the application examples.

### 3.4 Limits and Extension of the methodology

This methodology has some limits because for the lowest technologies which have a small minimum length, the parasitic effects are not included and then a variation of performance could be existed. Then to solve this problem, there are two solutions.

First, this methodology could be extent. Indeed the results given by the methodology could be a base of an optimization loop which has a better performance. In this work, the optimization function of Cadence environment gives a better result for the lowest technologies and then could reduce the variation of performance due to the parasitic effects. This

tool by iteration gives an optimization of the performances based on variables. Then with the calculated sizes of the transistors, we improve the results with a variation of the length and width of each component.

Secondly, the model of transistor could be more relevant. Using accurate equations like the BSIM3V3 model, in this methodology will give better results and performances. The only difference will be the complexity of the determination of the scaling factors.

#### 4. APPLICATION ON LINEAR EXAMPLES

Applications of these guidelines are proposed on linear and non-linear applications: an OTA where all the transistors are in saturation mode and a non-linear application: a ring oscillator, for a technology migration from CMOS 0.8  $\mu\text{m}$  to CMOS 0.35  $\mu\text{m}$ , and to CMOS 0.25  $\mu\text{m}$ .

##### 4.1 Application on an OTA

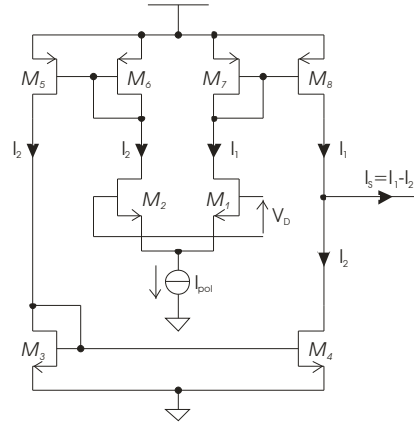


Fig. 1. Topology of the OTA

The original circuit has been designed in CMOS 0.8  $\mu\text{m}$  technology with a supply voltage of 5 V and first scaled in CMOS 0.35  $\mu\text{m}$  technology with a 3.3 V supply voltage, then in 0.25  $\mu\text{m}$  technology with a 2.5 V supply voltage. In this OTA, all the transistors are in saturation mode.

##### 4.2 conservation of the transconductance gain and reduction of the power consumption

Step 1: the figures of merit to be kept are the transconductance OTA gain and to reduce cost by decreasing the power consumption.

Step 2:  $K_V$ ,  $K_{OX}$ ,  $K_\mu$  are deduced from technological information.

Step 3: We want to conserve the transconductance OTA gain  $g_m$ . To reduce the power consumption, we choose to reduce the bias current.

For instance, by multiplied the transistors width (W) and the length L by a K factor and divided the biasing current by the same factor, the power consumption of the design decreases and keeps the same performances.

$$I_{D2} = K_I I_{D1} \quad (9)$$

$$\frac{\mu_{01} C_{OX1} W_1}{2L_1} V_{EG1}^2 = K_I \frac{\mu_{02} C_{OX2} W_2}{2L_2} V_{EG2}^2 \quad (10)$$

$$K_I^2 = \frac{K_\mu K_{ox} K_{EG}^2 K_W}{K_L} \quad (11)$$

$$K_L = \frac{L_{MIN2}}{K_I L_{MIN1}} \quad (12)$$

$$K_W = \frac{K_L}{K_I K_\mu K_{ox} K_{EG}^2} \quad (13)$$

The results of this methodology are given by the figure 2 and table 4.

Table. 3. Sizes of the transistors

Transistors	0.8 $\mu\text{m}$	0.35 $\mu\text{m}$	0.25 $\mu\text{m}$
W/L	5 V	3.3 V	2.5 V
M <sub>1</sub> ( $\mu\text{m}$ )	10/2	9.85/1.3	5.6/0.85
M <sub>2</sub> ( $\mu\text{m}$ )	10/2	9.85/1.3	5.6/0.85
M <sub>3</sub> ( $\mu\text{m}$ )	10/2	9.85/1.3	5.6/0.85
M <sub>4</sub> ( $\mu\text{m}$ )	10/2	9.85/1.3	5.6/0.85
M <sub>5</sub> ( $\mu\text{m}$ )	10/2	11.1/1.3	4.95/0.85
M <sub>6</sub> ( $\mu\text{m}$ )	10/2	11.1/1.3	4.95/0.85
M <sub>7</sub> ( $\mu\text{m}$ )	10/2	11.1/1.3	4.95/0.85
M <sub>8</sub> ( $\mu\text{m}$ )	10/2	11.1/1.3	4.95/0.85
I <sub>BIAS</sub>	45 $\mu\text{A}$	30 $\mu\text{A}$	20 $\mu\text{A}$

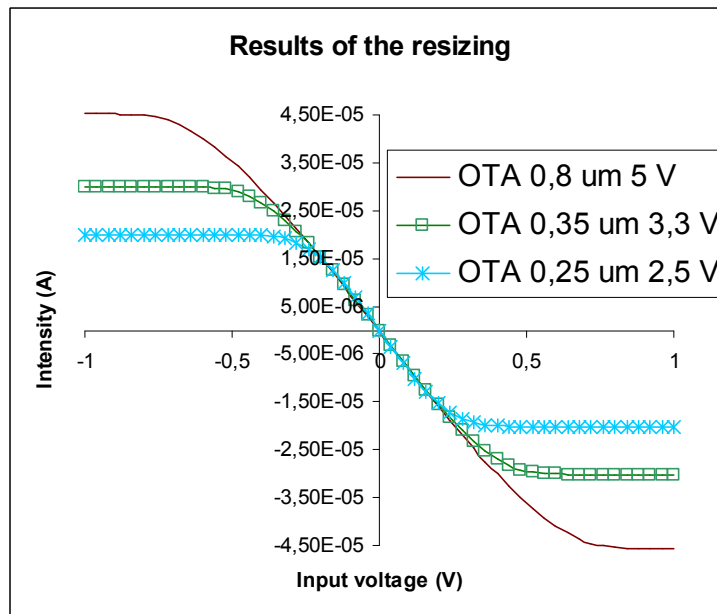


Fig. 2. DC transfert characteristic of the OTA

Figure 2 is obtained with using  $I_{D2} = K_I I_{D1}$  ( $K_I = 2/3$ ). Number n is chosen depends on the specifications we have and the goals that we want to reach.

Table. 4. Results of the simulations

Technology ( $\mu\text{m}$ )	0.8	0.35	0.25
Supply Voltage (V)	5	3.3	2.5
$G_0$ ( $\mu\text{A}\cdot\text{V}^{-1}$ )	78	80	81
Power Consumption ( $\mu\text{W}$ )	459	200	100
Area ( $\mu\text{m}^2$ )	160	109	36

The slope and the offset (figure 2) are conserved by this resizing methodology. The dynamic range is reduced but the consumption decreases of 56 % for the migration from 0.8  $\mu\text{m}$  to 0.35  $\mu\text{m}$ , and 50 % for the migration from 0.35  $\mu\text{m}$  to 0.25  $\mu\text{m}$  (Table 4). Simulation results describe that the methodology keeps the DC performance ( $G_0$ ), and reduces the cost with the decrease of area (32 % between 0.8  $\mu\text{m}$  and 0.35  $\mu\text{m}$ , and 67 % between 0.35  $\mu\text{m}$  and 0.25  $\mu\text{m}$ ).

## 5. APPLICATION ON NON-LINEAR EXAMPLES

For a non-linear application, the resizing methodology has been applied on a ring oscillator which is build with inverters. The CMOS inverter is a basic building block for circuit design.

### 5.1 The ring oscillator

A ring oscillator is built with an odd number of inverters which forms a closed loop with positive feedback. The inverters are identical.

The main characteristic of the ring oscillator is the oscillation frequency.

Step 1: the figure of merit to keep is the oscillation frequency. It is given by [12], [13].

$$f_{osc} = \frac{1}{2n(t_{PHL} + t_{PLH})} \quad (14)$$

Where  $t_{PHL} + t_{PLH} = (R_n + R_p)C_{tot}$

Step 2:  $K_V$ ,  $K_{OX}$ ,  $K_\mu$  are deduced from technological information.

Step 3: A simple way to conserve the oscillation frequency is to keep the same resistances and capacitances associated with the inverter.

### 5.2 MOS inverter

Fig. 3 describes the topology and the characteristics of the inverter.

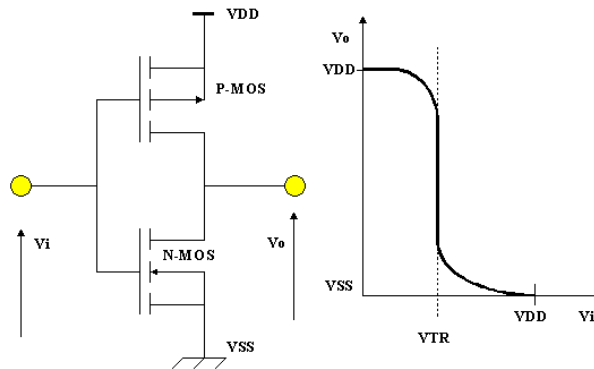


Fig. 3. The CMOS inverter transfer characteristics



We use minimum size CMOS inverters. It means that the widths and lengths of the two devices are taken as equal ( $W_p=W_n$  and  $L_p=L_n$ ).

### CMOS inverter capacitances:

The inverter input capacitance is given by

$$C_{IN} = C_{GN} + C_{GP} \approx (W_n L_n + W_p L_p) C_{OX} \quad (15)$$

Where the NMOS total capacitance is named  $C_{GN}$  and the PMOS one is named  $C_{GP}$ .

The input gate capacitance of the inverter is dominant over the output capacitance, then  $C_{IN} + C_{OUT} \approx C_{IN}$ . To conclude, the total capacitance with  $n$  inverters is equal to  $nC_{IN}$ .

$$C_{TOT} = n C_{IN} = n (W_n L_n C_{OXN} + W_p L_p C_{OXP}) \quad (16)$$

### CMOS inverter resistances:

The MOS drain-to-source resistance is given by (6) and (7).

### 5.3 Determination of scaling factors

As the resistances and the capacitances associated with the inverter have been kept, we determine the scaling factors of the length and the width.

#### Conservation of the total capacitance:

$$\text{NMOS: } W_{N2} L_{N2} C_{OXN2} = W_{N1} L_{N1} C_{OXN1} \quad (17)$$

$$\text{PMOS: } W_{P2} L_{P2} C_{OXP2} = W_{P1} L_{P1} C_{OXP1} \quad (18)$$

So with (17) and (18), the equation obtained is

$$W_2 L_2 = \frac{W_1 L_1}{K_{ox}} \quad (19)$$

#### Conservation of the resistances:

$R_{N2} = R_{N1}$  and  $R_{P2} = R_{P1}$  then

$$\frac{L_2}{W_2} = \frac{L_1}{W_1} \frac{K_{ox} K_{\mu}}{K_V} \frac{(V_{DD2} - V_{T2})^2}{(V_{DD1} - V_{T1})^2} \quad (20)$$

With (19) and (20) we obtain:

$$K_W K_L = \frac{1}{K_{ox}} \quad (21)$$

$$\frac{K_L}{K_W} = \frac{K_{ox} K_{\mu}}{K_V} \frac{(V_{DD2} - V_{T2})^2}{(V_{DD1} - V_{T1})^2} \quad (22)$$

Then the scaling factors are determined, the width factor is  $K_W$  and the length factor is  $K_L$ .

$$K_W = \frac{1}{K_{ox}} \sqrt{\frac{K_V}{K_{\mu}} \frac{(V_{DD1} - V_{T1})}{(V_{DD2} - V_{T2})}} \quad (23)$$

$$K_L = \sqrt{\frac{K_{\mu}}{K_V} \frac{(V_{DD2} - V_{T2})}{(V_{DD1} - V_{T1})}} \quad (24)$$

## 5.4 Simulations results

Three experiences have been made on some ring oscillators with different characteristics during a technology migration. Two applications are made on the same topology of ring oscillator but with different transistor's sizes. And one experience is on a ring oscillator with different number of inverters. The initial technology is CMOS 0.8  $\mu\text{m}$  and the target technology is CMOS 0.35  $\mu\text{m}$ , and CMOS 0.25  $\mu\text{m}$ .

All of these applications validate the methodology. We present here just the first application which is a ring oscillator with 5 inverters.

### Determination of the oscillation frequency:

From (6), (7), (17) and (18), we determine the theoretical oscillation frequency.

NMOS and PMOS initial sizes in technology 0.8  $\mu\text{m}$  with a supply voltage of 5 V are:

$$L_{IN} = L_{IP} = 2 \mu\text{m} \text{ and } W_{IN} = W_{IP} = 50 \mu\text{m}.$$

With using the scaling factors (23), (24), we determine the new transistor's sizes in technology 0.35  $\mu\text{m}$  and 0.25  $\mu\text{m}$  with different supply voltage.

Table. 5. New sizes of transistors

Size	0.35 $\mu\text{m}$ 5 V	0.35 $\mu\text{m}$ 3.3 V	0.25 $\mu\text{m}$ 2.5 V
$L_N$	1.95 $\mu\text{m}$	1.25 $\mu\text{m}$	1.00 $\mu\text{m}$
$L_P$	1.75 $\mu\text{m}$	1.40 $\mu\text{m}$	1.05 $\mu\text{m}$
$W_N$	47.85 $\mu\text{m}$	75.45 $\mu\text{m}$	34.10 $\mu\text{m}$
$W_P$	53.70 $\mu\text{m}$	64.30 $\mu\text{m}$	32.15 $\mu\text{m}$

The theoretical and experimental oscillation frequencies are given by Table 6. The theoretical values are determined by the scaling factors we define, and the experimental values are given by simulations.

Table. 6. Oscillation frequencies

$L_{MIN}$ ( $\mu\text{m}$ )	0.8	0.35	0.35	0.25
$V_{DD}$ (V)	5	5	3.3	2.5
$f_{osc}$ theo (MHz)	267	268	267	268
$f_{osc}$ exp (MHz)	267	268	266	270
Area ( $\mu\text{m}^2$ )	1000	936	930	339

We observe that the oscillation frequencies of the three ring oscillators are the same.

Simulation results (Table 6) describe that the methodology keeps the figure of merit we want to maintain (oscillation frequency).

## 6. CONCLUSION

The work presented here defines a resizing methodology for analog circuit design reuse. The goal is to obtain a scaled circuit with the same performances of the initial one and to reduce area. It was applied on a linear circuit (OTA) to compare with others resizing works and on a non-linear circuit (ring oscillator) to extend the methodology. The different topologies are designed in a 0.8  $\mu\text{m}$ , 5 V voltage supply standard CMOS technology and they were scaled to a 0.25  $\mu\text{m}$ , 2.5 V. This methodology decomposes the resizing process into three steps. This work clearly highlights which parameters are deduced from technological information and which ones are determined thanks to different strategic decisions.

Calculation and simulations were checked against the original design. The results of this technological migration support the success of this redesign technique: conservation of the performances and reduction of the area. The limits and the extension of this methodology are described.

## REFERENCES

1. C. Galup-Montoro, M.C. Schneider, "Resizing rules for the reuse of MOS analog design", Proceedings SBCCI 2000: XIII Symposium on Integrated Circuits and Systems Design, pp. 89-93, Manaus, Brésil, Septembre 2000.
2. C. Galup-Montoro, M.C. Schneider, R. Coitinho, "Resizing Rules for MOS Analog-Design Reuse", IEEE Design and Test of Computers, pp. 50-58, Mars-Avril 2002.
3. A. Cunha, M. Schneider, C. Galup-Montoro, "An MOS Transistor Model for Analog Circuit Design", IEEE Journal of Solid-State Circuits, Vol. 33, No 10, pp. 1510-1519, Octobre 1998.
4. R. Acosta, F. Silveira, P. Aguirre, "Experiences on Analog Circuit Technology Migration and Reuse", Proceedings SBCCI 2002 : XV Symposium on Integrated Circuits and Systems Design, pp. 169-174, Porto Alegre, Brésil, Septembre 2002.
5. A. Savio, L. Colalongo, Zs. M. Kovacs-Vajna, "Scaling rules and parameter tuning procedure for analog design reuse in technology migration", Proceedings IEEE ISCAS 2004 : International Symposium on Circuits and Systems, pp. 117-120, Vancouver, Canada, Mai 2004.
6. A. Savio, L. Colalongo, M. Quarantelli, Zs. M. Kovacs-Vajna, "Automatic scaling procedures for analog design reuse", IEEE Transactions on Circuits and Systems I: regular paper, Vol. 53 pp.2539-2547 December 2006.
7. <http://www.neolinear.com>
8. S. Funaba, A. Kitagawa, T. Tsukada, G. Yokomizo, "A Fast and Accurate Method of Redesigning Analog Subcircuits for Technology Scaling", Proceedings Analog Integrated Circuits and Signal, Vol. 25, pp. 299-307, 2000.
9. E. A. Vittoz, "Future of analog in the VLSI environment", Proceedings IEEE ISCAS 1990: International Symposium on Circuits and Systems, pp. 1372-1375, Genève, Suisse, Mai 2000.
10. T. Levi, N. Lewis, J. Tomas, P. Fouillat, "Scaling Rules for MOS analog design reuse", Proceedings IEEE MIXDES 06, pp. 378-382, Gdynia, Poland, Mai 2006.
11. T. DeMassa, Z. Ciccone, "Digital Integrated Circuits", John Wiley and Sons, 1996.
12. R. J. Baker, H. W. Li, D. E. Boyce, CMOS Circuit design, layout, and simulation, IEEE Press series on Microelectronic Systems, 1998.
13. A. S Sedra, K. C. Smith, Microelectronic Circuits Third Edition, International Edition, Saunders College Publishing, 1991.