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**IP-based design for analogue ASICs:
A case study**

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Abstract :

The design flow of Analog and Mixed Signal has to be improved. In a specific application, we propose a definition of the IP content and the structure of an IP-based library. The case study consists in an ASIC which imitates the electrical behaviour of a biological neuron.

1. Introduction

The main objective of this work is to improve the design flow of analogue and mixed signal integrated circuits. Purely digital systems profit from standardized tools and methods which allow automatic synthesis. In the analogue domain, automatic synthesis has probably no sense and efforts must be done towards developing consistent and coherent CAD (Computer Aided Design) methods and tools.

The main idea is to re-use the accumulated design knowledge which could be illustrated by the IP (Intellectual Property) concept. In this paper, we give our experience on the following aspects: content of an analogue IP, IP-based library and its integration in the system design flow, applied on a specific example.

2. Application domain

2.1 Microelectronics applied to neuroscience

Engineering of neuromorphic integrated systems is a research field where microelectronics encounters biology. The link between both is realized by computational neurosciences which model and emulate a part of brain activity. Different levels of modelling exist from the neuron physiology to the plasticity of large neurons networks. One issue is to have the adequate simulation system that implements those models;

that is the role of neuromorphic engineering [1], [2]. Important features of such systems are re-configurability, observability and also real-time running, especially for hybrid (real/artificial) experiments.

From the microelectronic point of view, one solution is to design analogue ASICs for the real-time computation of neurons activity and to digitally control the connectivity between these neurons. As it is often the case, the development of the analogue part requires the largest amount of time, due to the lack of formalism and automation in that domain.

2.2 Analogue ASICs description

The analogue ASICs integrate several biologically realistic neurons, following a mathematical model, known as Hodgkin-Huxley formalism [3]. This neuron model is close to the biology and is composed of non-linear conductances representing the ionic currents flowing through the neuron membrane. All model equations can be implemented using classical analogue building blocks like differential amplifiers, OTAs, current mirrors and current-mode multipliers. Indeed, an experience of about ten years and 19 designed ASICs [4] allow now to have an accurate idea of the system hierarchy and the recurrent analogue blocks, which is the basis of IP-based design.

Figure 1 illustrates the typical hierarchy of our analogue ASICs.

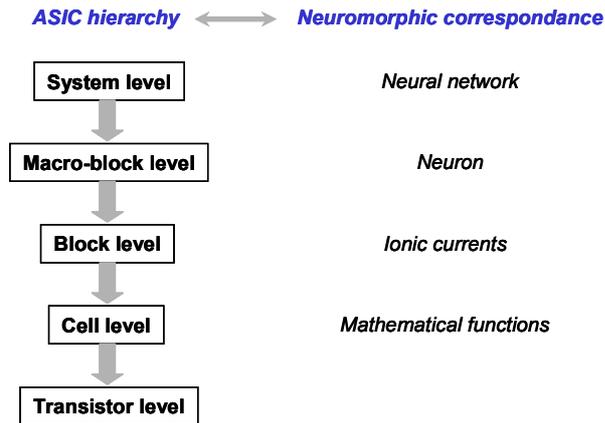


Figure 1: Typical ASIC hierarchy

At the beginning of the design process, the specifications are given by neuroscientists and biologists; they consist mainly in parameters controlling the *block level* but also in some data related to the network topology.

Due to the increasing complexity of networks to be implemented, it becomes crucial to maximize the re-using of previously designed blocks.

The following paragraphs will describe firstly what could be embedded in an analogue IP, then how these entities may be organised in a data-base and finally how to use this data-base in the ASIC design flow.

3. Analogue IP content

3.1 Analogue IP definition

Defining the IP content is the first important task because the IP concept is the base of design re-use. Some works already exist towards the re-use of AMS blocks [5] [6] [7].

What should be the main properties of an IP block? First, it should give a precise characterization of already designed block; second, it has to be described with adequate representations or models, consistent with the design levels, to enable the easy re-use of the block, along the complete design flow

Table 1 shows the different descriptions (or *views*) that are embedded in our IP blocks.

All these views have the same terminals and the same symbol.

Table 1: IP-AMS hierarchical description levels

View name	Description / Role
Symbol	visualizes the function
Connectical	verifies connexion between blocks (VerilogA)
Functional	models ideal electrical behaviour (VerilogA)

Behavioural	models non-ideal electrical behaviour, extracted from schematic (VerilogA)
Schematic	transistor-level schematic
Layout	
Characterization	See below ...

For the *connectical*, *functional* and *behavioural* views, we use verilogA language. These views are useful for multilevel simulations especially in the verification phase of the design process. The *functional* view describes the ideal equations of the function to be implemented. The *behavioural* view is more detailed indeed there are refined equations which fit the schematic behaviour.

One important point is to have a fluent and coherent design flow, that is why logical and mathematical links have been established between the different views.

The *characterization* view is the most important view for the research of the corresponding IP. This view is the main point of the re-use methodology. It contains information about the design and the re-use ability of the IP-block. The technology, the supply voltage, the terminals and their validity domains, the links between the functional model and the behavioural model, the area of the layout and the cost of the design (which may be calculated with the technology and the area) are defined in this file.

The validity domain gives the range of input signals, where the circuit functionality is conserved. This information comes from systematic simulation of the primitive *cells* (*cell level*); then it is propagated to the *blocks* and *macro-blocks*.

3.2 Example of IP: Sigmoid cell

The Sigmoid function is one of the basic functions implemented in our ASIC. Indeed in the biological model, there are some probability terms which can be modelled by this function.

- Biological equation to be implemented :

$$m_{\infty}(V_{mem}) = \frac{1}{1 + e^{\frac{-(V_{mem} - V_{offset})}{V_{slope}}}}$$

m_{∞} is the previously mentioned probability term. V_{offset} and V_{slope} are model parameters and V_{mem} represents the potential of the neuron membrane.

- Transformation to the electrical functional model:

Some conversion factors are added between the biological model and the electrical one. Indeed for the current, the voltage and the conductance we have to assure better signal dynamic performance for the robustness of the circuit. The two models use the same timing scale.

In the electrical functional model, m_{∞} is represented by a current, so the model equation becomes:

$$I_{act} = \frac{2I_{h_10u}}{1 + e^{\frac{-(V_{mem} - V_{offset_m})}{V_{slope_m}}}}$$

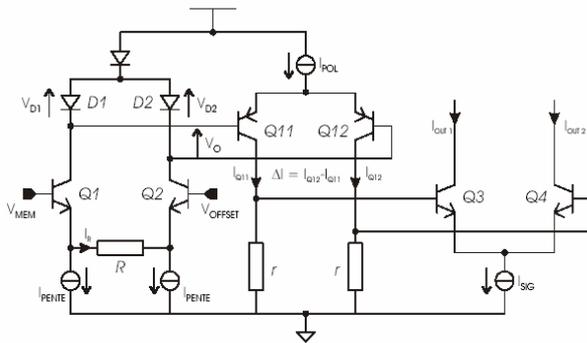


Figure 2: Schematic of the sigmoid cell

Symbol:

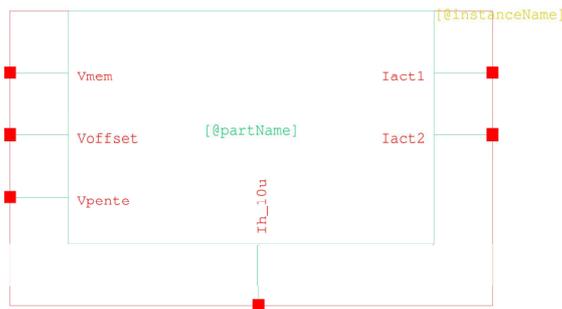


Figure 3: Symbol of the sigmoid cell

This component has six terminals. I_{h_10u} represents the bias current. V_{mem} , V_{offset} and V_{pente} are three voltage inputs for the differential pair. I_{act1} , I_{act2} are the two current outputs.

Characterization of the sigmoid cell:

Technology	BiCMOS AMS 0.35 μ m
Supply voltage	5 V
Inputs	V_{mem} , V_{offset_m} , V_{slope_m} , I_{h_10u}
Outputs	I_{act1} , I_{act2}

Validity domains:

Inputs	Minimum	Maximum
V_{mem}	7.5 mV	150 mV
V_{offset_m}	-900 mV	700 mV
V_{slope_m}	-2 V	2 V

Relation between the functional and the behavioural model:

For the behavioural model, the detailed analysis of the schematic gives a refined equation:

$$I_{act} = \frac{2 \cdot I_{h_10u}}{1 + e^{\frac{-10rR_{conv} \cdot I_{h_10u} \cdot (V_{mem} - V_{offset_m})}{R \cdot U_T \cdot (V_{cc} - V_{slope})}}$$

Layout's area: 8600 μ m²

4. Structure of the database

4.1 Data-base features

The data-base must implement:

- The hierarchy of the system
- The IPs and their content

For our application, the hierarchy is well established (Figure 1).

At the *cell level*, each IP corresponds to a specific mathematical function, which is a part of the biological neuron model, but several schematic implementations may be available for the same function.

4.2 Data-base implementation

The data-base is implemented with MySQL [8] formalism. Six tables have been created:

- one is for the link father-son between the different entities of the hierarchy
- one table defines each IP
- one table gives the number of IPs available for each function
- three other tables defines the set of model parameters for each hierarchical level (*Macro-block level*, *Block level* and *Cell level*).

4.3 Data-base exploration

The objective is to find one ASIC solution according to the initial specifications.

The chosen method is to perform a Top-Down exploration, from the *macro-block level* to the *cell level* using the validity domain as a selection criterium. If we have different corresponding IPs, we should choose the one with the largest validity's domain.

The exploration requests are made in Php [9]. These requests are created from the system specifications.

At the final step, a diagnostic is returned which quantifies the possibility to re-use IPs for a new ASIC project. In a case of re-use, IPs netlists are created for the designer.

5. Application example

5.1 Example description

As illustrated on Figure 4, the ASIC is composed of neurons which are defined by some ionic currents which are made by some elementary functions.

The ASIC represents the *system level*, a neuron the *macro-block level*, an ionic current the *block level* and an elementary function the *cell level*.

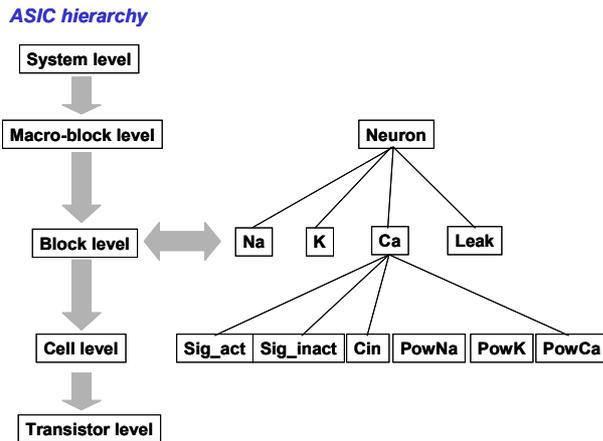


Figure 4: Hierarchy of the ASIC

Each cell contains some IPs which are defined previously.

5.2 Specifications

The system specifications are given by the neurobiologists. Then these specifications are converted in electrical ones. Finally, requests are created by these electrical specifications.

In this simple test example, the ASIC specifications are:

- Neuron 1: one neuron with 4 ionic currents (Na, K, Ca, Leak)
- Neuron 2: one neuron with 3 ionic currents (Na, K, Leak)

Figure 5 is a shoot screen of the software's interface which allows biologists to enter the specifications.

The parameters corresponding to the system specifications are summarized in Table 2.

Summary of the system specifications of Levi

You already have an account

You want to have 2 neurons in your network

Neuron 1

Cmem_bio in uF/cm2:

Area of neuron 1 in cm2:

Please choose your ionic currents

Sodium
 Potassium
 Leak
 Calcium
 5th ionic current

How many multysynapses for this neuron do you want?

Neuron 2

Cmem_bio in uF/cm2:

Area of neuron 2 in cm2:

Please choose your ionic currents

Sodium
 Potassium
 Leak
 Calcium
 5th ionic current

How many multysynapses for this neuron do you want?

[Come back to the initial system specifications](#)

Figure 5: System specifications

Table 2: Parameters of the system specifications

Currents	Voffset (mV)	Vslope (mV)	Tau (ms)	Vequi (mV)	gmax (S)
Neuron 1					
Na	-37	7.2	0.03	50	110 μ
K	-37	11.38	3	-100	22 μ
Ca	-35	11.4	8	-100	50 μ
Leak					220n
Neuron 2					
Na	-41	5.7	0.08	80	70 μ
K	-2	13.81	5	-120	13 μ
Leak					310n

From these specifications, requests are created and they explore the database using a Top-Down methodology.

We give an example of the exploration of the database and the requests created for the research.

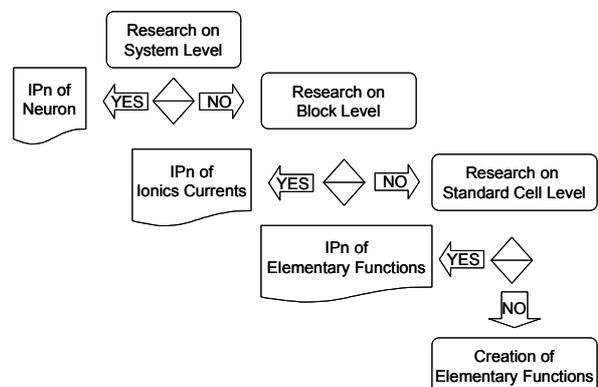


Figure 6: Top Down exploration

First we will look for an IP which corresponds to the specifications of the neuron (*Macro-block Level*), i.e. that its validity domains include the specified parameter values. If there is one, the research will be complete and positive. If not, we will look for a solution with several IPs at the lower level: ionic currents (*block level*). For example, the neuron N1 is composed of four ionic currents blocks which names are *Na*, *K*, *Ca* and *leak*. We will begin with the research of IPs corresponding to the Na ionic current, if it exists one then we will go to the next ionic current bloc, (*K*), etc.

At the lower level (*cell level*), if one request is negative, then the designer has to design a new IP-cell which will be further included in the database.

5.3 Results

The diagnostic of the request are given in Table 3. It describes the number of IPs we can re-use.

Table 3: Validation of the ionic currents

Ionic currents	Neuron 1	Neuron 2
Na	Right	Right
K	Wrong	Right
Ca	Right	
Leak	Right	Right

Table 4: Final diagnostic

Neurons	Numbers of IPs we can re-use	Percentage of re-use for this circuit
Neuron 1	49/63	78 %
Neuron 2	51/51	100 %

Table 3 describes an error in the re-use of the K ionic current. Indeed one parameter of the specifications ($V_{offset} = -2$ mV) is not included in each validity domain of K IPs. That's why we cannot find an IP for these specifications. So the designer has to build another IP which fits with the parameters.

6. Conclusion

In this paper, a case-study in analogue IP re-use is exposed. The questions that have been developed are: analogue IP definition, IP-based library and IP-based system design. The result is an automatic design space exploration, starting from the system specifications. This exploration allows to obtain a rapid estimation of the amount of re-usable circuits.

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