Thermal and Sensitivity Analysis of Multi-Fin Devices

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ABSTRACT

As device dimensions shrink into the nanometer range, power and performance constraints prohibit the longevity of traditional MOS devices in circuit design. A finFET, a quasi-planar double-gated device, has emerged as a replacement. FinFETs are formed by creating a silicon *fin* which protrudes out of the wafer, wrapping a gate around the fin, and then doping the ends of the fin to form the source and drain. Wider finFETs are formed using multiple fins between the source and drain regions.

While finFETs provide promising electrostatic characteristics, they, like other ultra-thin body nano devices, have the potential to suffer from significant self heating. We study in this paper self heating in multi-fin devices. We first propose a distributed thermal channel model and validate it using ANSYS. We use this model to study the electro-thermal properties of multi-fin devices with both flared and rectangular channel extensions. We analyze variations in fin geometric parameters such as fin width, gate length, and fin and gate height, and we investigate the impact on thermal sensitivity. We utilize a thermal sensitivity metric, METS, to characterize device thermal robustness. We provide experimental data to validate our findings. Our work is novel as it is the first to address thermal issues within multi-fin devices. Furthermore, it provides an impetus for further research on the emerging area of electro-thermal device and circuit design.

1. INTRODUCTION

Next-generation VLSI circuits will be composed of devices with dimensions in the nanometer range (e.g. sub-100nm gate lengths). For many decades, planar devices have been the favorites for both bulk and SOI processing. Planar devices however are susceptible to scaling effects. Subthreshold conduction (e.g. leakage current) is the major hurdle that these devices have yet to overcome. Leakage current stems from decreased oxide thicknesses, higher substrate dopings, and decreased channel lengths. A lowered threshold voltage to obtain better performance at lower operating voltages further exasperates the leakage problem.

The 2003 International Technology Roadmap for Semiconductors predicts several transistor improvements, including strained Si-channels, ultra-thin bodies, and metallic junctions [1]. It also predicts the move towards double-gate devices which allow more than one gate terminal to control the transistor channel. Among double-gated devices, the finFET, originally dubbed as the folded-channel MOSFET [5], promises better alignment of the double gates. Moreover, finFETs have high current drive and offer substantially better control over leakage and short channel effects.

Like a traditional MOSFET, the finFET is composed of a channel, a source, a drain, and a gate. The channel is embodied in a *fin* protruding out of the wafer plane. The fin is fabricated out of either undoped or lightly doped silicon. The gates of the finFET are created by wrapping the gate material around the three sides of the silicon fin, resulting in self-aligned front and back gates. Figure 1 shows the geometric parameters for a finFET. L_{gate} is the gate length; H_{fin} is the fin height; W_{fin} is the fin width or thickness; t_{ox} is the oxide thickness between the side gates and the fin; t_{ox-top} is the oxide thickness between the top gate and the fin. The width of a finFET is defined as: $W = 2 \times H_{fin}$. finFET fabrication uses a typical planar fabrication process with several new masks introduced into the process [10]. Hisamoto et al. [4] devised one of the first finFET fabrication flows, and several others have improved on it [3, 8, 19, 20]. The main flow roughly consists of etching a fin out of the silicon wafer, depositing the source and drain, depositing the gate oxides, and finally depositing the gate material.

While providing promising electrostatic characteristics, finFETs, along with other nanoscale devices, pose non-trivial self-heating challenges. Traditional device thermal modeling uses the heat diffusion equation to estimate the temperature at any point within the device at any instant in time [6, 14]. As device dimensions shrink into the nanometer range, the heat diffusion equation fails to capture the dominant heat transport mechanism (phonons), and does not consider the degraded thermal conductivity due to the reduced phonon mean free path [7]. The Boltzmann Transport Equation (BTE) can be used to estimate hot spots within a device with reasonable accuracy [11, 15]. While the BTE provides accurate temperature estimations, compact device modeling is needed to examine devices at a circuit level in order to balance a device's electrical and thermal performance [3, 12]. FinFET thermal problems are further exasperated with the construction of wider finFETs built using tightly-packed parallel fins between the source and the drain, hindering heat removal from the middle fins [17]. A multi-fin device is shown in Figure 2.

Our paper studies the effects of steady-state self-heating in multi-fin devices. We propose a distributed thermal model of the fin that improves the accuracy of the ultra-thin body (UTB) SOI thermal model introduced by Pop, Dutton, and Goodson [12]. We validate our model via ANSYS, a finite-element solver. We then extend the model to account for flared channel extensions and multiple-fins. By carefully examining the multi-fin model, we are able to identify the key parameters that affect device thermal sensitivity and maximum temperatures within multi-fin devices. We utilize a thermal sensitivity metric, METS [16], to characterize device thermal robustness. We provide several experiments to examine the thermal profiles and sensitivities of multi-fin devices. Our findings can be used to guide the design of optimal finFET devices, and to drive thermal-aware transistor and circuit-level optimizations. This area of device design will become important, specially for analog circuits, with the potential impact of temperature on performance and reliability.

The rest of the paper is organized as follows. We review in Section 2 the Pop et al. ultra-thin device model. In Section 3, we propose our single-fin distributed thermal model, compare our model with ANSYS, and extend the model for flared channel extensions.

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In Section 4, we model multi-fin devices. We provide experimental results in Section 5. We conclude by highlighting our findings and the role of thermal device modeling and its implication on circuit design.

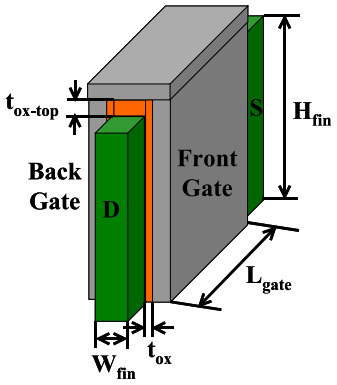


Figure 1: FinFET device.

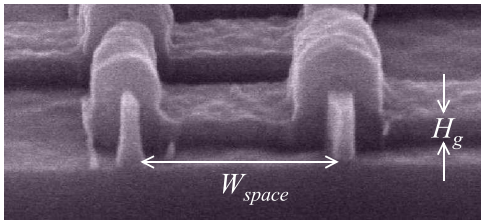


Figure 2: Multi-fin device [2].

2. BACKGROUND: THERMAL ANALYSIS FOR SINGLE-FIN DEVICES

Heat is generated in n-type transistors because of electron-phonon interactions. When a device is turned on, free electrons in the source are accelerated through the channel to the drain region. This acceleration causes the electrons to gain energy as they move through the channel. Once in the drain region, electrons are free to scatter with other electrons, phonons, impurity atoms, etc. Electron-phonon scattering results in an energy exchange between the electrons and the lattice, causing the lattice temperature to increase (other scattering mechanisms change electron momentum, but not energy) [13].

Heat generated in the drain region of a finFET device causes a temperature gradient within the device. A detailed discussion of heat generation within transistors can be found in [9, 13]. An approximation of the generated heat (Watts) is:

$$Q = I_D \cdot V_{GS} \tag{1}$$

The relationship between heat and temperature is governed by Fourier's law of heat conduction as shown in equation (2), where ΔT is temperature difference, L is the length of the heat conduction, k is the thermal conductivity of material in the heat conduction path, A is the cross sectional area of heat conduction, and Q is the heat.

$$\Delta T = \frac{L}{k \cdot A} \cdot Q \tag{2}$$

The electrical analogy of Fourier's law is Ohm's law. When heat is applied to a solid, a temperature gradient forms across the solid. This relationship is mathematically identical to an electrical current creating a voltage difference across and electrical resistor when forced through the resistor. If substitutions are made in equation (2) such that $\Delta T = \Delta V$, $Q = I$, and $L/kA = R$, the equation appears in the form of Ohm's law, $\Delta V = R \cdot I$. The equivalence between Fourier's law and Ohm's law is useful. Heat transfer analysis involving complicated geometries can be simplified by identifying select points within the geometry where temperatures are to be calculated. SPICE can then be used to solve for node voltages (i.e. temperatures) in the thermal network [18].

Pop et al. introduced a thermal model for an ultra-thin body SOI (UTB-SOI) device using the thermal-electrical equivalence [12]. The model uses a reduced thermal conductivity to account for the thin device geometry and impurity effects on the phonon mean free path. While not accounting for all thermal nano concerns, the model can be applied to devices with different gating structures, including finFETs. We refer to this model as the UTB model in the rest of the paper.

An ultra-thin device and its equivalent UTB model are respectively shown in Figure 3 and in Figure 4. The gate, drain, and source pads are assumed to connect through metal contacts to other circuit elements. Their top surface is assumed to be at a reference temperature. Adiabatic boundary conditions are applied to all other surfaces, resulting in heat flow in and out of the device at the top surface of the pads. Equivalent resistances are calculated using the formula $R = L/kA$, based on the materials and geometries through which heat transfer occurs. The current source representing the heat Q can be applied to the UTB model at the drain node since it is the heat generation region. The injected current can be calculated using equation (1). Circuit analysis can then be used to solve for the temperatures at the drain, source, channel, and gate. Pop et al.'s findings showed that the device temperatures are most sensitive to the drain pad and channel extension dimensions.

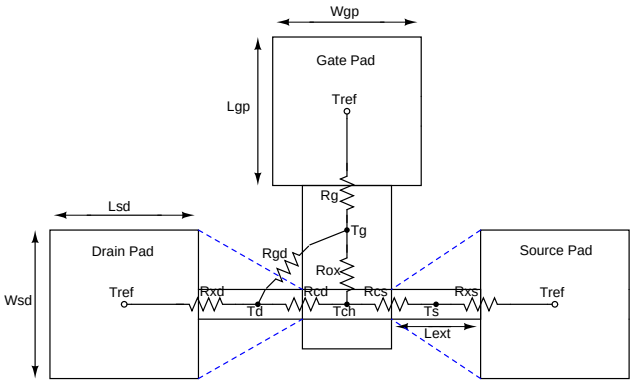


Figure 3: Top view of a finFET layout with equivalent thermal resistances [12]. Only one gate pad is used for this analysis.

3. SINGLE-FIN DISTRIBUTED THERMAL MODEL

We intend to use the UTB device model to investigate the effects of fin layout, finFET sensitivity and device geometries on the maximum temperatures of multi-fin devices. Using the device geometries in Table 1, we compared the temperatures obtained using the UTB model with ones obtained using ANSYS, a finite-element solver. The heat distribution obtained using ANSYS is shown in Figure 6.

We constructed the UTB device model with two different channel models based on lumped resistance and distributed resistance.

L_g	H_g	W_g	H_{fin}	W_{fin}	t_{ox}	L_{ext}	L_q	L_{sd}	W_{sd}
50*nm*	75*nm*	140*nm*	65*nm*	10*nm*	16Å	50*nm*	5*nm*	200*nm*	200*nm*

H_{sd}	L_{gp}	W_{gp}	W_{space}	R_{if}	k_g	k_{ch}	k_{ext}	k_{ox}	k_{sd}
65*nm*	200*nm*	200*nm*	100*nm*	$20E-9\frac{m^2 \cdot K}{W}$	$45.3\frac{W}{m \cdot K}$	$6.5\frac{W}{m \cdot K}$	$13.0\frac{W}{m \cdot K}$	$1.38\frac{W}{m \cdot K}$	$13.0\frac{W}{m \cdot K}$

Table 1: Model finFET dimensions and thermal conductivities

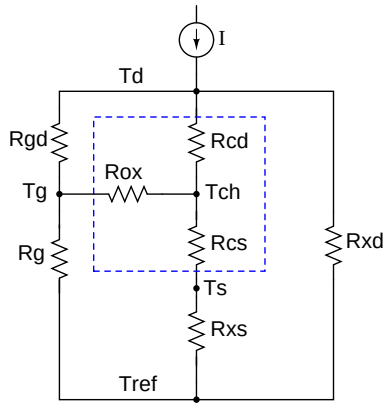


Figure 4: Pop's equivalent thermal circuit [12].

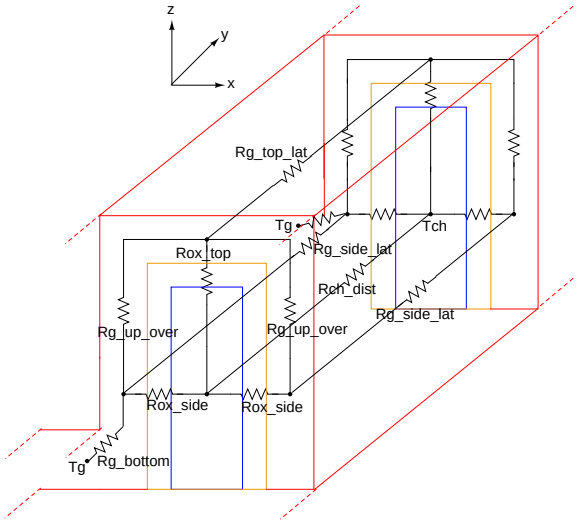


Figure 5: Thermal circuit distributed channel resistance model which replaces R_{ox}, R_{cd}, and R_{cs} in Figure 4.

The lumped channel resistance model uses R_{ox}, R_{cd}, and R_{cs} to approximate heat flow through the channel, oxide, and gate regions. As a first order approximation, the lumped channel model predicts heat flow through the device fairly well. However, in comparison to the finite-element solution, we realized that the lumped channel model could be improved. This is due to the 3-D nature of heat flow in the channel region.

To capture the 3-D heat flow effects in the UTB model, we created a distributed thermal resistance network within the channel region, as shown in Figure 5. This model replaces R_{ox}, R_{cd}, and R_{cs} in the original UTB model. We slice the channel into *n segments* resulting in *n-1 cuts*. The segments represent distributed

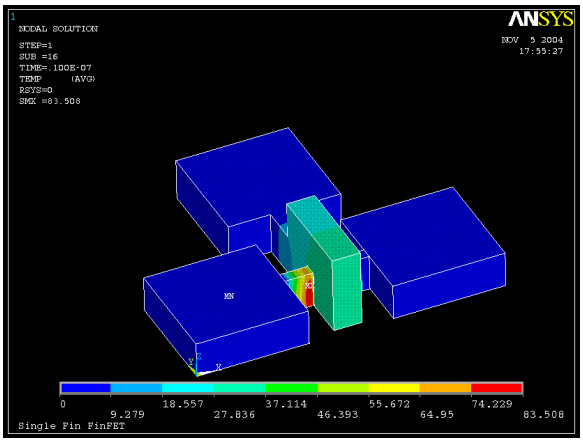


Figure 6: ANSYS thermal model of a finFET.

lateral heat flow within the channel. At each cut (the x direction in Figure 5) we introduce two resistors, labeled R_{ox_side}, to represent the thermal resistance between the center of the fin and the front and back gates. Similarly, we use R_{ox_top} to represent the thermal resistance between the center of the fin and the top gate. To model the thermal resistance through the gate material, we introduce $R_{g\_up\_over}$. We also add at each cut R_{g_bottom}, representing the thermal resistance between each cut and the thermal gate node (T_g in Figure 4). Along each segment (the y direction in Figure 5) we introduced four resistances $R_{g\_side\_lat}$, $R_{g\_side\_lat}$,$R_{g\_top\_lat}$, and R_{ch_dist}. These four resistors connect the thermal nodes within each cut.

Using the distributed channel model improves the accuracy of the UTB model when compared to ANSYS. The correspondence between nodal temperatures of the UTB model and ANSYS simulation temperatures ensured the correct heat (Q) and thermal resistances have been applied in the single-fin finFET thermal model. The thermal conductivities used in the ANSYS model are the same ones used in the UTB model. To provide a heat generation rate, q''', to ANSYS, we use the values of I_D and V_{GS} in (1) to calculate J and E. J is the current density through the fin, and E is the electric field applied to the gate. The heat generation rate q''' ($Watts/m^3$) can be computed as using [15]:

$$Q/m^3 = J \cdot E \tag{3}$$

Table 2 shows the results for three different devices using SPICE and ANSYS simulations. The three device sizes (nominal W_{fin}, 2x, and 4x) demonstrate the applicability of the model over a range of device sizes. Table 2 also shows how the distributed channel improves the accuracy of the model. T_d represents the drain temperature in the heat generation region. T_{ch} corresponds to the temperature in the middle of the channel, equidistant from the source and drain. T_g represents the gate temperature between the fin and the gate pad, while T_s corresponds to the source temperature at the edge of the gate where electrons are injected into

	$W_{fin} = 10nm$			$W_{fin} = 20nm$			$W_{fin} = 40nm$		
	ANSYS	Lumped	Dist.	ANSYS	Lumped	Dist.	ANSYS	Lumped	Dist.
T_d	59.57	96.66	60.42	62.57	79.99	59.26	63.05	67.40	58.35
T_{ch}	17.80	14.18	16.19	24.70	19.29	22.11	28.51	24.30	28.47
T_g	9.66	12.26	11.06	13.00	16.83	14.61	15.37	21.53	18.17
T_s	13.58	7.71	12.57	17.85	11.13	16.48	20.86	15.19	20.96

Table 2: Thermal model nodal temperatures and simulated ANSYS temperatures. All temperatures are in degrees Celsius.

the channel. The ANSYS results are based on averaging the temperatures over a thin cross-section. The lumped and distributed columns correspond to the two different channel geometries in the UTB model. As Table 2 shows, the maximum discrepancy between the distributed model with 20 segments and finite-element solution is $4.70°C$ and the source temperatures (T_s) match within $1.37°C$. The differences are due to approximations made to compute the resistance values. The correlation between ANSYS and our distributed model degraded with fewer than 20 segments. The remainder of this work is based on the UTB distributed channel model with 20 segments.

Electrical and thermal device performance is dependent on the fin layout. Figure 3 shows two finFET channel extension layout styles; standard rectangular fin and a flared fin (shown as blue dashed lines in Figure 3). Using a flared channel extension can improve device performance as the parasitic source/drain series resistance is reduced. The increase in device current translates into larger heat generation rates. In order to properly estimate device temperatures, the UTB model must account for flared channel extensions. We alter the UTB model R_{xd} and R_{xs} resistances based on fin width and source/drain pad width. Inclusion of channel extension flaring allows us to compare the thermal effects of rectangular and flared channel extensions.

4. MULTI-FIN THERMAL MODEL

To model wider finFETs with multiple fins, the equivalent thermal circuit model described in Section 2 is modified as follows. We assume that fins are spaced some distance W_{space} apart, and that there will be two gate pads, one on each side of the outside-most fins. If a flared channel extension is used, the thermal resistance of the extension is based on fin spacing, W_{space}, not the source/drain pad width.

If an instance of Figure 4 is used for each fin, only these outer fins can have the resistor R_g. An open circuit replaces R_g for all inner fins. Furthermore, gate nodes of adjacent fins will be connected by an inter-gate thermal resistance, R_i, representing the heat flux path between fins through the poly gate. This inter-gate resistance R_i is calculated using $R = L/kA$ where L is the fin separation W_{space}, k is the thermal conductivity of polysilicon, and A is the cross sectional area of heat flow through the gate poly. Heat injection occurs within the drain region for each fin.

5. EXPERIMENTAL RESULTS

Our goal is to examine the thermal properties and sensitivities of rectangular and flared channel multi-fin devices. We first show multi-fin temperature profiles. We then examine thermal sensitivity. Finally, we vary fin geometries and investigate the impact of gate length, gate height, fin width, fin height, and fin spacing on the temperature of multi-fin devices. Our baseline (nominal) device is a single fin (distributed channel model, rectangular fin extension) with the parameters shown in Table 1. Our data, when normalized, is in reference to this single-fin case.

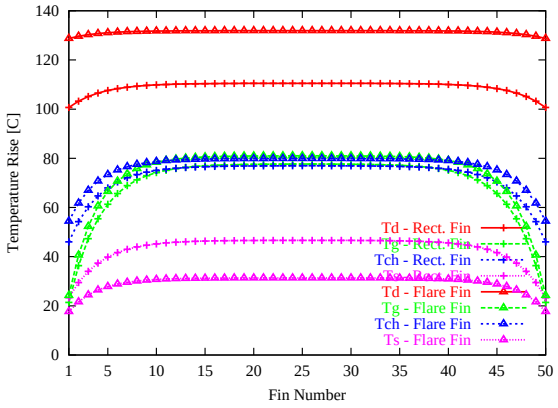


Figure 7: Temperature profile at the source (T_s), channel (T_{ch}), gate (T_g), and drain (T_d), for a 50-fin device. The rectangular channel extension device is represented by *Rect. Fin*, while the flared channel extension device is shown as *Flare Fin*.

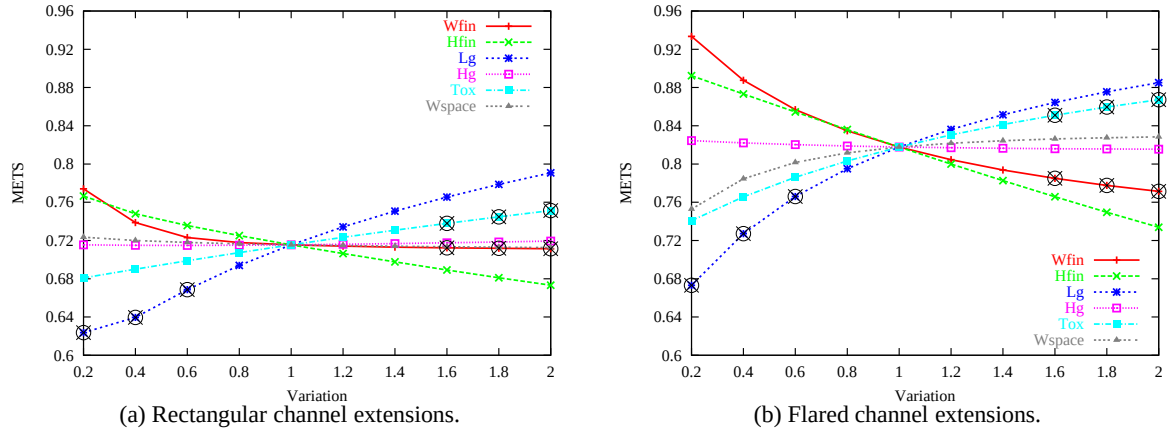
5.1. Multi-Fin Thermal Profile

We first examine the temperature profile of two 50-fin devices: one with a rectangular channel extension, and another with a flared channel extension. We assume that fins are spaced at a distance, W_{space}, of 100nm. Figure 7 shows a plot of temperature rise (above ambient) of the drain (T_d), the gate (T_g), the channel (T_{ch}), and the gate (T_g) for each of the 50 fins.

Several observations can be made. First, the flared channel extension yields higher temperatures at all nodes due to the improved electrical performance and thus the increased heat generation. Second, the inner fins are hotter than outer ones for the drain, source, gate, and channel. The drain temperature, while the hottest part of the finFET, has the smallest variation across the fins. Third, the gate temperature for the inner fins is hotter than the channel temperature. This is because each fin has the same access to the source/drain pads; however, the gate pads at the reference temperature are further away from the inner fins. The gate pads are effective at removing the heat from the gates for outer fins, but less so for the inner fins. Finally, for the majority of inner fins, the temperature is relatively constant from one fin to the next. Thus, adding more fins to a device beyond a certain number of fins will no longer increase peak temperatures.

5.2. Peak Temperatures for Multi-Fin Devices

The peak temperatures for devices with 1, 3, 5, 10, 25, and 50 fins are compared in Figure 8. The results are consistent with those shown in Figure 7. Indeed, the flared channel extension causes higher temperatures than the rectangular channel extension. Also, the maximum temperature at the drain, source, channel, and gate increases with a larger number of fins, but reaches steady state at



(a) Rectangular channel extensions. (b) Flared channel extensions.

Figure 9: Thermal sensitivity plot for 50-fin rectangular channel extension and flared channel extension devices. The parameter variation ranges from 0.2x to 2x a nominal device. The METS range is [0,1] with a value of 1 representing thermal insensitivity. Points with an x through them indicate that the device does not conform to the fin electrical design recommendations.

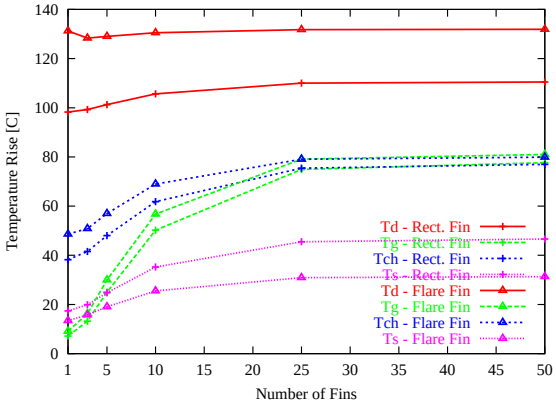


Figure 8: Temperature dependence (at the source, channel, gate, and drain) on the number of fins, demonstrated for 1, 3, 5, 10, 25, and 50-fin devices. The different channel extension configuration are represented as *Rect. Fin* and *Flare Fin*.

or beyond 25 fins. For a single-fin device, the source temperature is at a higher temperature than the gate; however, with 5 or more fins, the gate temperature exceeds that of the source. This is due to hindrance of heat removal from the inner fins due to the increased proximity from the source and drain pads.

5.3. Thermal Sensitivity of 50-Fin Devices

The confined dimensions and complex geometries of finFETs can lead to significant self-heating, which can degrade device performance, which in turn reduces heat generation. The robustness of a device to this regenerative effect is captured using a proposed metric called METS, *M*etric for *E*lectro-*T*hermal *S*ensitivity *METS* [16]. METS is derived from the ratio of current change to temperature changes with and without electo-thermal simulations, and it ranges from 0 to 1. A unity value indicates that a device's electrical performance is immune to self-heating. A lower value indicates less robustness to self-heating. In [16], METS is applied to evaluate the thermal robustness of a single-fin device. Here, we apply this metric to multi-fin devices to understand the impact of geometric variations on device thermal robustness.

Figure 9(a) shows the METS for a multi-fin device with rectangular channel extensions, while Figure 9(b) shows the METS for a multi-fin flared-channel device. To understand the impact of geometric process variations, we varied W_{fin}, H_{fin}, L_g, H_g, and T_{ox} from 0.2x to 2x our nominal device, and we computed the METS for these devices. For a nominal device (x=1 in both figures), the METS for a flared-channel device is higher than that of a rectangular-channel device (0.82 vs 0.72). This indicates that the flared channel extension is effective in reducing the thermal sensitivity of finFETs. The flared channel extension decreases both the thermal and electrical resistance of the extensions resulting in higher device currents and larger heat flow through the extensions to the pads. The geometric variations from the nominal device have less of an impact on both temperature and current thus making the flared device more robust than the rectangular one. Thus, despite the increase in device nodal temperatures as we saw in Figure 7, the flared channel multi-fin device is thermally more robust than the one with rectangular extensions.

5.4. Thermal Sensitivities of Multi-Fin Devices

From Figure 9(a), for -20% variations for a 50-fin device, the device is most electro-thermally sensitive to L_g, then T_{ox}, then H_g, then W_{space}, then W_{fin}, and least to H_{fin}. This implies that the change in current per degree rise in temperature is more pronounced for the change in L_g than it is for H_{fin}. We emphasize here that each device variation will electrically produce a certain change in the current. However, here we are examining the co-dependence of electrical and thermal properties, and not the absolute change in current. To investigate how thermal sensitivities change for devices with different number of fins, we performed the following study.

For each device size (1, 3, 5, 10, 25, and 50 fin device) we examined the current and temperature co-dependence for -20% variation in the geometric parameters. As we saw earlier in Figure 8, a wider device has higher peak temperatures. This suggests that as the number of fins per device increases, the current through each fin of the device decreases, resulting in heightened thermal sensitivity and reduced METS. Our study confirms this. Figure 10 examines the increase in current (relative to a nominal device) per degree change in temperature. The figure thus shows the normalized average current change per degree Celsius versus

METS for the different (-20% of nominal) variations in a multi-fin rectangular-extension device. We make two observations. First, for each variation, the METS increases with a reduced number of fins. That is, multi-fin devices are less robust to self heating than single-fin devices, and spread-heating is evident. Second, for a n-fin device, where n equals 50, 25, 10, 5, 3, and 1, the figure shows that variations in H_{fin} and W_{fin} have the lowest METS, thus suggesting that these two parameters are the least sensitive among the examined parameters, resulting in the least change of current per change in temperature.

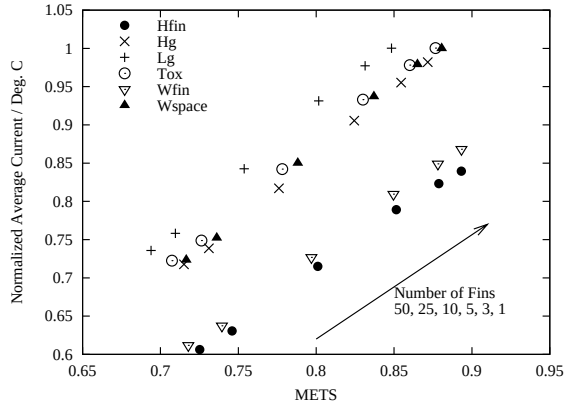


Figure 10: Correlation of METS to change in current per degree Celsius for a rectangular channel extension device with a -20% variation in W_{fin}, H_{fin}, L_g, H_g, and T_{ox}. The current is normalized to that of a nominal single-fin device.

6. CONCLUSION

We developed in this paper a distributed thermal model that improves over the UTB compact thermal model proposed by Pop et al. [12]. We validated our model against ANSYS simulations and we found reasonably accurate results. Using this model, we examined both the thermal profiles and thermal sensitivities of multi-fin devices built with both rectangular and flared channel extensions. We found the flared channel extensions to be more thermally robust despite their hotter temperatures. We also studied the impact of geometric variations, and used METS to assess the electro-thermal impact of such variations. We found that fin height and fin width are most electro-thermally robust to variations. We also showed that devices with fewer fins have improved device thermal sensitivity.

Our findings motivate further research into the newly emerging area of research, *electro-thermal device design*. There is a need to balance electrical and thermal properties. The impact of confined device geometries and ballistic electron transport on device reliability must be carefully examined. In addition, our device-level thermal study paves the way for layout and circuit-level thermal investigations.

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