



HAL
open science

Infrastructures for Education, Research and Industry in Microelectronics - recent developments

Bernard Courtois, Kholdoun Torki, Sébastien Colin, Hubert Delori, Sylvaine Eyraud, Jean-François Paillotin, Gregory Dipendina, Sophie Dumont

► **To cite this version:**

Bernard Courtois, Kholdoun Torki, Sébastien Colin, Hubert Delori, Sylvaine Eyraud, et al.. Infrastructures for Education, Research and Industry in Microelectronics - recent developments. 2007. <hal-00162486>

HAL Id: hal-00162486

<https://hal.science/hal-00162486v1>

Preprint submitted on 13 Jul 2007

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



HAL Authorization

Infrastructures for Education, Research and Industry in Microelectronics – Recent Developments

B. Courtois, K. Torki, S. Colin, H. Delori, S. Eyraud, J-F Paillotin, G. di Pendina, S. Dumont
CMP Service - 46 avenue Félix Viallet – 38031 Grenoble Cedex – France, E-mail: Bernard.Courtois@imag.fr

Abstract: Infrastructures to provide access to custom integrated hardware manufacturing facilities are important because they allow Students and Researchers to access professional facilities at a reasonable cost, and they allow Companies to access small volume production, otherwise difficult to obtain directly from manufacturers. This paper is reviewing the most recent developments at CMP like the introduction of a CMOS 65nm process, and the cooperation between the major infrastructures services available worldwide.

I. THE NEED FOR INFRASTRUCTURES

Infrastructures to provide access to custom integrated hardware manufacturing facilities are important for several reasons:

- they allow Students and Researchers to access professional facilities at a reasonable cost,
- they allow Companies to access small volume production, otherwise difficult to obtain directly from manufacturers.

The needs of Universities, Research Laboratories and Companies can be summarized as follows:

- Universities need to have access to technology for teaching their students. Those students will be in the industry. Therefore they have to be trained at least on the actual state of the art technology processes.
- Research Laboratories usually need to have high performance technologies to validate new concepts. The quality of the research results depends mostly on the quality of the technologies. Accessing to up to date technologies is a necessity.
- Industrial users also need to access to the state of the art of the offered technologies. This is vital for industrial users. The development of a product is usually long (more than 1 or 2 years). It is necessary that an industrial user has access to an up to date process, giving guaranty on product life.

Offering manufacturing Services has to be governed by the following basic principles:

- industrial quality process lines should be used (University process lines cannot offer a stable yield),
- design kits to link CAD and MPC/MPW facilities should be offered to ease the design.

It is also to be noted that almost every country or continent is a high cost country or continent to another one at the time of global markets. It is thus important to keep students, researchers, industrialists ahead of others in order to stay in

business. To stay ahead means to train, research, use, advanced design methods and tools and to design on advanced processes.

II. DEVELOPMENTS AT CMP

A review of early national efforts can be found in [1], and a review of first cooperative initiatives may be found in [2]. Since 1981 several periods may be distinguished, starting from a NMOS process in 1981 to the introduction of a 65 nm CMOS process in late 2005.

Processes available: Presently the processes available for ICs and MEMS manufacturing are depicted in Table 1.

Austriamicrosystems	0.35μ CMOS C35B4C3
	0.35μ CMOS C35B4M3
	0.35μ CMOS-Opto C35B4O1
	0.35μ CMOS Flash C35B4E3
	0.35μ SiGe BiCMOS S35D4M5
	0.35μ HV-CMOS H35B4D3
STMicroelectronics	0.12μ CMOS HCMOS9GP
	90nm CMOS CMOS090
	65nm CMOS CMOS065
	0.35μ SiGe BiCMOS BiCMOS6G
	0.25μ SiGe:C BiCMOS7RF
OMMIC	0.2μ HEMT GaAs ED02AH
	0.2μ HEMT GaAs ED02AH Bulk Micromachining
MEMSCAP	ASIMPS CMOS + DRIE
	PolyMUMPs
	SOI MUMPs
	Metal MUMPs
CSMC	0.6μ CMOS 2P/2M/HR
	0.6 μ CMOS 2P/2M/HR Bulk Micromachining

TABLE 1: CMP IC AND MEMS PROCESSES AVAILABLE

ICs design kits and CAD software: Design kits and libraries are distributed by CMP for most of the processes and most commonly used CAD tools. CMP sometimes develop design kits, in cooperation with the manufacturers and the CAD vendors. CMP also offers special CAD software conditions from a few CAD vendors. As a focal point, CMP also distributes information on configuration files, converters, etc. About 40 design kits are available for each process and the main CAD tools.

Other services: Packaging and testing services are also offered. Various types of packages are supported, including DIL, SOIC, CQFP, JLCC, PGA, etc. Test of prototypes is usually done by the final user. On request, especially for low volume production, CMP may take over testing together with manufacturing.

Key figures: Since 1981, CMP has served more than 1000 Institutions from 66 countries in various processes. Support to Industry started in 1993 for small volume production. CMP is ISO 9002-1994 certified from 2000 to 2003. CMP is working on the certification ISO 9002-2000.

Recent developments: Recent developments have been the move to very deep submicron processes: 120 nm CMOS, 90 nm CMOS, 65 nm CMOS, .35 μ HBT SiGe BiCMOS, .25 μ SiGe:C HBT BiCMOS from STMicroelectronics and the exploration of new MEMS fabrication offerings.

The move to very deep submicron processes: CMP introduced 120 nm CMOS as early as 2001. A total of 175 circuits were fabricated from 2001 to June 2007. CMP introduced 90 nm CMOS in 2004 and nearly 100 circuits have been fabricated up to now. Finally 65nm CMOS was launched in 2006 and a ten of circuits have been fabricated already. This means a total of nearly 300 circuits coming from about 50 Research Laboratories and Industrial Companies. These processes have been very well received. Let's detail what happened with the CMOS 90 nm. The 90nm CMOS has been announced in 2004, first DRMs and design kits have been shipped to designers in 2004. The list of Institutions who have used the 90nm CMOS to date is depicted in Table 2. One can notice a number of top level Universities in Europe and USA mostly. All Canadian Universities are using the 90nm CMOS process. The move to 65nm has started. The 65nm CMOS has been announced in 2006. The Table 3 depicts the list of Institutions who have received the DRMs and design kits up to now. Again there are many top level Universities in Europe and in USA who are moving to 65nm CMOS.

CANADA : 2	AUSTRALIA : 1
DENMARK : 1	BRAZIL : 2
FINLAND : 1	CANADA : 1
FRANCE : 2	FINLAND : 2
GERMANY : 1	FRANCE : 8
ITALY : 3	GERMANY : 1
NORWAY : 3	ITALY : 9
SPAIN : 1	NORWAY : 2
SWEDEN : 1	SPAIN : 4
SWITZERLAND : 2	SWEDEN : 1
USA : 8	SWITZERLAND : 3
	TUNISIA : 1
25 Institutions from 11 countries	U.K : 4
	USA : 12
	51 Institutions from 14 countries
TABLE 2: INSTITUTIONS HAVING SUBMITTED CIRCUITS 90NM CMOS	TABLE 3: INSTITUTIONS HAVING RECEIVED THE 65NM DRMS & DESIGN KITS

Advanced MEMS processes: For many years, CMP has been offering the MUMPS processes from MEMSCAP: PolyMUMPS, MetalMUMPS, SOIMUMPS. Recently CMP has been moving to SUMMITV from SANDIA and to a MEMS process based on the CMU post process capabilities.

The SUMMIT (Sandia Ultra-planar Multi-level MEMS Technology) fabrication process is a five-layer polycrystalline silicon surface micromachining process (one ground plane/electrical interconnect layer and four mechanical layers). The MEMS structures made possible by this five-layer planarized surface micromachining process are extremely diversified. CMU post process is a post CMOS processing from Carnegie Mellon University. This post process, applied to an advanced process proposed by CMP (0.35 SiGe BiCMOS from STMicroelectronics), allows to combine on the same chip MEMS structures (resonators, cantilevers, accelerometers, etc.) and microelectronics structures of an advanced BiCMOS process. CMP also introduced a low cost bulk post process micromachining based on a CMOS .6μ from CSMC.

III. OTHER MAJOR INFRASTRUCTURES

There are 7 major infrastructure services today: CIC (Taiwan), CMC (Canada), CMP (France), IDEC (Korea), MOSIS (USA), VDEC (Japan) and ICC(China). Three of them, CMC, CMP and MOSIS have decided in 2002 to cooperate. In 2006, CMP and ICC have also set up a cooperation agreement. It might happen that further cooperation will be developed later on. The following briefly depicts 6 of these services, as per their inputs to the 2006 CMP Annual report.

CIC: National Chip Implementation Center (CIC) Project was initiated by the National Science Council in 1992. This project aims to pave the way for a national research and service center for IC/System design. In 1993, the task force of the CIC Project, under the leadership of Dr. Jen-Sheng Hwang, was established. Afterwards, Prof. Chen-Yi Lee was appointed as the Director General of CIC in 2000. In 2003, CIC affiliated to the National Applied Research Laboratories (NARL). Since 2004, Professor Jing-Yang Jou has been the Director General of CIC. In Table 4, the process technologies provided by CIC are listed.

CMOS 0.13μm 1-poly 8-metal	TSMC (3 runs/year)
CMOS 0.18μm 1-poly 6-metal	TSMC (5 runs/year)
CMOS 0.18μm 1-poly 6-meta	UMC (6 runs/year)
CMOS 0.35μm 2-poly 4-metal	TSMC (5 runs/year)
CMOS 0.35μm 2-poly 4-metal MEMS post-fabrication	ITRI (5 runs/year)
SiGe BiCMOS 0.35μm 3-poly 3-metal	TSMC (4 runs/year)
GaAs 2.0μmHBT	GCTC (1 run/year)
GaAs 0.15μm PHEMT	WIN (2 runs/year)

TABLE 4: CIC IC AND MEMS PROCESSES AVAILABLE

There were 1423 prototyped ICs being successfully fabricated in 2005, including 1377 ICs from the academics and 46 ICs

from the research institutes as well as domestic industrial sectors.

CMC: CMC Microsystems (www.cmc.ca) provides national infrastructure for microsystems research and technology development, accelerating Canadian competitiveness through the development of highly qualified people and the commercial advancement of research. Established in 1984 as a not-for-profit corporation, CMC manages a major five-year grant awarded by the Natural Sciences and Engineering Research Council of Canada (NSERC), matched by industrial contributions. For the period 2005-2010, CMC directs a national program valued at over \$110 million (including cash and in-kind contributions). In terms of fabrication services, CMC offers the following (Table 5):

90-nm CMOS	STMicroelectronics through CMP
0.13 μ CMOS	IBM through MOSIS
0.18 μ CMOS	TSMC through MOSIS
0.35 μ CMOS	TSMC through MOSIS
0.5 μ SiGe BiCMOS, 5AM & 5HP	TSMC through MOSIS
0.8 μ CMOS in three process flavors: high-voltage--up to 300V, mid-voltage range-- \pm 20V, and standard-voltage--2.7V to 5.5V	DALSA Semiconductor
2.5 GHz Bipolar linear array	Gennum Corporation
PolyMUMPs surface micromachining process	MEMSCAP through CMP
MetalMUMPs	MEMSCAP through CMP
Micragem SOI-based micromachining process	Micralyne Generalized MEMS process
Protolyne for semi-custom microfluidics device	Micralyne Generalized MEMS process
Protolyne for semi-custom microfluidics devices	Micralyne
Photonics/optoelectronics	through Canadian Photonics Fabrication Centre

TABLE 5: CMC IC AND MEMS PROCESSES AVAILABLE

A total of 403 designs were fabricated in 2006 using the technologies listed above.

ICC: Founded in 2000 by Science and Technology Commission of Shanghai Municipality, Shanghai Research Center for Integrated Circuit Design (so-called ICC) is dedicated in promoting Shanghai and all China IC Design industry to realize durative rapid development. ICC established the public service platform open to all IC design enterprises, universities and research institutes, providing full services to improve design quality and lower the cost. The services ICC provides include Multi-Project Wafer service, SoC design platform, testing service, training and evaluation, information service, etc. From 1996 to 2000, Shanghai MPW Service (SMS), operated by Fudan University, was mainly open to academic users. From 2001, ICC began to operate SMS, expanded the service to industrial sectors and became the China National MPW Center. Totally 761 designs from more than 250 design houses, universities and research institutes were prototyped on MPW

runs and low volume production since 2001. In 2006, the process technologies are listed in Table 6.

CSMC 0.6um CMOS
Chartered 0.35um CMOS
Chartered 0.25um CMOS
Chartered 0.35um SiGe
TSMC 0.18um CMOS
TSMC 0.25um CMOS
TSMC 0.35um CMOS
SMIC 0.18um CMOS
SMIC 0.35um EEPROM
HJTC 0.18um CMOS
HJTC 0.25um CMOS
HJTC 0.25um EEPROM

TABLE 6: ICC IC PROCESSES AVAILABLE

There are totally 22 runs in the year of 2006. 101 chips from 63 customers were successfully fabricated. Among those, 54 were industrial projects, the remaining 47 were educational and research projects. In 2006, ICC provided an SoC design support platform with the cores from ARM, ZSP, and Synopsys, such as ARM7TDMI, ARM926EJ, NEO, ZSP200, ZSP400.

IDEC: IDEC (Integrated Circuit Design Education Center) was launched in 1995 with the support of the Ministry of Commerce, Industry and Energy and major semiconductor industries for the purpose of educating designers in the non-memory IC field. The objectives of IDEC include (a) building-up and strengthening the infrastructure of VLSI design education; (b) training highly-qualified VLSI system designers; and (c) contributing to Korean semiconductor industries by promoting collaborations between universities and industries. Currently, IDEC provides MPW services for 62 WGs (Working Groups) in Korea. As of January 2007, a total of 1,814 IC chips have been successfully fabricated through the IDEC MPW (Multi-Project Wafer) program. The technologies being provided in 2007 are listed in Table 7:

CMOS 0.35 μ , 1-poly 4-metal	Samsung Electronics
CMOS 0.18 μ , 1-poly 4-metal	Samsung Electronics
CMOS 0.35 μ , 2-poly 4-metal	Magnachip/Hynix
CMOS 0.18 μ , 1-poly 6-meta	Magnachip/Hynix
CMOS 0.18 μ , 1-poly 6-metal	Dongbu Electronics
InGaP HBT	Knowledge-on

TABLE 7: IDEC IC PROCESSES AVAILABLE

The students who fabricate chips using IDEC MPW Service are required to give posters/demo presentations in the IDEC Chip Design Contest.

MOSIS: MOSIS is a low-cost prototyping and small volume production service for VLSI circuit development with a worldwide customer base. Since 1981, the service has fabricated more than 50,000 integrated circuit designs for use by commercial firms, government agencies and universities and has served as the model for similar operations throughout the world. It is a not-for-profit organization started in 1980 by

DARPA (Defense Advanced Research Projects Agency of the U.S. Department of Defense) at the Information Sciences Institute to provide their research community with access to advanced IC fabrication lines in a cost effective manner. In 1986, the service was further expanded to include U.S. commercial firms and in 1995 to include both commercial firms and educational institutions outside the U.S. Since 1994, MOSIS has been entirely self-supported, deriving all of its revenue from commercial operations. The processes available today from MOSIS are listed in Table 8.

Agilent/HP (Avago)	0.5 μ CMOS
AMI Semiconductor	0.35 μ , 0.5 μ , 0.7 μ , 1.5 μ CMOS
IBM	90nm, 0.13 μ , 0.18 μ and 0.25 μ CMOS 0.13 μ , 0.18 μ , 0.25 μ , 0.35 μ and 0.5 μ SiGe BiCMOS
TSMC	0.13 μ , 0.18 μ , 0.25 μ , 0.35 μ CMOS
Austriamicrosystems through CMP	0.35 μ CMOS; 0.35 μ HV CMOS 0.35 μ SiGe BiCMOS

TABLE 8: MOSIS IC PROCESSES AVAILABLE

CMOS-compatible MEMS technologies are also available.

VDEC: VLSI Design and Education Center (VDEC), which is located in the University of Tokyo, has been utilized by academic users in Japan since its foundation in May, 1996. As an MPC service center, VDEC aims at improvements of education on VLSI design and supports on VLSI chip fabrication for national universities, public universities, private universities and colleges in Japan. VDEC receives a lot of supports from Japan government, as well as semiconductor industries through STARC (Semiconductor Technology Academic Research Center). Presently the following technologies are available for chip fabrication service Table 9.

2-poly 2-metal CMOS 1.2 μ	SCG Japan Ltd (OnSemiconductor Ltd)
2-poly 3-metal CMOS 0.35 μ	Rohm Co. Ltd
1-poly 5-metal CMOS 0.18 μ	Rohm Co. Ltd
1-poly 5-metal CMOS 0.18 μ	Hitachi Ltd
2-metal 0.8 μ bipolar	NEC Compound Semicond Devices Ltd
1-poly 5-metal CMOS-SOI 0.15 μ	Oki Electric
1-poly 6-metal CMOS 90 nm	ASPLA
VDEC-MOSIS CMOS 0.25 μ /0.18 μ	TSMC
VDEC-MOSIS Si-Ge BiCMOS 0.5 μ	IBM

TABLE 9: VDEC PROCESSES AVAILABLE

Totally 445 chips on 6154 mm² silicon area were designed and fabricated in the last fiscal year (2005.4–2006.3). Besides, since 2003, some MOSIS chip fabrication technologies, such as TSMC 0.18 μ , 0.25 μ CMOS and IBM 0.5 μ Si-Ge BiCMOS, have been provided to VDEC users at a lower cost based on a close VDEC-MOSIS cooperative relationship.

IV. EXPANDING TO PCBs AND MEMS

CMP and MOSIS offered long ago to expand services to PCBs, but it seems that the needs were less important in this area. CMP also offered MCMs, but the offer was not taken very well. Another move has been very important: the expansion to

MEMS. CMP offered manufacturing for MEMS as early as 1995, being the first service to offer MEMS. Since then the portfolio has been largely expanding and today CMC-CMP-MOSIS offer MEMS manufacturing, including the PolyMUMPS, MetalMUMPS and SOIMUMPS from MEMSCAP. These 3 services enjoy a 10 years MEMS experience, obtained through 69 runs, 198 designs. It is important that MEMS can be obtained from the same services delivering ICs, so that integration (either at the packaging level or at the die level) is made easier.

V. PRESENT COOPERATIVE EFFORTS

Presently, the major cooperative effort is undertaken by CMC, CMP and MOSIS. These 3 infrastructure services announced it at DAC in June 2002. Since then, the cooperation has been steadily expanding [3]. Separately, CMP has also set up a number of bilateral cooperation with infrastructure services, with special groups in various countries, and has established distributors in several parts of the world.

VI. CONCLUSIONS

A few trends and comments may conclude. The major services are going global in terms of cooperation, acting worldwide. The more advanced services are also going global in terms of technologies, addressing in the future electronics, photonics, mechanics, fluidics, as CMC-CMP-MOSIS plan to do. It is worth to note that the 7 major infrastructure services share the same legal status (services hosted by a University). The most advanced of these services shared the same development in extending their services from Universities to Companies and evolving from a subsidized service (by Ministries, Agencies, etc.) to a non-profit non subsidized kind of service.

REFERENCES

- [1] "MPC Services available worldwide", invited paper, APCCAS'94 IEEE Asia-Pacific Conference on Circuits and Systems, December 5-8 1994, Grand Hotel, Taipei, Taiwan.
- [2] "Infrastructures for Education and Research: from National Initiatives to Worldwide Development", invited talk, Technical University of Darmstadt, M. GLESNER 60th birthday ceremony, 29 August 2003.
- [3] CMC, CMP & MOSIS, "The Scale of Cooperation Increases as the Dimensions of Microchips Decrease", invited paper, 3rd International Conference on MSE, 1-2 June 2003, Anaheim, USA.