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Low Schottky barrier source/drain for advanced MOS architecture: device design and material considerations

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Abstract

An alternative MOSFET architecture based on the use of low barrier Schottky source/drain (S/D) contacts coupled to a thin silicon-on-insulator (SOI) film is described. Two-dimensional device simulations are used to demonstrate the advantage of low Schottky barrier S/D over conventional implanted technologies in terms of current drive capabilities. It is shown that the silicide penetration in the silicon does not increase the contact resistance for this structure while a severe degradation of the current drive is observed for conventional MOS architectures. Experiments conducted on Pt/Ge metallic stacks on p-type silicon show that very low Schottky barriers to hole can be obtained (~ 50 meV).

1. Introduction

The sustained interest for the development of ultra-high density, high-frequency and low-power CMOS technology is highly motivated by new requirements of portability and power for information processing. Historically device scaling remains the primary method by which the semiconductor industry has improved productivity and performance. From the 130 nm technology node [1], upcoming CMOS technologies will have to face many grand challenges. Among them, a new dielectric gate stack that incorporates a high κ insulator will be needed. The objective of this paper is to focus on another critical problem associated with deeply scaled devices: the optimization of the source/drain (S/D) architecture. Based on data available in the International Technology Roadmap for Semiconductors (ITRS'99) [1], the strong constraints imposed to doping and contact technologies are recalled in Section 2. An alternative MOSFET architecture based on the use of low barrier Schottky S/D contacts coupled to a thin silicon-on-insulator (SOI) film is proposed in Section 3. In

Section 4, device simulations are used to demonstrate the reduced contact resistances of low Schottky barrier S/D with respect to conventional implanted technologies. Finally, preliminary results on material stacks that exhibit ultra-low Schottky barriers to holes are discussed.

2. Challenges related to S/D engineering

In conventional MOSFET architectures, the total resistance associated to the S/D structure results from the series combination of several components. The accumulation resistance R_{acc} characterizes the current confinement due to the overlap between the S/D extension and the gate.

A geometrical spreading resistance R_{sp} is subsequently associated to a link resistance R_{lnk} that accounts for the drop of electrical conductivity due to the lateral decay of doping concentration from the peak of the junction to the channel concentration [2,3]. Finally, R_{sh} gives the resistance of the deeper junction used for contacting and R_{co} reflects the contact resistance at the silicon/silicide interface. With devices shrinkage to smaller dimensions by a scaling factor α ($\alpha > 1$), R_{sh} remains nearly constant as the extension length is scaled in concert with the junction depth. The geometric

spreading resistance R_{sp} decreases as the junction depth becomes better matched to the channel depth. More problematic is the case of the link resistance R_{link} that requires steeper lateral doping profile to properly scale down (e.g. for the 35 nm technology node, abruptness should be 0.5 or 2.2 nm/dec depending on scaling criterion [1]). Finally, the contact resistance R_{co} also strongly impacts the total series resistance as it increases as the square of the scaling factor. Thus, the general trend for conventional bulk MOS transistor is clearly drawn: controlling the specific contact resistivity is essential to minimize R_{co} while sharp processing techniques are required to control the lateral steepness of the S/D extension that governs R_{link} .

Therefore, in the near term perspective, i.e. down to the 100 nm technology node, the difficulty will consist in the formation of ultra-shallow junctions with a highly controlled extension depth and a sufficient abruptness to control short channel effects [4]. Contacting the S/D regions with a low sheet resistance material and a low specific contact resistivity is also a challenge for conventional silicide processes. Among the main difficulties to face, the most important are:

- dopant activation above solid solubility to achieve low junction sheet resistance,
- steep 2D dopant profiling,
- boron penetration in gate oxide (p-MOS),
- low contact sheet resistance (silicide) and low contact specific resistivity (silicide/silicon interface) while minimizing the silicon consumption and reducing the contact area,
- maximum activated dopant concentration at the silicide/silicon interface,
- increased interdependency of doping and silicide processes.

3. Low Schottky barrier S/D architecture

As stated in the ITRS'99 for a long term perspective, the grand challenge below the 70 nm node may be crudely formulated as the transistor structure. This means that a completely new architecture is needed to achieve sufficiently low series resistances (<10% of the total device resistance) and ensure immunity against short channel effects as far as the S/D architecture is concerned. Several theoretical studies and scaling methods [5,6] tend to demonstrate that conventional MOSFET architectures fabricated on a bulk silicon substrate will not survive below ~50 nm of gate length without a severe degradation of the device performance (control of short channel effect, I_{on}/I_{off} trade-off, power consumption, frequency of operation, etc.). Alternative architectures are mainly based on the use of a very thin film SOI substrate: typical active SOI layer thicknesses

ranging between 2 and 20 nm are proposed for 10–40 nm gate length MOSFETs. Beyond the introduction of a thin SOI film, the novelty of the MOSFET architecture proposed in this paper lies in the use of low Schottky barrier (ideally 0 eV) contacts that replace the conventional ohmic contacts on a highly doped S/D region. Unlike other published Schottky barrier MOSFETs [7–9], the principle of operation is based on the accumulation mode. This structure is hereafter called the “Accumulation Low Schottky Barrier MOSFET” (ALSB-SOI-MOS). In the following, both simulation and experimental aspects are discussed under the scope of a p-channel MOSFET. However, the ALSB-MOS concept also applies to the n-channel counterpart as far as a low Schottky barriers to electrons can be obtained [10]. Table 1 summarizes the main roadblocks associated with the doping/contact technology and the solutions provided by the ALSB-SOI-MOS transistor architecture:

- The junction depth issue is inherently removed as Schottky contacts do not require doped S/D extensions.
- Silicide penetration and silicon consumption does not limit the current drive and can even provide enhanced current performance (Section 4.2).
- Material engineering can provide extremely low Schottky barrier (Section 5).
- High channel doping and related effects (dopant fluctuation, hot carriers) are minimized.

4. Simulated scaling properties of the S/D contacts

4.1. Choice of a conventional structure for comparison with the ALSB-SOI architecture

Schematic representations of the ALSB-SOI and of the conventional SOI structures are presented in Table 2. A fair comparison of electrical performance between the ALSB-SOI architecture and the conventional counterpart with implanted S/D and ohmic contacts proves to be a difficult task for several reasons:

- Considering its thin SOI film substrate, the ALSB-SOI-MOS structure controls short channel effect through the tight coupling between the front gate oxide and back buried oxide, allowing a low channel doping that also enhances mobility. For the sake of a fair comparison, our so-called ‘conventional MOS structure’ also benefits from the same thin SOI film and accumulation mode of operation.
- The S/D architecture of the conventional SOI MOSFET is based on a highly doped S/D extension with a $10^{-7} \Omega\text{cm}^2$ specific contact resistivity which is representative of the best midgap silicide used for ohmic contact [11]. The S/D extensions have been chosen with

Table 1

Main technology requirements imposed to S/D engineering for the 35 nm technology node and technological solutions provided by the ALSB-SOI-MOS architecture [1]

Technology challenges associated to conventional S/D	Solution provided by the ALSB-SOI architecture
Extremely reduced junction extension depth (8–13 nm) Lateral abruptness of source extension (0.5 nm/dec)	S/D contacts realized by Schottky contacts directly on the low doped SOI layer (no specific doping of S/D regions, e.g. ion implantation)
Very thin silicide thickness (12 nm) Reduced consumption of silicon by the silicide process (7–17 nm)	The thickness of the silicide and the corresponding thickness of silicon consumed by the silicidation reaction do not increase the contact resistance
Low contact sheet resistance for a reduced silicide thickness (12.5 Ω/\square for a silicide thickness of 12 nm)	
Extremely low specific contact resistivity at the silicide/silicon interface ($< 1.5 \times 10^{-8} \Omega\text{cm}^2$)	Contacting through a very low barrier Schottky: (a) <i>p-MOS case</i> : $\Phi_{bp} < 50$ meV, i.e. $\rho_s < 10^{-8} \Omega\text{cm}^2$ using a germanium-based stack (b) <i>n-MOS case</i> : Schottky metal or alloy still to be identified. Erbium disilicide gives $\Phi_{bn} \sim 0.2$ eV or $\rho_c \sim 210^{-6} \Omega\text{cm}^2$. Alloy with erbium still to explore
In case of bulk substrate, very high channel doping level and its interaction with the S/D extension abruptness ($3 \times 10^{19}\text{cm}^{-3}$)—Channel doping fluctuations	Lightly doped SOI film (typ. $\sim 10^{15}\text{cm}^{-3}$)

Table 2

Structural parameters of the ALSB-SOI-MOS and conventional SOI transistors used in device simulations

Structure	p-MOS ALSB-SOI-MOS	p-MOS SOI conventional S/D
Gate length (nm)	40	40
S/D architecture	Low barrier Schottky contact	Ohmic contacts on highly doped diffused regions
C_{SOI} (cm^{-3})	p-Type, 2×10^{15}	p-Type, 2×10^{15}
C_{SD} (cm^{-3})	–	p-Type, 2×10^{20}
Φ_{bp} (eV)	0.025	–
ρ_c (Ωcm^2)	–	10^{-7}
W_{spa} (nm)	10	10
t_{oxeq} (nm)	1	1
t_{si} (nm)	10	10
t_{box} (nm)	200	200
t_{sho} (nm)	Variable $0 \rightarrow t_{si}$	Variable $0 \rightarrow t_{si}$

an ideal lateral abrupt profile. Referring to the discussion in Section 2, the contribution of the link resistance R_{sh} becomes negligible while it usually alters the current drive as significantly as the contact resistance R_{co} does when the lateral doping steepness is not infinite [3]. Clearly, the box doping profile adopted for the conventional SOI structure should not affect unfavourably the total series resistance.

- Consumption of silicon during the silicidation reaction reduces the effective transfer area over which current crosses the silicon/silicide interface [12]. Thus, the contact resistance is expected to be strongly related to the silicide penetration depth into the SOI film as it will be demonstrated in Section 4.2. In case of very shallow junctions or very thin SOI films, the elevated S/D configuration obtained by selective epitaxial growth

[11] is a potential technique to minimize the contact and other components of the series resistance. This structure requires a very careful optimization of the doping profile in the elevated layer along with the layer and spacer thickness [13]. In an attempt to obtain a clear and comprehensive understanding with regard to the role of doping profile, Ref. [14] has shown that it was difficult to improve the contact resistance when the elevated layer was grown on a shallow junction (<35 nm). This was attributed to the extreme sensitivity of the specific contact resistivity with the interfacial doping concentration. Moreover, the elevated S/D may necessitate the use of large spacers to reduce the gate-to-S/D capacitance and/or the use of a second sidewall spacer covering the facets where the epitaxially grown layer is thinner near the oxide edges [15]. The consequence is an increase of the resistance R_{sh} associated to the junction length. Other techniques such as pattern-constrained epitaxy [16] or confined lateral selective epitaxial growth [17] can be used for elevating S/D regions but at the expense of process complexity. Finally, an alternative solution is to recess the channel but self-alignment of the gate to S/D dopings remains a difficult challenge to face [18].

In summary, the ALSB-SOI MOSFET is compared to the SOI MOSFET with conventional S/D sketched in Table 2. Although this conventional structure does not take a potential advantage of elevated S/D, it can be considered that the penalty is compensated by the ideal steep profile of the extension that makes the link resistance R_{sh} negligible [3].

4.2. Impact of the silicide penetration depth

The objective of this section is to demonstrate the advantages of the accumulation low Schottky barrier MOSFET with respect to conventional structures that use highly doped diffusions with ohmic contacts. A schematic representation of the ALSB-SOI and conventional SOI structures is given in Table 2. The gate length is set to 40 nm for both structures. The ALSB structure is a non overlapping S/D to gate structure characterized by a gap of 10 nm (W_{spa}). The conventional SOI structure has also a gate to S/D separation of 10 nm and a highly doped p^+ diffusion that extends up to the gate edge to obtain an exact overlapping. Figs. 1 and 2 show the $I_{DS}-V_{GS}$ characteristics for both structures at $V_{DS} = -1.2$ V, no silicide penetration into the SOI film ($t_{sho} = 0$ nm) and for gate lengths varying from 20 to 200 nm. In addition, the same figure also displays the $I_{DS}-V_{GS}$ curves at $V_{DS} = -0.1$ V for the two extreme gate lengths (20 and 200 nm) to outline the sensitivity to DIBL. Clearly, the ALSB-SOI MOSFET demonstrates better scaling properties in terms of subthreshold slope, DIBL and off-state current considering that both architectures have the same long channel linear threshold voltage (V_{TH} at $V_{DS} = -0.1$ V). In order to investigate

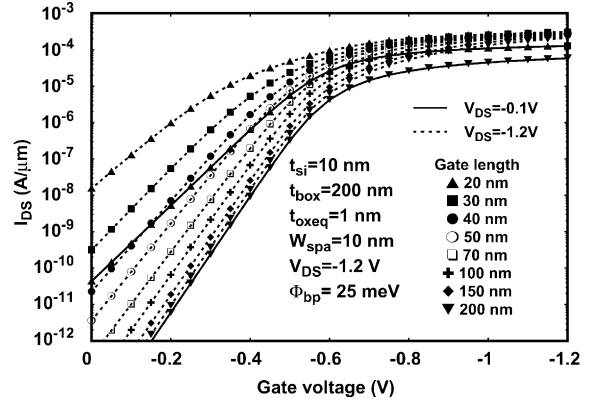


Fig. 1. Simulated set of $I_{DS}-V_{GS}$ characteristics of the ALSB-SOI MOSFET for different gate lengths. Dashed lines correspond to a S/D voltage $V_{DS} = -1.2$ V. Full lines correspond to the current-voltage curves obtained at $V_{DS} = -0.1$ V for the two extreme gate lengths, $L_G = 20$ and 200 nm.

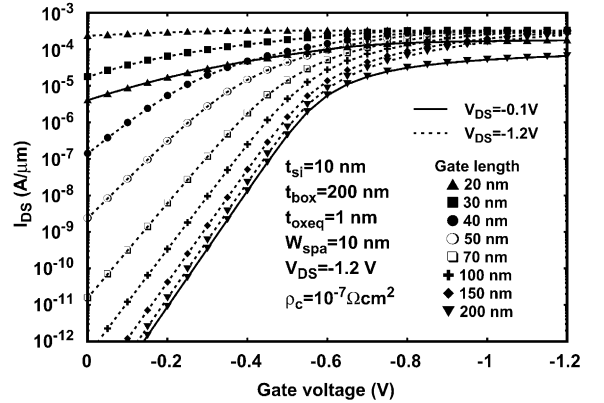


Fig. 2. Simulated set of $I_{DS}-V_{GS}$ characteristics of the conventional MOSFET for different gate lengths. Dashed lines correspond to a S/D voltage $V_{DS} = -1.2$ V. Full lines correspond to the current-voltage curves obtained at $V_{DS} = -0.1$ V for the two extreme gate lengths, $L_G = 20$ and 200 nm.

the impact of silicon consumption during the silicidation phase, a detailed study of the electrical performance has been conducted by varying the silicide penetration depth t_{sho} of the S/D contacts. Fig. 3 shows the variations of the maximum saturated transconductance at $V_{DS} = -1.2$ V as a function of the silicide penetration depth (t_{sho}). It clearly appears that the transconductance of the conventional SOI MOS structure is strongly reduced by a significant increase of the series resistances induced by a reduction of the effective surface of the contact. The same general trend is observed for the maximum saturated current at $V_{GS} = V_{DS} = -1.2$ V (Fig. 4). It is worth noting that performance reduction of the conventional MOSFET is monotonous with silicon consumption as

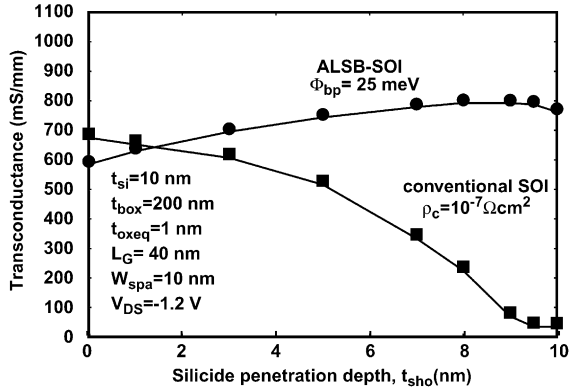


Fig. 3. Simulated variations of the maximum saturated transconductance as a function of the silicide penetration depth. In the ALSB case the Schottky barrier height is 25 meV and in the conventional case the specific contact resistance is $10^{-7} \Omega\text{cm}^2$. The simulated structures are described in Table 2.

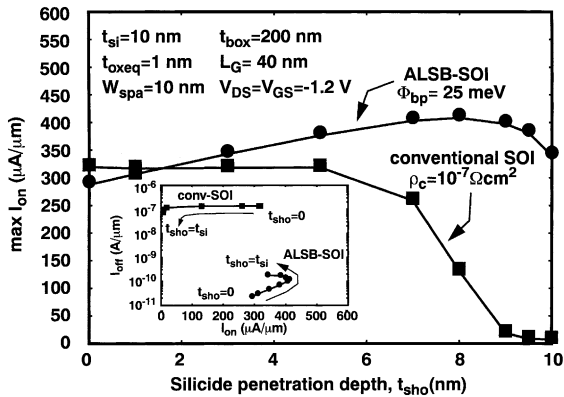


Fig. 4. Simulated variations of the maximum current at $V_{GS} = V_{DS} = -1.2 \text{ V}$ as a function of the silicide penetration depth. In the ALSB case the Schottky barrier height is 25 meV and in the conventional case the specific contact resistance is $10^{-7} \Omega\text{cm}^2$. The simulated structures are described in Table 2. The inset shows the I_{off} vs I_{on} characteristics obtained at $V_{DS} = -1.2 \text{ V}$.

already observed in [12]. In contrast, the ALSB-SOI-MOS structure first benefits from an increase in current and transconductance which is only slightly reduced for a quasi total consumption of the silicon film. The inset in Fig. 4 shows that an excellent I_{on}/I_{off} ratio is maintained for the ALSB-SOI structure even for the highest I_{on} current obtained at $t_{sho} \sim 8 \text{ nm}$. The impact of the silicide penetration depth t_{sho} on the transconductance and current performance can be explained simply by considering the schematic in Fig. 5. The contact resistance can be divided into two components associated in parallel:

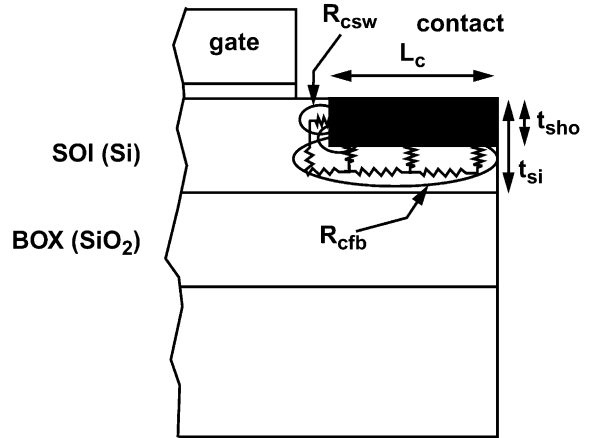


Fig. 5. Schematic representation of the two resistance components associated to the specific contact resistance. R_{cfb} and R_{csw} are flat-bed and side-wall contributions, respectively.

(1) The first contribution is a flat-bed component R_{cfb} that represents the resistance calculated according to the transmission line method [19]: $R_{cfb} = (R_{\square} L_T) / W \coth \times (L_c / L_T)$ with $L_T = (\rho_c / R_{\square})^{1/2}$ being the transfer length, W the device width, L_c the contact length, ρ_c the specific contact resistivity of the silicon/silicide interface and R_{\square} the sheet resistance of the silicon under the contact $R_{\square} = \rho_{si} / (t_{si} - t_{sho})$. As expected R_{\square} depends on the difference between the SOI film thickness t_{si} and the silicide penetration depth t_{sho} for a given silicon resistivity ρ_{si} under the contact.

(2) The second contribution R_{csw} is a side-wall component that appears when the amount of consumed silicon is non-zero: $R_{csw} = \rho_c / (W t_{sho})$.

The inverse of these two resistance components as well as the inverse of the resulting total resistance issued from their association in parallel ($1/R_c = 1/R_{cfb} + 1/R_{csw}$) are reported in Fig. 6. The proposed modeling of the contact resistance gives a remarkable agreement with the simulated variation of the current and transconductance as a function of the silicide penetration depth. Fig. 7 reports the variations of the subthreshold swing and saturated threshold voltage at $V_{DS} = -1.2 \text{ V}$ as a function of the silicide penetration depth. No severe deviation is observed for both structures. However, due to the more important sensitivity to short channel effects already observed in Fig. 2, the conventional MOSFET exhibits a significantly higher subthreshold swing ($\sim 116 \text{ mV/dec}$) with respect to the ALSB-SOI counterpart ($\sim 83 \text{ mV/dec}$).

4.3. Optimization of the S/D to gate spacing

The S/D to gate spacing (W_{spa}) is a very important parameter that strongly influences the series resistances.

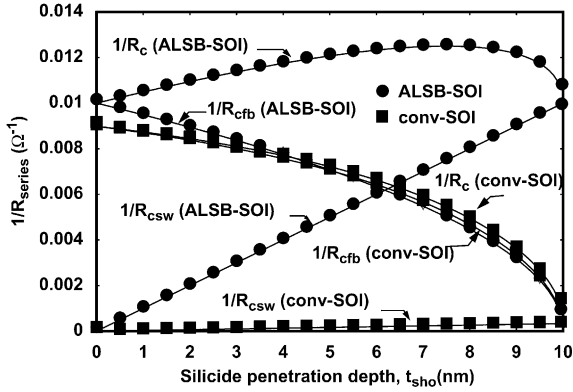


Fig. 6. Variations of the contact resistance as a function of the silicide penetration depth. Results issued from analytical modeling. The total resistance is given by the parallel association of the flat-bed and side-wall components ($1/R_c = 1/R_{cfb} + 1/R_{csw}$).

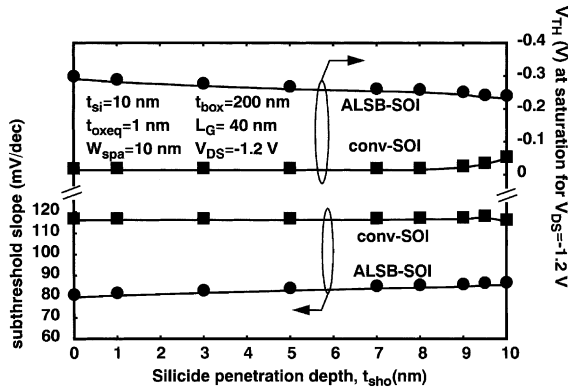


Fig. 7. Simulated variations of the subthreshold swing and of the saturation threshold voltage as a function of the silicide penetration depth. The simulated structures are described in Table 2.

This is specially true in the case of the ALSB-SOI-MOS structure because this spacing corresponds to a low doped region while the same region is highly doped in the conventional structure. When the gate voltage is pushed above the threshold voltage, the field effect induces a band bending that reduces the barrier height that carriers (i.e. holes in the p-MOS case) have to overcome to enter the channel. Fig. 8 shows the typical band curvature (valence band) when the gate voltage is increased (in absolute value) for two different S/D to gate spacing ($W_{spa} = 10$ and 150 nm). Obviously the modulation of source to channel barrier height is a sensitive function of this spacing that needs a careful optimization. Fig. 9 shows the variation of the transconductance as a function of the S/D to gate spacing. As expected, the ALSB-SOI-MOS structure presents a reduced transconductance for large values of W_{spa} because of the important contribution of the corresponding

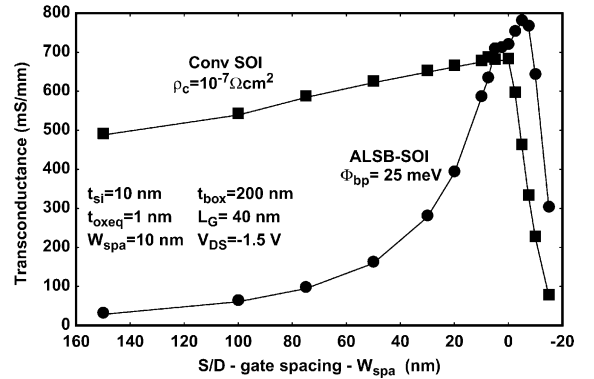


Fig. 9. Variations of the transconductance as a function of the S/D to gate spacing (W_{spa}). Comparison between the ALSB-SOI and the conventional structures.

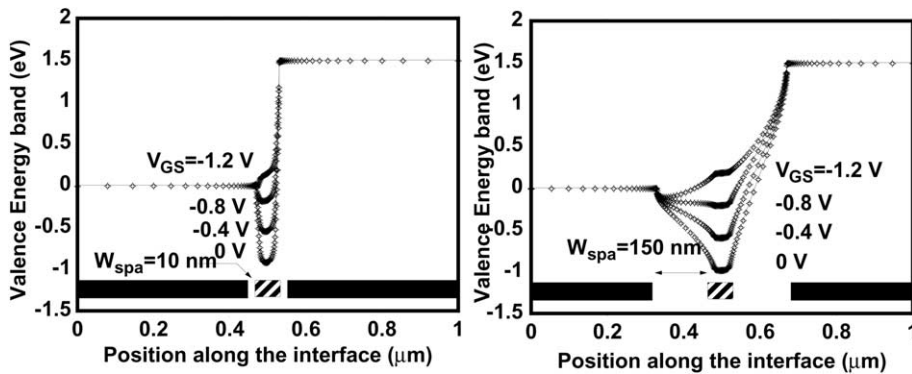


Fig. 8. Typical variations of the valence energy band for the ALSB-SOI-MOS structure with different S/D to gate spacing—left: $W_{spa} = 10$ nm; right: $W_{spa} = 150$ nm ($t_{si} = 10$ nm, $t_{box} = 200$ nm, $t_{oxeq} = 1$ nm, $L_G = 40$ nm, $V_{DS} = -1.5$ V, $C_{SOI} = 10^{15}$ cm⁻³, $\Phi_{bp} = 25$ meV).

series resistance. When the gap between the S/D and gate is reduced, the transconductance of the ALSB-SOI structure rapidly grows up to finally increase beyond the performance of the conventional structure that exhibits a fast roll-off for overlapping S/D and gate electrodes. It is worth noting that a negative W_{spa} value means that the S/D contacts penetrate under the gate. This causes a dramatic decrease of the transconductance that reflects a loss of control by the electric field developed by the gate.

5. Fabrication of low Schottky barriers to holes

As outlined in Section 3, ideal operating conditions are reached for a virtually zero barrier height between the metal contact and the channel in order to minimize the specific contact resistivity. A zero barrier height is generally not desirable when the Schottky contact is fabricated on a bulk substrate because the reverse current flowing into the substrate can reach an unacceptable high level. This remark is not relevant for a thin SOI substrate that provides the necessary isolation. Thus, the ideal operating mode of the ALSB-SOI MOSFET is based on the unique modulation of the source to channel potential barrier by the field effect developed by the gate voltage. If a zero barrier height can be really achieved, the MOSFET current will only be controlled by the gate terminal. If a non zero Schottky barrier exists, the current can be ultimately controlled by the S/D contact resistance when the channel is pushed in strong accumulation. This explains why a very low barrier Schottky contact is necessary to preserve the high current drive of the structure. As already outlined in Section 3, the discussion concentrates on low Schottky barrier to holes (Φ_{bp}) for which experiments have been conducted in the present work. It is worth noting that low Schottky barriers to electrons (Φ_{bn}) can also be obtained based on erbium disilicide [10]. The lowest values of Φ_{bp} reported in the literature generally lie in the 0.2–0.22 eV range for platinum silicide [8,9,20,21] and can reach 0.09 eV for iridium silicide [22]. These experiments have been generally conducted on a n-type substrate in order to keep source and drain junctions in the reverse mode. As the SOI substrate enables the use of a p-type substrate, the present experiments are conducted on a p-type substrate, consistently with an accumulation mode of operation of the ALSB MOSFET.

The choice of Ge/Pt bi-layer that forms a GePtSi silicide is guided by recent observations of Schottky barrier lowering on a crystalline SiGe substrate [23]. It is indeed observed that Φ_{bp} decreases with the Ge fraction x on a strained $\text{Si}_{1-x}\text{Ge}_x$ substrate. The amount of reduction in the barrier height for the metal/ $\text{Si}_{1-x}\text{Ge}_x$ junction with respect to the metal/Si junction was found roughly equal to the valence band discontinuity at the $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ heterojunction. As opposed to the reference

[23], the active layer of the SOI substrate used in this work is silicon and not epitaxial $\text{Si}_{1-x}\text{Ge}_x$. Therefore the choice of a bi-layer of Ge/Pt is motivated by the expected reduction of barrier height that can be obtained by alloying platinum, germanium and silicon. It is worth noting that such a Φ_{bp} barrier reduction using the Ge/Pt bi-layer structure deposited by e-gun evaporation has never been reported in literature. Fig. 10 shows the variations of the Schottky barrier to holes (Φ_{bp}) as a function of the bias. The measured device consists in two back-to-back Schottky diodes that ensure that the current is always limited by one of the reversed biased junction. These data have been obtained from measurements conducted from 300 to 150 K. The barrier height is classically given by the activation energy extracted from Arrhenius plots for several bias conditions (Fig. 11). It can be observed that PtGeSi Schottky contact gives a Schottky barrier as low as 50 meV, a value suitable for high performance ALSB-SOI p-MOSFET [10].

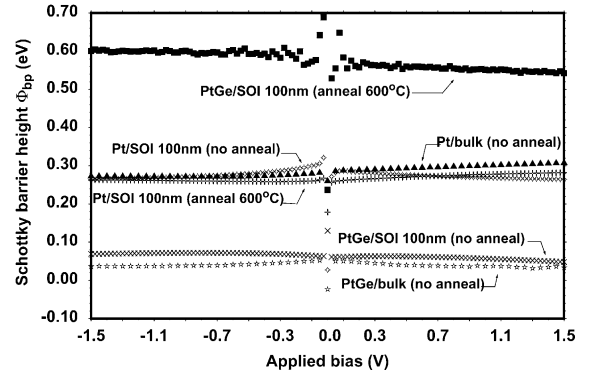


Fig. 10. Schottky barrier to holes (Φ_{bp}) as a function of the applied bias. Contacts realized on a bulk p-type bulk or SOI substrates.

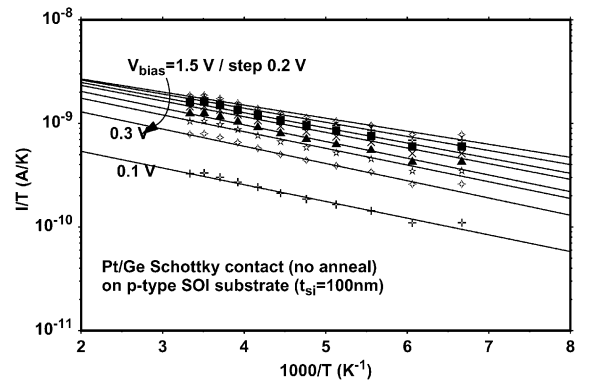


Fig. 11. Typical Arrhenius plot for barrier height extraction (Φ_{bp}) corresponding to Pt/Ge Schottky contacts on p-type SOI substrate ($t_{si} = 100$ nm).

6. Conclusion

It has been shown that the ALSB-SOI-MOS architecture avoids the use of highly doped S/D region while preserving a very low specific contact resistivity. The electrical characteristics of this transistor have been critically analyzed by 2D device simulations. In particular, it has been shown that the silicide penetration into the silicon slightly reduces the contact resistance for the ALSB-SOI MOS structure while it limits dramatically the current drive for the conventional MOS architecture. Experiments have been conducted to show that very low Schottky barriers on p-type silicon can be obtained using Pt/Ge-based stacks.

References

- [1] SIA Semiconductor Industry Association, 'The International Technology Roadmap for Semiconductors—TRS', 1999.
- [2] Ng KK, Lynch WT. Analysis of the gate-voltage-dependent series resistance of MOSFET's. *IEEE Trans Electron Dev* 1986;33:965–72.
- [3] Keys P, Grossmann HJ, Ng KK, Rafferty CS. Series resistance limits for 0.05 μm MOSFETs. *Superlattices Microstruct* 2000;27:125–36.
- [4] Taur Y. 25 nm CMOS design considerations. *IEDM Tech Dig* 1998;(December):789–92.
- [5] Wong HS, Frank DJ, Solomon PM. Device design considerations for double-gate, ground-plane and single-gated ultra-thin SOI MOSFET's at the 25 nm channel length generation. *IEDM Tech Dig* 1998:407–10.
- [6] Pikus FG, Likharev KK. Nanoscale field-effect transistors: an ultimate size analysis. *Appl Phys Lett* 1997;71:3661–3.
- [7] Tucker JR, Wang C, Carney PS. Silicon field-effect transistor based on quantum tunneling. *Appl Phys Lett* 1994;65(5):618.
- [8] Lepselter MP, Sze SM. SB-IGFET: an insulated-gate field-effect transistor using Schottky barriers contacts for source and drain. *Proc IEEE* 1968;(August):1400–2.
- [9] Wang C, Tucker JR. Sub-40 nm PtSi Schottky source/drain metal-oxide-semiconductor field-effect transistors. *Appl Phys Lett* 1999;74:1174–6.
- [10] Kedzierski J, Xuan P, Anderson EH, Bokor J, King TJ, Hu C. Complementary silicide source/drain thin-body MOSFETs for the 20 nm gate length regime. *IEDM Tech Dig* 2000;(December):57–60.
- [11] Osburn CM, Bellur KR. Low parasitic resistance contacts for scaled ULSI devices. *Thin Solid Films* 1998;332:428–36.
- [12] Su LT, Sherony MJ, Hu H, Chung JE, Antoniadis DA. Optimization of series resistance in sub-0.2 μm SOI MOSFET's. *Electron Dev Lett* 1994;15:363–5.
- [13] Tian H, Kim KW, Hauser JR, Masnari NA, Littlejohn MA. Effects of profile-doped elevated source/drain structures on deep-submicron MOSFET's. *Solid-State Electron* 1995;38:573–9.
- [14] Sun JJ, Bartholomew RF, Bellur K, Srivastava A, Osburn CM, Masnari NA. The effect of the elevated source/drain doping profile on performance and reliability of deep submicron MOSFET's. *IEEE Trans Electron Dev* 1997;44:1491–8.
- [15] Sun JJ, Osburn CM. Impact of epi facets on deep submicron elevated source/drain MOSFET characteristics. *IEEE Trans Electron Dev* 1998;45:1377–80.
- [16] Wong HS, Chan KK, Lee Y, Roper P, Taur Y. Fabrication of ultrathin, highly uniform thin-film SOI MOSFET's with low series resistance using pattern-constrained epitaxy. *IEEE Trans Electron Dev* 1997;44:1131–5.
- [17] Schubert P, Neudeck GW. Confined lateral selective epitaxial growth of silicon for device fabrication. *IEEE Electron Dev Lett* 1990;11:181.
- [18] Chan M, Assaderaghi F, Parke SA, Hu C, Ko PK. Recessed-channel structure for fabricating ultra-thin SOI MOSFET with low series resistance. *IEEE Electron Dev Lett* 1994;15:22–4.
- [19] Murmann H, Widmann D. Current crowding on metal contacts to planar devices. *IEEE Trans Electron Dev* 1969;16:1022–4.
- [20] Koeneke CJ, Sze SM, Levin RM, Kinsbron E. Schottky MOSFET for VLSI. *IEDM Tech Dig* 1981:367–70.
- [21] Snyder JP, Helms CR. Experimental investigation of a PtSi source and drain field emission transistor. *Appl Phys Lett* 1995;67:1420–2.
- [22] Misra D, Simhadri VS. A survey of the potential of an IrSi Schottky barrier MOSFET based on simulation studies. *Solid-State Electron* 1992;35:829–33.
- [23] Nur O, Willander M, Turan R, Sardela Jr. MR, Hansson GV. Metal-semiconductor junctions on p-type $\text{Si}_{1-x}\text{Ge}_x$ strained layers. *Appl Phys Lett* 1996;68:1084–6.