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# Wave-mechanical calculations of leakage current through stacked dielectrics for nanotransistor metal-oxide-semiconductor design

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Quantum calculations of leakage current through ultrathin dielectric heterostructures are used to propose design criteria for the next generation of metal-oxide-semiconductor devices in a deep submicron technology. By using as input parameters both the dielectric constant and the barrier height of different dielectrics, including at first stage  $\text{SiO}_2$ ,  $\text{Si}_3\text{N}_4$ ,  $\text{TiO}_2$ , and  $\text{Ta}_2\text{O}_5$ , but also such emerging materials as  $\text{HfO}_2$  and  $\text{ZrO}_2$ , we show that, depending on the voltage range investigated, the hierarchy between those dielectrics is not simply given by the increase of their permittivity. Deeper considerations based on resonant tunneling mechanisms, of prime importance when dielectric heterostructures are used for fabrication purposes, must be taken into account especially for the future low-consumption nanotransistors with operating voltages below 1 V. © 2003 American Institute of Physics. [DOI: 10.1063/1.1544650]

## I. INTRODUCTION

As a consequence of very large scale integration, scaling down the gate length in ultimate metal-oxide-semiconductor (MOS) transistors marks the intersection of several research domains, including materials, technology, and modeling techniques. Within this context, the gate dielectric remains one of the main concerns. New high- $\kappa$  materials, as well as new architectures, have been proposed and tested since classical approaches appear to be unrealistic on a nanometer scale. Indeed, some aspect ratio between gate length and dielectric thickness has to be preserved in order to maintain the control of charge in the device channel. Oxide thickness reduction yields an increase of the gate leakage current and therefore of the static consumption.

According to the *International Technology Roadmap for Semiconductors*,<sup>1</sup> constant adequacy to Moore's law will require oxide thickness of 10 Å around 2010. Now, a maximum in the gate leakage current of  $1 \text{ A cm}^{-2}$ , commonly admitted as a consumption criterion for desktop applications, shows the limitation of  $\text{SiO}_2$  as an insulator gate.<sup>2</sup> Several solutions have been proposed for the next MOS field-effect transistor (MOSFET) generations. Basically, the use of a high-permittivity dielectric allows the thickness to be increased, while maintaining the same control of charge. However, from a technological point of view, the substitution of silicon dioxide by another higher permittivity material is not easy without degrading interface quality. Moreover, among the different candidates, several dielectrics are not thermally stable on silicon. Thus, in most of the MOSFET processes, a

small  $\text{SiO}_2$  layer exists on the silicon surface prior to anything else.

Among the different possible solutions to continue downscaling, a first approach consists of a progressive introduction of impurity atoms (e.g., nitrogen) in a thermal dioxide growing process. This can lead to a  $\text{Si}_3\text{N}_4$  final layer by oxygen substitution.<sup>3</sup> It has been shown that such an oxynitride layer can reduce boron penetration from *p*-type polysilicon gates<sup>4</sup> and thus parasitic currents. Since a greater average permittivity allows us to increase the insulator thickness, the leakage current can be reduced with a constant charge control. Nevertheless, it has been shown that oxynitrides are not able to replace silicon dioxide for thicknesses lower than 13 Å.<sup>5</sup>

A second approach would be the use of high- $\kappa$  dielectrics in a stacked configuration. Such insulator engineering combines three main advantages. First, the excellent  $\text{Si}/\text{SiO}_2$  interface properties can be kept. Second, the stacked configuration brings a solution to the problem of thermal instability on silicon. Finally, the multilayer insulator offers another degree of freedom in the design. Several couples of dielectric layers can achieve the same  $\text{SiO}_2$  equivalent thickness.<sup>6</sup> Therefore, the reduction of leakage current is based on the choice of permittivities ( $\kappa$ ) and barrier heights ( $\Delta E_c$ ) values. Our main topic is to propose some design rules towards an optimized bilayered insulator for future MOSFET generations. Section II describes the quantum model that was developed in order to describe energy states, to perform a transmission energy spectroscopy, and to calculate the current density through stacked dielectrics. A parametric study involving several materials, such as  $\text{Si}_3\text{N}_4$ ,  $\text{Ta}_2\text{O}_5$ , and  $\text{TiO}_2$ , is presented in Sec. III. These materials have been chosen as representative candidates for high- $\kappa$  dielectrics in terms of

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( $\kappa, \Delta E_c$ ) parameters. Nevertheless, new applicants, such as  $\text{HfO}_2$  and  $\text{ZrO}_2$ , whose dielectric parameters are close to  $\text{Ta}_2\text{O}_5$ , will be also considered. In Sec. IV, a discussion, based on quantum considerations, on the competition between different conduction mechanisms (tunneling, resonant tunneling, thermionic, etc.) is given. Section V contains concluding remarks.

## II. NUMERICAL METHOD

The motivation is to give a quantum description of conduction mechanisms through stacked dielectric layers in order to analyze the origins of gate leakage current in nano-MOS transistors. To this aim, we use a one-dimensional code solving jointly Poisson's and Schrödinger's equations. This resolution is applied in the direction perpendicular to the gate. Thus, the simulation domain includes the semiconductor material (here, Si), with or without doping modulation, the different stacked dielectric materials and finally the metal, representing the outer reservoir.

The inputs are the microstructure parameters in terms of thickness, doping concentration in case of semiconductors, dielectric constant, conduction-band edge discontinuities (with reference to a given material) along the operating conditions, notably the applied voltage and the device temperature. The output informations are mainly the current–voltage relationships. In addition, such physical figures as quantum transmissions, envelope wave functions, and current increments can be exploited to analyze more deeply the intrinsic conduction properties.

Compared to other approaches found in literature,<sup>7–11</sup> the numerical tool outlined here does not require any approximation on the potential profile and on energy domains under consideration. Let us mention that it was primarily developed to treat III–V electronic quantum devices as Schottky diodes,<sup>12</sup> HBVs (heterostructure barrier varactors),<sup>13</sup> or RTDs (resonant tunneling diodes).<sup>14</sup> It is a full analysis of the current–voltage relationship, whatever the current origin (tunneling, thermally-assisted tunneling, resonant tunneling, thermionic emission), via the integration over energy of a transmission spectrum times a function describing the balance between filled and empty states in the emitting and collecting regions. Defect-assisted tunneling could be also treated in principle, but will not be considered in the present work.

In practice, our calculation is divided into four steps:

(i) The electrostatic potential is determined in the semiconducting region by solving the Poisson equation under Thomas–Fermi approximation. Any homo- or heterojunction can be simulated. A Dirichlet condition (a fixed potential) is assumed on one side of the simulation domain, which will later be the semiconductor/oxide interface, whereas a Neumann condition (zero electric field) is assumed on the opposite side. The resulting band bending has to be taken into account prior to any current estimation. Besides, in case of accumulation regime, electrons or holes can accumulate in front of the oxide region and form, by space-charge effect, a quasitriangular electrostatic quantum well. The implications of such quantum effects are expected to be comparable to

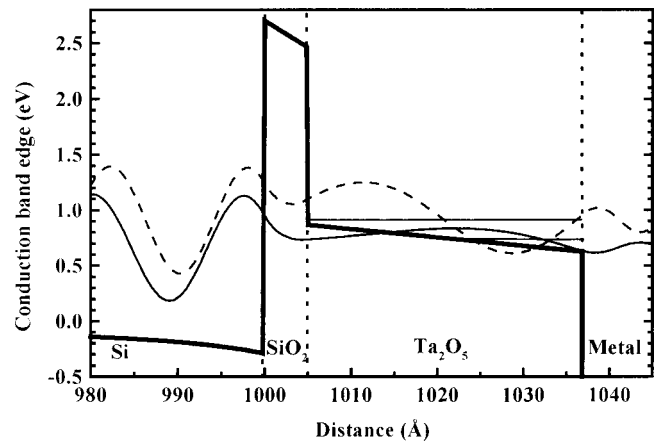


FIG. 1. Potential profile for a  $\text{SiO}_2$  (5 Å)/ $\text{Ta}_2\text{O}_5$  (32 Å) heterostructure at 0.95 V. Also given, the two first wave functions (real part) at  $E=0.81$  and 1.01 eV revealing quantum bound states localized in the  $\text{Ta}_2\text{O}_5$  region bounded on one side by  $\text{SiO}_2$  and on the other by the interface  $\text{Ta}_2\text{O}_5$  metal (virtual confinement wall).

those present in the emitter region of a RTD.<sup>15</sup> At this point, let us note that we have ignored this two-dimensional (2D) gas of electrons to establish the potential using a classical three-dimensional (3D) Fermi distribution. Moreover, using a zero-current Thomas–Fermi approximation, we also neglect the influence of charges responsible for the current on the potential. In previous papers, we have studied in detail the degree of approximation afforded by such assumptions and concluded that, as long as potential is considered (an integrated value), no significant error was made on the potential profile.

(ii) The potential profile has to be determined throughout the structure. To this aim, the electric field is extracted from the previous step at the Dirichlet boundary. As the insulator layers are supposed to be free of charges, the electric field is assumed to be constant for a given dielectric and thus the potential is easily determined. Finally, as a function of the last oxide/metal discontinuity, the Fermi level within the metal is deduced. Compared to the Fermi level reached in the semiconductor assumed at thermal equilibrium on the opposite side of the structure, bias voltage is finally deduced. Here again, induced by the potential drop within the dielectric heterostructure, quantum effects appear due to the semiconductor/dielectric and dielectric/metal heterointerfaces. The oxide region appears as a “cavity” where quasi-bounded states can be evidenced. These energy states induce temporary localization with a sufficient strength to affect dramatically the conduction characteristics as seen in the following.

(iii) The envelope wave functions are calculated for each energy by solving the time independent Schrödinger equation. Different approaches can be used depending on boundary conditions whether open, semi-open, or closed structures are under concern. In our case, we will focus on the ballistic tunnel current issued from the semiconductor region. Thus, we considered an open structure, with the need of plane wave boundaries on each side. As illustrated in Fig. 1, wave functions are calculated at each energy value and can reveal momentary localization within the oxide barrier with a po-

tential form given by the dielectric heterostructure. Here, quantum effects would appear for lower energies than in the pure case of SiO<sub>2</sub>, since barrier heights are generally lowered with other dielectrics. Fowler–Nordheim (FN) regimes or other tunneling assisted mechanisms would then affect conduction properties, and bias voltage ranges when they appear have to be carefully studied when the device design is considered.

(iv) The final step, as wave functions are known, is to derive current–voltage characteristics. Assuming a transmission coefficient calculated by the ratio of the incoming and the transmitted particle current (square of the plane wave amplitude weighted by the local wave vector) and Fermi–Dirac distributions on both sides, a global procedure for each energy is used by integrating the transmission spectra times the so-called “supply function,” which gives the balance between the filled and empty states in the supplying and collecting regions. Details of the procedure can be found in Ref. 12. Here, it is important to notice that no approximation is made depending on energy domains as often done with pure tunnel (in general Wentzel–Kramers–Brillouin approximation), FN regime (triangular barrier) and thermionic (Richardson-type formula) separations. Some effects such as quantum reflection, even for energies higher than any barrier height, are naturally included in our approach.

As a final comment on the numerical procedure, let us mention that the comparison between the different dielectric stacks is sometimes difficult due to the lack of accuracy of material parameters. Moreover, as often mentioned in III–V or IV–IV electronics, the concept of effective mass for such thin layers (a few angstroms) becomes questionable. Nevertheless, such descriptions are easy to handle and give in general physically meaningful results supported by experiments. In order to limit the number of parameters used in the simulation, our calculations have been tested with classical SiO<sub>2</sub> structures with a satisfactory agreement with experimental or previously published current density values and evolutions as a function of bias voltage. Then, to explore other dielectric candidates, only two parameters are chosen to be characteristic of a given material, namely, the dielectric constant  $\kappa$  (considered as the relative permittivity in this article), and the barrier height  $\Delta E_c$  compared to the semiconductor (Si). It will be seen in the following that already with these sole two parameters, conception rules can be drawn for ultimate MOS design.

### III. PARAMETRIC STUDY: OPTIMIZATION OF STACKED LAYERS GEOMETRY

The properties of the major high permittivity dielectrics, which can candidate in stacked layer gates, are presented in Table I.<sup>2,6</sup> Among these materials, Ta<sub>2</sub>O<sub>5</sub> appears like a favorite due to its high- $\kappa$  and well-known properties for memory applications. TiO<sub>2</sub> seems more advantageous in terms of permittivity, but the drawback is a smaller barrier height. Both TiO<sub>2</sub> and Ta<sub>2</sub>O<sub>5</sub> present thermal instability<sup>2</sup> when used directly on Si, which implies the use of a SiO<sub>2</sub> interfacial layer. Recent studies tend to promote the use of HfO<sub>2</sub><sup>16</sup> and ZrO<sub>2</sub><sup>17</sup> mainly in the perspective of a single dielectric layer substitution as these materials are more stable

TABLE I. Reference parameters for gate dielectric materials.

Material	Dielectric constant $\kappa$	Band gap $E_g$ (eV)	Barrier height $\Delta E_c$ (eV) to Si
SiO <sub>2</sub>	3.9	9	3.0
Si <sub>3</sub> N <sub>4</sub>	7.5	~5	2.0
Ta <sub>2</sub> O <sub>5</sub>	~25	~4.4	1.4
TiO <sub>2</sub>	~40	~3.5	1.1
HfO <sub>2</sub>	25	5.7	1.5
ZrO <sub>2</sub>	25	7.8	1.4

on Si. Nevertheless, a real monolayer approach does not seem achievable without compromising the dielectric potential. Therefore, a bilayer approach employing interlayered dielectrics such as SiO<sub>2</sub> or Al<sub>2</sub>O<sub>3</sub><sup>18</sup> is mostly preferable as stability on Si is not the only criterion. It should be noted that concerning HfO<sub>2</sub> and ZrO<sub>2</sub>, barrier height and permittivity are very close to the values reported for Ta<sub>2</sub>O<sub>5</sub> (Table I). We can therefore conclude that our model applied to ZrO<sub>2</sub> and HfO<sub>2</sub> would rather give similar current trends and transmission evolutions as for Ta<sub>2</sub>O<sub>5</sub>. We focused on TiO<sub>2</sub> and Ta<sub>2</sub>O<sub>5</sub> because, although these materials exhibit comparable leakage current around 1-V gate bias, their conduction mechanisms are different and illustrate the role of both barrier height and permittivity as design parameters. In our simulations, we consider metal/TiO<sub>2</sub>/SiO<sub>2</sub>/Si and metal/Ta<sub>2</sub>O<sub>5</sub>/SiO<sub>2</sub>/Si, where the silicon is *n*-type with a doping of 10<sup>17</sup> A/cm<sup>3</sup>. The metal work function is equal to 4.3 eV. Figure 2 depicts the current densities versus voltage [ $J(V)$ ] evolutions for SiO<sub>2</sub>/Ta<sub>2</sub>O<sub>5</sub> and SiO<sub>2</sub>/TiO<sub>2</sub> heterostructures, which are compared to a conventional SiO<sub>2</sub> monolayer and a SiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub> bilayer. The dielectric thicknesses have been calculated to achieve an equivalent oxide thickness  $t_{eq} = 10$  Å following the equation

$$t_{eq} = t_{SiO_2} + \frac{\kappa_{SiO_2}}{\kappa_{high-\kappa}} \times t_{high-\kappa}, \quad (1)$$

where  $t_{SiO_2}$  and  $t_{high-\kappa}$  are the thicknesses of SiO<sub>2</sub> and the high- $\kappa$  dielectric respectively and  $\kappa_{SiO_2}$  and  $\kappa_{high-\kappa}$  are the corresponding dielectric constants.

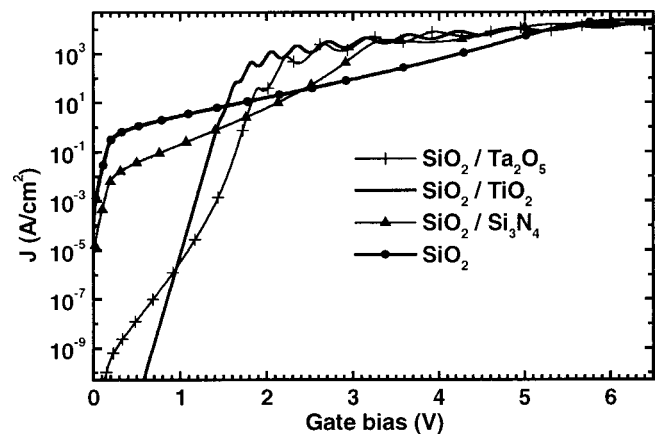


FIG. 2. Tunneling current density as a function of gate voltage for 10 Å pure oxide and for SiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub>, SiO<sub>2</sub>/TiO<sub>2</sub> and SiO<sub>2</sub>/Ta<sub>2</sub>O<sub>5</sub> stacked dielectrics (for  $t_{eq} = 10$  Å).



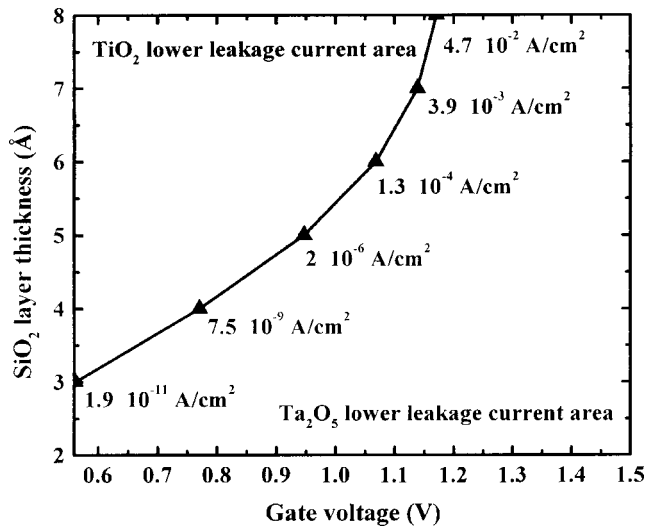


FIG. 3. SiO<sub>2</sub>/TiO<sub>2</sub> and SiO<sub>2</sub>/Ta<sub>2</sub>O<sub>5</sub> stacked-layer tunneling-currents intersections plotted from 2- to 8-Å SiO<sub>2</sub> layer thicknesses (for  $t_{eq} = 10$  Å) versus gate voltage. This curve separates two distinct areas, indicating the best stacked layer to minimize leakage currents following the initial parameters.

In Fig. 2, the SiO<sub>2</sub> interlayer has been fixed to 5 Å. This choice will be commented later. The SiO<sub>2</sub> monolayer ( $t_{ox} = 10$  Å) curve confirms that the 1-A/cm<sup>2</sup> leakage current limit recommended for desktop applications is exceeded for low voltages (around 0.5 V). The SiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub> bilayer shows a rather similar evolution with lower current values, typically one order of magnitude lower with respect to the SiO<sub>2</sub> counterpart around 1 V. For higher voltages, the slope slightly increases which leads to a crossing point before 2.5 V. This behavior is the consequence of the low Si<sub>3</sub>N<sub>4</sub> barrier height (2 eV) to be compared to the 3 eV of SiO<sub>2</sub>. This general phenomenon, common to every stacked structure will be discussed in details in the following section. At first order, all stacked dielectrics chosen here satisfy the roadmap criteria, but because of the weak leakage current margin of Si<sub>3</sub>N<sub>4</sub>, this dielectric is often presented only as a short term candidate comparing to high- $\kappa$  materials. At longer term, other options must be considered.

The high- $\kappa$  based (TiO<sub>2</sub> and Ta<sub>2</sub>O<sub>5</sub>) stacked  $J(V)$  curves depict clearly several typical behaviors. In the following section, the conduction properties associated to each regime will be pointed out. Overall, the Ta<sub>2</sub>O<sub>5</sub>-based bilayer seems more advantageous above 1 V approximately. However, it can be noted that the  $J(V)$  characteristics intersect at 0.95 V and considering the future MOSFET generations scaling parameters, bias voltages below 1 V must be taken into account.<sup>1</sup> Figure 3 shows the evolution of the crossing point as a function of the interlayer thickness. This curve sets a frontier which permits a choice between TiO<sub>2</sub> and Ta<sub>2</sub>O<sub>5</sub> by observing the leakage current. The domain below this curve corresponds to the Ta<sub>2</sub>O<sub>5</sub> lower leakage current area. Inversely, the area favorable to TiO<sub>2</sub> is located above the curve. As predicted, the current decreases with the interlayer thickness because of the low permittivity of SiO<sub>2</sub>. According to the literature, a thickness lower than 5 Å does not seem technically achievable.<sup>2</sup> This means that the TiO<sub>2</sub>-based bilayer leads to the lowest leakage current until the 0.95-V

bias. Because of the great current margins observed for both materials, it would not be reasonable to make predictions for the future technologies from the sole consumption criterion. Nevertheless, these first calculations show that, considering the leakage current amplitude, the choice of a dielectric heterostructure cannot be valid within the whole 0.5–1.5 V range. Other parameters linked to the technological feasibility have to be clearly analyzed.<sup>2</sup> Nevertheless, in order to bring further informations on the degradation mechanisms, a complete understanding of the way current builds up in such stacked structures is necessary. In the following section, we propose such an analysis from a transmission spectroscopy.

#### IV. QUANTUM CURRENT CONTRIBUTIONS IN STACKED LAYERS

In Fig. 2, the quite pure tunneling behavior of the oxide and oxide/nitride  $J(V)$  characteristics can be noted since no pronounced oscillation appears below a 3-V bias. Nevertheless, tunnel current oscillations caused by quantum wave interferences may appear for ultrathin oxide and oxide/nitride gate but for higher voltages.<sup>19</sup> The measurements of the oscillation quasiperiod have been recently used to estimate oxide parameters as, for example, its thickness.<sup>20,21</sup> On the contrary, the weak barrier height of the high- $\kappa$  dielectrics causes the current oscillations to occur just above the 1.5-V gate voltage. For a single layer, these quantum interferences can be modeled by the analytical Airy function approximation (single triangular well). Obviously, in its initial formulation, this approach is not valid for stacked layers due to simultaneous multiple current contributions.

In order to interpret the different current slopes at the 0.95-V crossing, we plotted the quantum transmission probability and the supply function as a function of energy in Fig. 4(a) and the variations of the conduction-band edge versus distance in Fig. 4(b). Due to a weaker barrier height, the peaks in the quantum transmission appear at much lower energy levels for the SiO<sub>2</sub>/TiO<sub>2</sub> stack than for SiO<sub>2</sub>/Ta<sub>2</sub>O<sub>5</sub>. For both stacked layers, the dominant contributions can be roughly divided in several domains while increasing energy.

For SiO<sub>2</sub>/TiO<sub>2</sub>, below 400 meV, the current behavior is dominated by the direct tunneling through the total bilayer thickness. Above 400 meV, direct tunneling through the oxide layer is combined with a FN contribution through the second layer. Resonant levels appear in the quasitriangular quantum well delimited by the TiO<sub>2</sub> conduction-band edge. An alignment of these preferential paths with the concentration of free electrons in the emitting region yields the maxima observed on the transmission evolution. Above 570 meV, the tunneling length is equal to the SiO<sub>2</sub> interlayer thickness.

Conduction through the SiO<sub>2</sub>/Ta<sub>2</sub>O<sub>5</sub> stacked layers is governed by the same mechanisms but FN tunneling appears later since the Ta<sub>2</sub>O<sub>5</sub> barrier is higher. Indeed, the first resonant level is located at 800 meV, as illustrated by the first transmission maximum. For such a high energy level, the number of occupied states is low. Thus, we think that the contribution of this level to the total current will be weak at a 0.95-V bias voltage. As expected by comparing the total

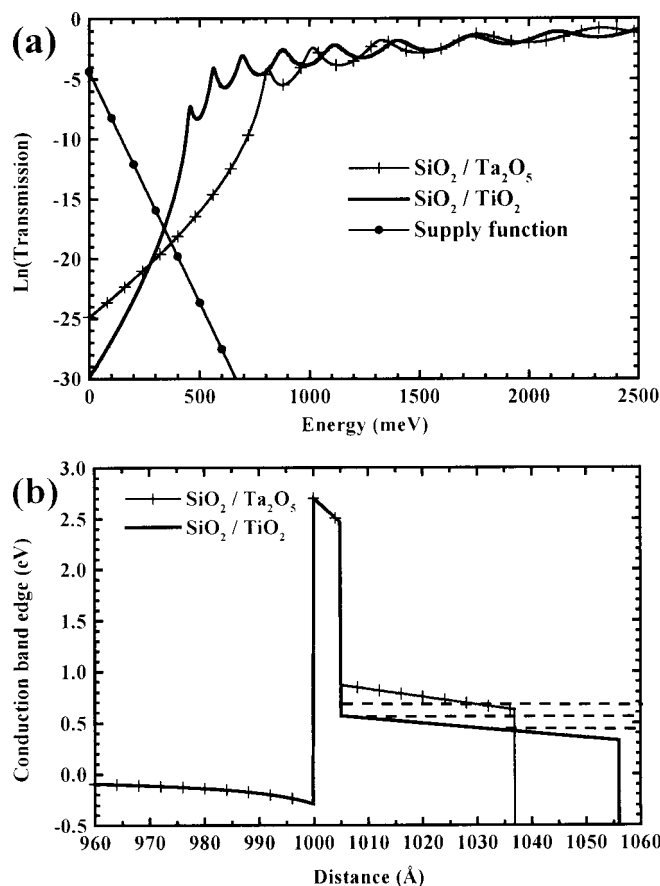


FIG. 4. (a) Quantum transmission probabilities and supply function versus injection energy at 0.95-V bias voltage for  $\text{SiO}_2/\text{TiO}_2$  and  $\text{SiO}_2/\text{Ta}_2\text{O}_5$  stacked layers and (b) spatial variations of the conduction-band edge for the corresponding stacked gates with the first three quantum bound states for the  $\text{SiO}_2/\text{TiO}_2$  heterostructure.

thickness of both high- $\kappa$  stacked structures, the pure tunneling contribution is higher for  $\text{Ta}_2\text{O}_5$  below 300 meV.

For both structures, increasing the supply voltage shifts the transmission peaks towards lower energies. As for a single layer dielectric, the positions of the resonant levels and then the energy offsets in the transmission resonances are governed by the quantum well geometry. Therefore, it strongly depends on the thickness and the slope (i.e., bias voltage and permittivity) of the high- $\kappa$  material triangular barrier.

To quantify the influence of the resonant levels on the total current, we calculated the current increment  $dJ$ .<sup>12</sup> This increment is plotted as a function of energy for increasing bias voltages in Fig. 5. For each curve, the current amplitude has been divided by the maximum value to allow a clear insight into the different conduction mechanisms.

For  $\text{Ta}_2\text{O}_5$ , these curves confirm that the pure tunneling is the dominant phenomenon as illustrated by the monotonous decrease of current values. This decrease follows the supply function variation which models the occupation statistics. However, at 1.44 V, the first resonant level contribution around 400 meV is no more insignificant. This tunneling path shift towards low energy explains the first peak appearance on the corresponding  $J(V)$  characteristic. For  $\text{SiO}_2/\text{TiO}_2$  stacked layer, the major current is governed by a

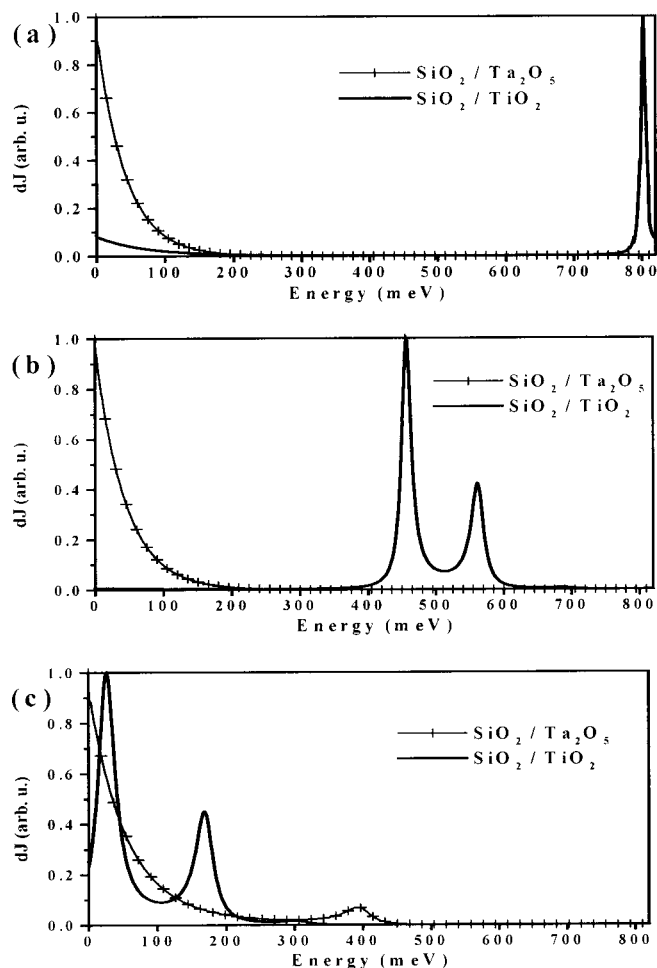


FIG. 5. Current increments of both stacked layers versus energy to illustrate the significant tunneling contributions for increasing bias voltages: (a)  $V_g = 0.54$  V, (b)  $V_g = 0.95$  V, (c)  $V_g = 1.44$  V.

resonant mechanism through several preferential tunneling paths. At 0.44 V, the total current involves a conduction mechanism through a single resonant level and a weak contribution of direct tunneling. At the  $J(V)$  crossing voltage (0.95 V), the pure tunneling becomes negligible, while the resonant effect contribution is shared among two levels. At this voltage, it can be noticed that the scale proportions between the two curves are respected. For the highest voltage (1.44 V), three levels contribute to the total current. The  $J(V)$  oscillations are controlled by the superposition of significant transmission levels with the supply function. For instance, at 1.44 V, we can observe an oscillation in the  $J(V)$  curve due to the presence of a resonant level near the Si conduction-band edge. When this resonant level shifts under the occupied injection states, a  $J(V)$  minimum appears. When increasing bias, the shift of the resonant levels in the supply function window creates the oscillations on the  $J(V)$  characteristic. At this point, it has to be mentioned that from a quantitative point of view, further refinements appear necessary. First of all, even if the conclusions drawn before will remain valid, ideally a 2D treatment of the accumulation layer pronounced effects at increasing voltage should be included. Let us mention also that the optimal parameters deduced for the heterostructure have to be weighted by the fact

that our approach is ballistic. Other contributions induced, particularly by defects, should degrade the calculated current leakage values. Other design criteria including capacitance considerations, which quantum determination is under development, must be added to this first conduction approach.

## V. CONCLUSION

In summary, we have used an approach based on the conduction mechanisms through stacked dielectrics to propose design criteria for the ultrathin insulator of future MOS nanotransistors. The natural trend is to invoke the use of high- $\kappa$  dielectrics to overcome the problem of too thin SiO<sub>2</sub> thicknesses when following the classical downscaling. In the article, we have shown that, the  $\kappa$  value is not a sufficient parameter to decrease the leakage current for a given equivalent barrier width. Among the dielectrics often quoted in the literature, such as TiO<sub>2</sub> or Ta<sub>2</sub>O<sub>5</sub>, at least two parameters have to be taken into consideration, namely, the permittivity and the barrier height, to define what dielectric heterostructure would lower the leakage current. Moreover, this kind of parametric study is of prime importance since the trade-off, and consequently the choice of a material, stands in the expected operating voltage range (below 1 V) of the future generations of MOS devices.

<sup>1</sup>See *The International Technology Roadmap for Semiconductors* (Semiconductor Industry Association, San Jose, CA, 2002), see also <http://public.itrs.net/> for the most recent updates.

<sup>2</sup>G. D. Wilk, R. M. Wallace, and J. M. Anthony, *J. Appl. Phys.* **89**, 5243 (2001).

<sup>3</sup>X. Guo and T. P. Ma, *IEEE Electron Device Lett.* **19**, 207 (1998).

<sup>4</sup>T. Ito, T. Nakamura, and H. Ishikawa, *IEEE Trans. Electron Devices* **29**, 498 (1982).

<sup>5</sup>S. Song, W. S. Kim, J. S. Lee, T. H. Choe, J. K. Choi, M. S. Kang, U. I. Chung, N. I. Lee, K. Fujihara, and H. K. Kang, *Tech. Dig. VLSI Symp.* **2000**, 190 (2000).

<sup>6</sup>J. Zhang, J. S. Yuan, Y. Ma, and A. S. Oates, *Solid-State Electron.* **44**, 2165 (2000).

<sup>7</sup>J. Sune, P. Olivo, and B. Ricco, *J. Appl. Phys.* **70**, 337 (1991).

<sup>8</sup>F. Ranna, S. Tiwari, and D. A. Buchanan, *Appl. Phys. Lett.* **69**, 1104 (1996).

<sup>9</sup>E. M. Vogel, K. Z. Ahmed, B. Hornung, W. Kirklen Henson, P. K. McLarty, G. Lucovsky, J. R. Hauser, and J. J. Wortman, *IEEE Trans. Electron Devices* **45**, 1350 (1998).

<sup>10</sup>E. Cassan, *J. Appl. Phys.* **87**, 7031 (2000).

<sup>11</sup>R. Clerc, G. Ghibaudo, and G. Pannanakis, *Solid-State Electron.* (in press).

<sup>12</sup>F. Podelvin, O. Vanbésien, and D. Lippens, *J. Appl. Phys.* **89**, 6247 (2001).

<sup>13</sup>E. Lheurette, X. Mélique, P. Mounaix, F. Mollot, O. Vanbésien, and D. Lippens, *IEEE Electron Device Lett.* **19**, 338 (1998).

<sup>14</sup>L. Burgnies, O. Vanbésien, V. Sadaune, D. Lippens, J. Nagle, and B. Vinter, *J. Appl. Phys.* **75**, 4527 (1994).

<sup>15</sup>P. Mounaix, O. Vanbésien, and D. Lippens, *Appl. Phys. Lett.* **57**, 1517 (1990).

<sup>16</sup>Z. Xu, M. Houssa, S. De Gendt, and M. Heyns, *Appl. Phys. Lett.* **80**, 1975 (2002).

<sup>17</sup>M. Houssa, V. V. Afanas'ev, A. Stesmans, and M. M. Heyns, *Appl. Phys. Lett.* **79**, 3134 (2001).

<sup>18</sup>C. Zhao, O. Richard, E. Young, H. Bender, G. Roebben, S. Haukka, S. De Gendt, M. Houssa, R. Carter, W. Tsai, O. Van Der Biest, and M. Heyns, *J. Non-Cryst. Solids* (in press).

<sup>19</sup>G. Lewicki and J. Maserjian, *J. Appl. Phys.* **46**, 3031 (1975).

<sup>20</sup>L. Mao, C. Tan, and M. Xu, *Solid-State Electron.* **44**, 1501 (2000).

<sup>21</sup>H. Katto, *Solid-State Electron.* **45**, 101 (2001).