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G. Larrieu, Emmanuel Dubois. Schottky-barrier source/drain MOSFETs on ultra-thin silicon-on-insulator body with a tungsten metallic midgap gate. IEEE Electron Device Letters, 2004, 25, pp.801-803. <10.1109/LED.2004.838053>. <hal-00140981>

HAL Id: hal-00140981

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Submitted on 20 Sep 2024

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Schottky-Barrier Source/Drain MOSFETs on Ultrathin SOI Body With a Tungsten Metallic Midgap Gate

Guilhem Larrieu and Emmanuel Dubois, *Member, IEEE*

Abstract—This letter presents a simple low-temperature process to fabricate Schottky-barrier (SB) MOSFETs that integrates a midgap metallic gate (tungsten). The device architecture is based on a thin (10 nm) and lowly doped silicon-on-insulator film that provides a threshold voltage of -0.3 V independent on the depletion charge and therefore not sensitive to variations in film thickness and doping. A gate encapsulation technique using an SiO_2 -like hydrogen silsesquioxane capping layer features 15-nm-wide spacers and ensures the compatibility with the PtSi self-aligned silicide process. Long-channel devices present an ideal subthreshold swing of 60 mV/dec, over six decades of $I_{\text{on}}/I_{\text{off}}$ without any sign of sublinear upward bending of the $I_{\text{DS}}-V_{\text{DS}}$ curves at low drain voltage.

Index Terms—Metal gate, Schottky-barrier (SB) MOSFET, silicon-on-insulator (SOI).

I. INTRODUCTION

SCHOTTKY-BARRIER (SB) MOSFETs have recently received a renewed interest for the potential they offer to solve end-of-roadmap challenges associated with the source/drain (S/D) architecture [1], [2]. The most important features of the SB design lies in the suppression of highly doped shallow junctions and in the use of low sheet and low specific contact resistances provided by a metallic junction. Additional benefits also include 1) the tight control of the junction abruptness that directly impacts short channel effects and the link series resistance [3]; 2) the reduction of the thermal budget that alleviates issues associated with the integration of a metallic gate; and 3) the opportunity to operate without gate to S/D overlap that minimizes capacitive coupling [2], [4]. Several authors have experimentally demonstrated the use of platinum silicide (PtSi) S/D which remains the most popular contact material for p-type SB MOSFETs because of its very low SB height for holes [5]. For the n-type counterpart, Schottky contacts that present a low barrier to electrons currently use rare earth silicides based on erbium [6]–[8] or ytterbium [9]. In most cases, devices fabricated on bulk silicon exhibit high leakage current either due to sharp junction edges that generates a peak of electric field not controlled by the gate [10] or due

This work was supported by the European Commission through the Source and Drain Architecture for Advanced MOS Technology Project under Grant IST-2000-26475.

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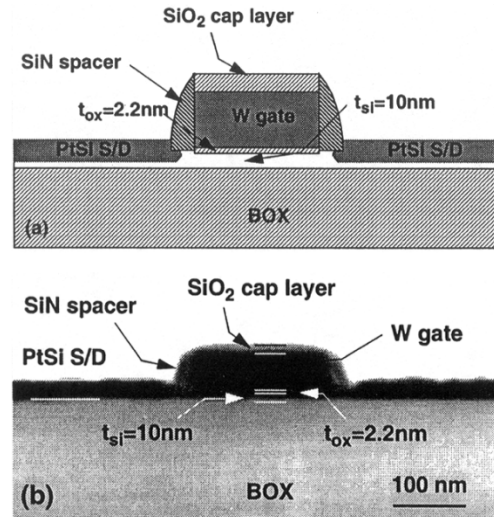


Fig. 1. (a) Schematic representation and (b) TEM cross section of a p-type SB MOSFET with PtSi S/D. This device architecture features a thin 10-nm-thick SOI channel, a 2.2-nm SiO_2 gate oxide, a 40-nm-thick tungsten gate encapsulated by 15-nm-wide SiN spacers at each sidewall and an SiO_2 -like HSQ capping layer on the top.

to subsurface punchthrough as the channel length is scaled down [6], [11]–[13]. The implementation of the SB design on a thin silicon-on-insulator (SOI) substrate was achieved by some other groups to decrease the off-state current I_{off} and the associated subthreshold swing S [7], [14], [15]. Alternatively, a SiGe p-channel was proposed to take advantage of the lower SB height offered by the PtGeSi–SiGe junction to improve the current drive [16]. One common characteristic of the above contributions is the improper scaling of the threshold voltage provided by an n^+ polysilicon gate associated to a lowly doped substrate. More recently, a metallic HfN gate and a 6-nm HfO_2 high- κ gate dielectric [8] was incorporated to the design of a PtSi-based SB p-MOSFET on bulk silicon. This last contribution also points out the difficulty to control the gate to S/D spacing and the integrity of a metallic gate material during the formation of the PtSi S/D contacts using a self-aligned silicide process. In this letter, we successfully demonstrate for the first time the integration of a metallic midgap material in tungsten using a gate encapsulation technique. The fabrication process is developed on a lowly doped p-type thin SOI layer which provides SB p-MOSFETs with ideal long channel current–voltage characteristics and a threshold voltage of -0.3 V compatible with low power operation.

II. DEVICE STRUCTURE AND FABRICATION

Fig. 1(a) gives a schematic representation of the device structure. SOI (100) wafers with resistivity of 14–22 $\Omega \cdot \text{cm}$ are thinned down to a thickness to 10 nm by chemical etching. The channel is MESA-isolated by reactive ion etching (RIE) of the SOI film down to the buried oxide. A 2.2-nm-thick gate oxide is subsequently grown by dry oxidation in O_2 at 725 $^\circ\text{C}$ and a 40-nm tungsten film is deposited by physical evaporation. E-beam lithography is used to define the gate pattern in an inorganic negative-tone resist, namely, hydrogen silsesquioxane (HSQ) [17]. It is worth noting that HSQ does not only present excellent properties for e-beam applications but is also more conventionally known as a low- κ flowable oxide used for backend metal interlayer isolation [18]. Under electron irradiation, HSQ holds the remarkable property to evolve from a cage-like monomer to a network-like polymer that approaches the structure of SiO_2 [17], [19]. Therefore, after patterning the gate by RIE based on an SF_6/N_2 chemistry, the residual HSQ covering the tungsten gate is not removed but used as a capping layer. A 15-nm-thick nitride layer is then deposited by plasma-enhanced chemical vapor deposition to ensure a conformal coverage over the gate. An anisotropic RIE etching step is subsequently used to define 15-nm-wide spacers. According to this process sequence, the two sidewall nitride spacers and the residual HSQ resist on the top ensure a complete encapsulation of the metal gate. Finally, a PtSi self-aligned process is implemented to form the S/D Schottky junctions. After depositing a 5-nm-thick Pt layer, the silicidation reaction is activated by rapid thermal annealing at 300 $^\circ\text{C}$ during 2 min under N_2/H_2 (97%/3%) atmosphere [20]. Fig. 1(b) is a transmission electron microscope (TEM) cross section of a device after process completion. The 10-nm silicon film is nearly fully silicided and the spacing between the gate and the S/D contacts is about 10 nm, which corresponds to the optimum value to efficiently control short channel effects without any degradation of the current drive [21]. Unreacted Pt covering the gate and sidewall spacers is finally etched away using hot diluted aqua regia. The gate encapsulation ensures a perfect protection against this last wet etching step and authorizes a wide choice of gate materials useful to accommodate multiple threshold voltage options [22].

III. RESULTS AND DISCUSSION

Fig. 2 presents the $I_{\text{DS}}-V_{\text{GS}}$ curves obtained on a 2 μm long and 10 μm wide p-MOSFET. Ideal characteristics are obtained with a subthreshold swing close to the low bound of 60 mV/dec at room temperature. The off-state current is maintained in the range of ten pA and the $I_{\text{on}}/I_{\text{off}}$ ratio is greater than 3×10^6 at $V_{\text{DS}} = -1.5$ V. Upward sloping at low V_{DS} has been previously observed for short-channel SB MOSFETs and was invoked as the characteristic signature of a reverse-biased Schottky junction [6], [12], [16]. It was also argued that barrier lowering by the gate field at the source/channel Schottky junction was much less effective in wide geometry transistors, a phenomenon responsible for a severe degradation of the current drive in planar SB MOSFETs [15]. Fig. 3 shows the $I_{\text{DS}}-V_{\text{DS}}$ characteristics measured for the same long and wide geometry ($L = 2$ μm and

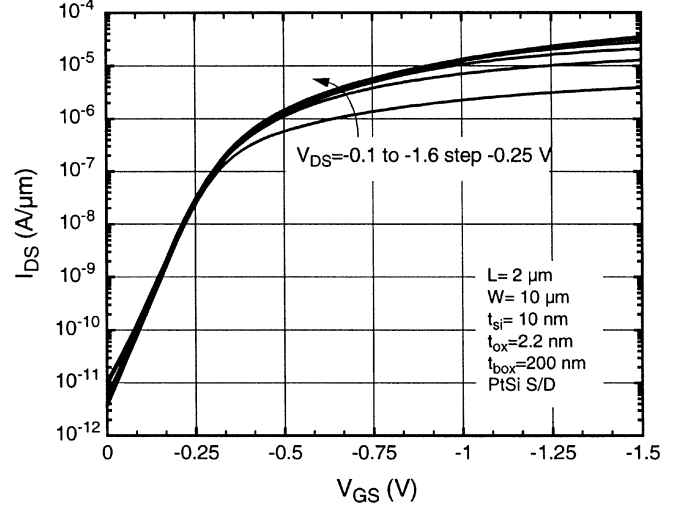


Fig. 2. Measured $I_{\text{DS}}-V_{\text{GS}}$ characteristics (log scale) of a long channel p-type SB MOSFET with PtSi S/D. The gate length L and width W are 2 and 10 μm , respectively. A near ideal subthreshold swing of 62 mV/dec is obtained with an off-state current of 5 pA/ μm .

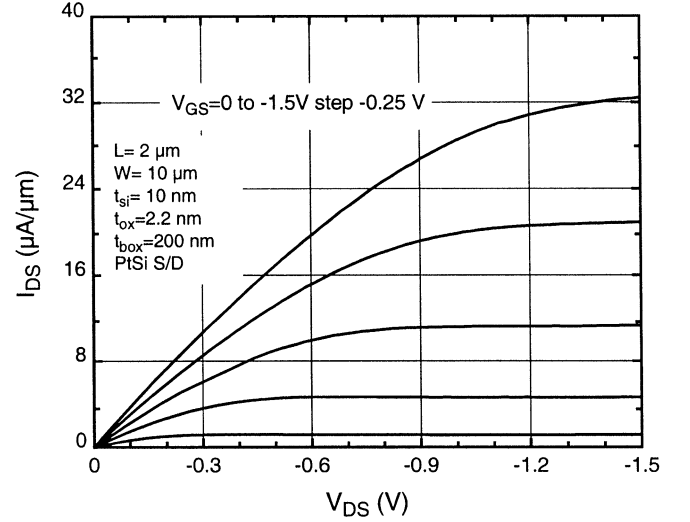


Fig. 3. Measured $I_{\text{DS}}-V_{\text{DS}}$ characteristics of a long channel p-type SB MOSFET with PtSi S/D. The gate length L and width W are 2 and 10 μm , respectively. A current drive of 32.5 $\mu\text{A}/\mu\text{m}$ at $V_{\text{DS}} = V_{\text{GS}} = -1.5$ V is obtained. No sign of sublinear upward bending of the $I_{\text{DS}}-V_{\text{DS}}$ curves at low drain voltage is observed.

$W = 10$ μm). These characteristics are well saturated and no sublinear behavior is observed in the linear regime. An excellent current drive of 32.5 $\mu\text{A}/\mu\text{m}$ is obtained at $V_{\text{GS}} = V_{\text{DS}} = -1.5$ V, about three times larger than that obtained in [8] for a gate length scaled at 2 μm and an equivalent HfO_2 oxide thickness (EOT) of 2 nm (2.2 nm in this letter). In the case of a midgap gate material, the long-channel threshold voltage (V_{TH}) of an accumulation-mode p-MOS on a lowly doped thin SOI body is independent on the depletion charge [23]. In this situation, it can be shown [24], [25] that V_{TH} reduces to a threshold potential $-\phi_T = -(kT/q) \ln(p_T/n_i)$ where p_T conveniently defines the hole concentration at threshold. Fig. 4 shows the $I_{\text{DS}}-V_{\text{GS}}$ characteristics in linear format from which the threshold voltage

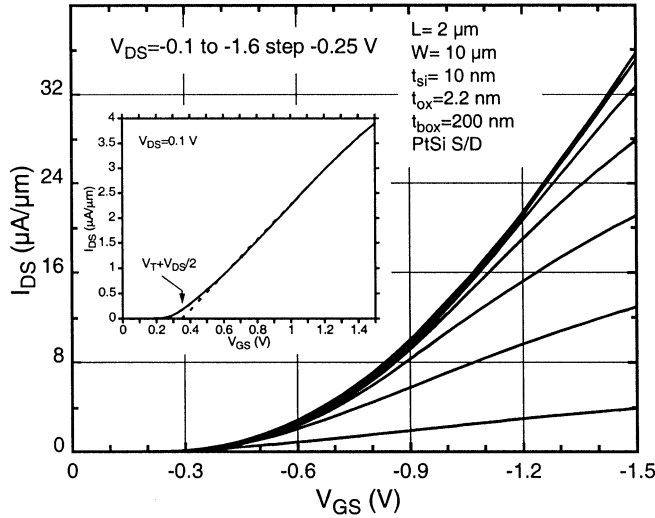


Fig. 4. Measured I_{DS} - V_{GS} (linear scale) characteristics of a long channel p-type SB MOSFET with PtSi S/D. The gate length L and width W are 2 and 10 μm , respectively. The midgap workfunction provided by the tungsten gate gives a threshold voltage of -0.3 V.

is measured at -0.3 V. This value corresponds to a critical concentration p_T around $2 \times 10^{15} \text{ cm}^{-3}$ consistent with previously published results [25].

IV. CONCLUSION

A p-type SB MOSFET that integrates a midgap metallic tungsten gate and PtSi silicided S/D on an ultrathin SOI body has been demonstrated for the first time. The fabrication process features a low thermal budget (300 $^{\circ}\text{C}$) and a gate encapsulation based on a SiO_2 -like HSQ cap layer surrounded by 15-nm nitride spacers. I_{DS} - V_{GS} characteristics exhibit an ideal subthreshold swing, a ratio I_{on}/I_{off} over six decades and an adjustment of the threshold voltage as expected from a midgap gate.

ACKNOWLEDGMENT

The authors would like to thank J. Katcki of the Institute of Electron Technology, IET Warsaw, Poland for performing the TEM cross section.

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