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Transmission electron microscopy of iridium silicide contacts for advanced MOSFET structures with Schottky source and drain

A. Łaszcz^a, J. Kącki^{a,*}, J. Ratajczak^a, G. Larrieu^b, E. Dubois^b, X. Wallart^b

^a Institute of Electron Technology, Al. Lotników 32/46, 02-668 Warsaw, Poland

^b IEMN/ISEN, UMRS CNRS 8520, Avenue Poincaré, Cite Scientifique, BP 69, 59652 Villeneuve d'Ascq Cedex, France

Abstract

The IrSi_x contacts have been used in Accumulated Low Schottky Barrier MOSFET on SOI. An IrSi_x layer is formed as a result of reaction between metal and semiconductor during annealing. The process of silicidation in the Ir/Si/SiO₂/Si structure has been studied by means of cross-sectional transmission electron microscopy (XTEM). The influence of annealing temperatures (300, 600, 900 °C) on silicide formation was analysed. The formation of a thin IrSi_x layer was observed at a temperature as low as 300 °C. In the Ir/Si/SiO₂/Si structure annealed at 600 °C, the Ir atoms are shown to penetrate across the Si layer, causing disturbance of the Ir/Si interface. After annealing at 900 °C large IrSi_x islands were formed in Si. The expansion of the IrSi_x grains in the Si layer was observed. TEM results were correlated with XPS and electrical measurements.

Keywords: Transmission electron microscopy; Photoelectron spectroscopy; Semiconductors; Surfaces and interfaces; Thin films

1. Introduction

In a good accumulated low Schottky barrier-SOI-MOSFET device, the source/drain (S/D) contacts should have a very high barrier to the substrate to reduce leakage current whereas a very low barrier height to the inverted channel to have an unimpeded drain current [1]. In order to alleviate these two conflicting constraints on the barrier height, a thin silicon-on-insulator (SOI) substrate can be judiciously used to eliminate the first requirement [2]. In this context, IrSi-based metallic S/D junctions appear as a very competitive candidate because this silicide demonstrates the lowest known Schottky barrier to holes [3] potentially even more attractive than PtSi-based contacts for the integration of PMOS transistors [2,4].

The Ir–Si phases are formed when Ir is deposited on Si and silicided by subsequent annealing [5]. Petersson et al. [6] reported that at annealing temperatures: 400–600 °C, 500–950 °C and 1000 °C IrSi, IrSi_{1.75} and IrSi₃ phases were formed, respectively. The another compositions of the Ir–Si phase, such as Ir₃Si₅ and Ir₃Si₄ (formed in ultrahigh vac-

uum) have been found by Engström et al. [7] and by Chung and Hwang [8].

One of important issues is the influence of the Schottky barrier contact microstructure on its electrical properties. The differences in Schottky barrier heights depend on phase composition and microstructures of the Ir–Si system [5,9–11]. TEM investigation is very important for technology optimization and understanding the electrical performance of Schottky contact.

The aim of this paper is the investigation of the influence of the annealing temperature on silicidation process in the Ir/Si/SiO₂ contact structure to p-type Si by means of transmission electron microscopy (TEM). Results of TEM observations have been correlated to XPS and electrical measurements.

2. Experimental

The Ir layer was deposited by means of e-gun evaporation on the SOI structure. The thicknesses of the Ir, Si and SiO₂ layers were 15, 100 and 400 nm, respectively. In order to form Schottky contacts the samples were annealed by rapid-thermal-annealing (RTA) process at follow-

ing temperatures: 300, 600, 900 °C for 120 s under N₂ + H₂ (3%).

The process of silicidation in the Ir/Si/SiO₂/Si contact structure has been investigated by means of cross-sectional transmission electron microscopy (XTEM). The TEM specimens were prepared by the method described in [12] and studied in a JEM-200CX transmission electron microscope operating at 200 kV. XPS analysis was carried out on Physical Electronics 5600 spectrometer fitted in a UHV chamber (base pressure 1 × 10⁻¹⁰ Torr). We use a monochromatized Al X-ray source ($h\nu = 1487$ eV) and the detection angle is 45° with respect to the sample surface normal. For depth profile analysis, we use an Ar⁺ ion gun with an ion energy of 1 keV and a beam raster of 5 mm × 5 mm. Concentration profiles are obtained using standard sensitivity factors provided by the manufacturer.

3. Results and discussion

3.1. TEM analysis

A TEM cross-section of an as-deposited Ir/Si/SiO₂ contact to the p-type Si substrate is shown in Fig. 1. The thicknesses of Ir and Si layers are 15 and 100 nm, respectively. Small grains are observed in the Ir layer. The Ir/Si interface is smooth.

During annealing at 300 °C for 120 s between Ir and Si layers a 3 nm thick IrSi_x layer was formed (Fig. 2). Formation of this layer caused decreasing of the thickness of the Ir layer, since a part of the Ir layer was consumed during silicidation process. The thickness of the Ir layer is about 12 nm. Similar studies of a thin IrSi_x layer formed below 500 °C were reported [5,11]. The Ir/IrSi_x and IrSi_x/Si interfaces are smooth.

In Fig. 3a and b TEM cross-sections of the Ir/Si/SiO₂/Si structure annealed at 600 °C for 120 s is shown. At this tem-

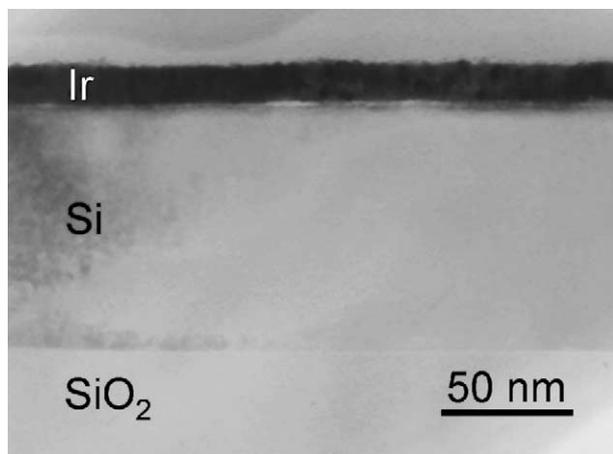


Fig. 1. Cross-sectional TEM view of an as-deposited Ir/Si/SiO₂ contact to the p-type Si.

perature practically the whole Ir layer reacts with silicon, therefore a thick IrSi_x layer is formed. In certain areas the thickness of the IrSi_x layer increases up to a half of the Si layer thickness. In this case a grained structure of the silicide layer becomes visible. Due to the fact that silicide penetration depth into silicon is considerable in certain regions, the IrSi_x/Si interface is very uneven.

At 900 °C the silicidation process is more intense than at lower temperatures (Fig. 4a and b). The tendency of the IrSi_x layer to expand into the Si layer, visible even at 600 °C, enables IrSi_x grains to consume the whole thickness of the Si layer and touch the SiO₂ interface, which prevents further growth. The growth is also limited by the small quantity of deposited Ir. In certain areas there is not enough Ir at the surface, therefore, islands are created (IrSi_x grains separated by silicon) after all Ir atoms reacted with silicon.

According to Petersson et al. [6] and Ohdomari et al. [10] one can expect that at 300 °C the IrSi phase is formed while at temperatures 600 and 900 °C the IrSi_{1.75} phase can be expected.

3.2. Electrical characterisation

Electrical measurements of Ir-based silicide contacts have been carried out to determine the annealing conditions that provide the lowest Schottky barrier to holes and, therefore

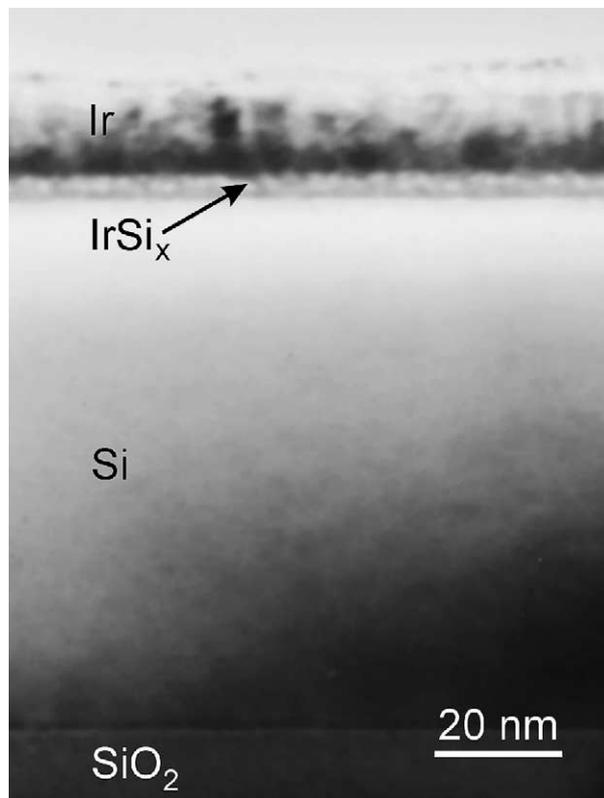


Fig. 2. TEM cross-section of the Ir/Si/SiO₂/Si structure annealed at 300 °C for 120 s.

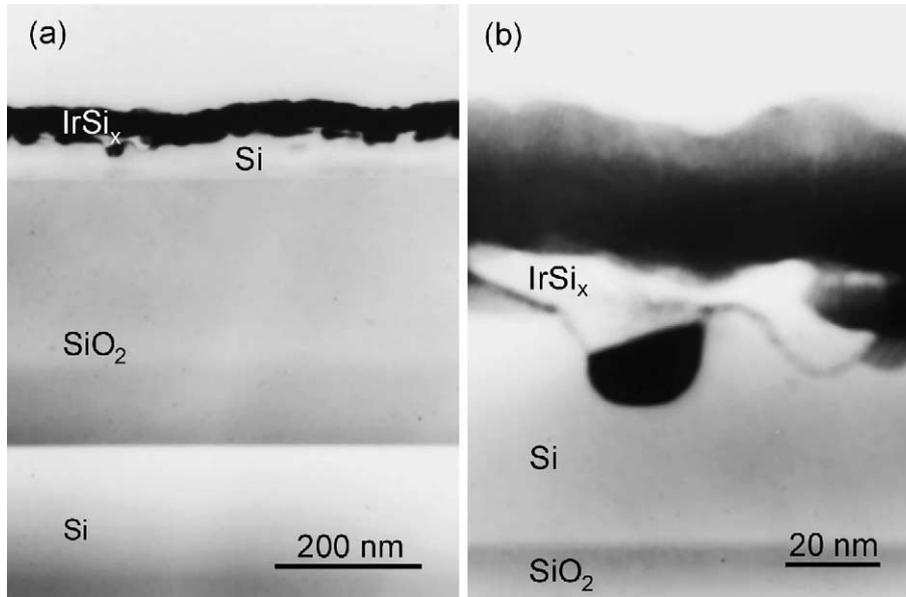


Fig. 3. (a, b) Cross-sectional TEM views of the Ir/Si/SiO₂/Si structure annealed at 600 °C for 120 s.

the lowest specific contact resistance that characterizes the carrier transport through the silicide/silicon interface. The maximum current drive capability as defined in [4] has been extracted from current–voltage characteristics measured in the 170–300 °K temperature range. This information is reported in Fig. 5 for different annealing conditions. Surprisingly, the silicide compound formed at ambient temperature exhibits a significant current drive. The best electrical performance is obtained at the annealing temperature of 300 °C. For thermal treatments realized at higher temperatures (600–900 °C), a severe decrease of the current performance is observed in conjunction with the increase of size of silicide grains and in direct relation with the degradation of the Ir–Si interface in terms of smoothness and homogeneity.

3.3. XPS analysis

In order to investigate the interfacial layer, an XPS depth profile was recorded on the sample annealed at 300 °C. Fig. 6 gives the Si and Ir concentration depth profiles depending on the chemical environment of each element. The Ir4f profile can be decomposed into two Ir4f(IrSi_x) and Ir4f(Ir) contributions. The corresponding deconvolution basis of spectra shows that the Ir4f spin-orbit doublet exhibits a chemical shift of 0.3 eV from 60.7 to 61 eV relevant to the elemental Ir and IrSi_x emission lines, respectively. This result is also consolidated by the concomitant chemical shift of the Si2p emission line. Using a basis of two Si2p spectra centered around 99.2 eV for Si2p(Si) and 99.65 eV for Si2p(IrSi_x), the original Si2p profile can also be deconvolved into two

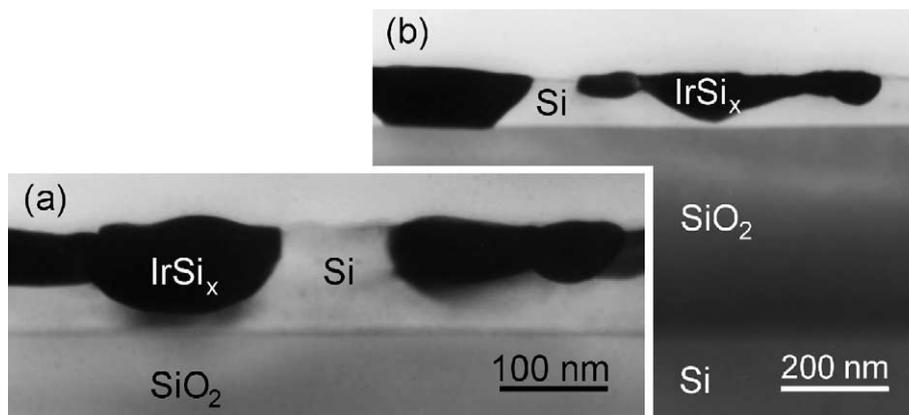


Fig. 4. (a, b) TEM cross-sections of the Ir/Si/SiO₂/Si structure annealed at 900 °C for 120 s.

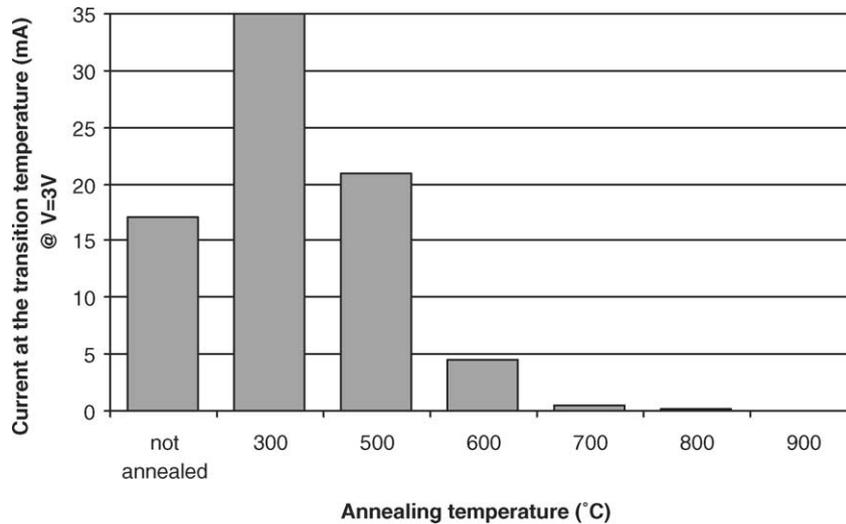


Fig. 5. Electrical characterisation of IrSi-based silicide contacts obtained at different temperatures (not annealed and RTA annealing at 300, 500, 600, 700, 800 and 900 °C). The best current drive is obtained at an annealing temperature of 300 °C. The current performance is directly connected to the smoothness and homogeneity of the IrSi/Si interface confirmed by TEM analysis.

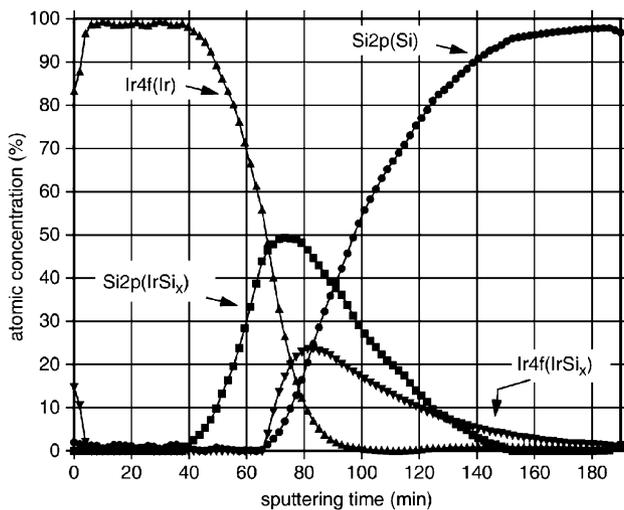


Fig. 6. XPS analysis of the IrSi silicide layer obtained by a 300 °C annealing during 120 s. Atomic concentration profiles obtained from the Si2p and Ir4f photoemission lines after deconvolution to determine the chemical environment of each specie. The original Si2p depth profile is deconvoluted into its Si2p(IrSi_x) and elemental Si2p(Si) contributions. The original Ir4f depth profile is deconvoluted into its Ir4f(IrSi_x) and elemental Ir4f(Ir) contributions. The analysis clearly indicates the formation of an IrSi_x compound also confirmed by the TEM analysis of Fig. 2.

contributions that indicate the formation of IrSi_x silicide-like bonds. On the other hand, the presence of a continuous IrSi_x silicide layer at the Ir/Si interface appears consistent with the TEM analysis presented in Fig. 2.

4. Conclusion

The intensity of the reaction of silicidation process depends on annealing temperature. Annealing at 300 °C causes

a partial reaction between Ir and Si, resulting in the formation of a very thin IrSi_x layer. At the temperature of 600 °C the entire Ir layer is consumed in silicidation reaction. Annealing at 900 °C causes the formation of IrSi_x islands in Si.

It is demonstrated that the best electrical performance is obtained at an annealing temperature of 300 °C for which TEM analysis reveals a continuous and regular layer of IrSi_x clearly identified by XPS experiments.

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