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Measurement of low Schottky barrier heights applied to metallic source/drain metal–oxide–semiconductor field effect transistors

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This article investigates the extraction of low Schottky barrier heights in the perspective of integration of metal–oxide–semiconductor field effect transistors (MOSFET) with a metallic source/drain. A test structure composed of two back-to-back junctions is proposed to characterize materials with a low Schottky barrier. To complete the proposed measurement setup, particular attention is placed on a Schottky transport model that continuously combines thermionic emission, field emission, and barrier lowering due to image charge. In the case of platinum silicide (PtSi) contact, it is shown that Arrhenius plots can be accurately reproduced over a wide range of temperature and applied bias. A consolidation of the measurement strategy and of the associated transport model is also performed through measurements and simulations on a long channel *p*-type Schottky barrier silicon-on-insulator MOSFET with PtSi source/drain. A excellent agreement between simulated and experimental current-voltage characteristics is obtained for a zero-field barrier height of 0.14 eV consistent with the value (0.145 eV) that best fits the Arrhenius plot measured on test structures. The corresponding bias-dependent effective barrier height in the 0.11–0.12 eV range is therefore confirmed at the device level. © *2004 American Institute of Physics.* [DOI: 10.1063/1.1756215]

I. INTRODUCTION

Among the main difficulties to overcome toward the 10 nm gate length metal–oxide–semiconductor field effect transistor (MOSFET), many challenges are associated with the source/drain (S/D) regions. The tight constraints of dopant activation to achieve very highly doped junctions, extremely steep lateral profiling, low contact specific resistance have motivated a renewed interest in MOSFET's architectures that integrate Schottky S/D. The advantage of this design is that roadblocks associated with the control of S/D doping for short gate geometries are inherently solved.[1] Recent publications[2,3] have outlined the need for extremely low Schottky barriers (~0.1 eV) to obtain current drives that compete with highly doped S/D MOSFETs. Platinum silicide (PtSi) presents a typical barrier height to holes around 0.22–0.25 eV.[4–7] According to the literature reporting on the integration of PtSi Schottky *p*-MOSFET, typical values of ϕ_{bp} also lie in the 0.20–0.25 eV range when PtSi S/D are considered.[8–14] However, there remains some controversy on the relevance of this parameter to quantify the current drive capability in a real Schottky-barrier (SB) MOSFET. One major difficulty comes from the fact that most test structures use a single Schottky junction associated in series with an Ohmic contact. In that case, it may be difficult to discriminate between the resistances associated with each terminal. To circumvent this problem, an experimental structure with two identical Schottky contacts is desirable. In addition, the localization of the contacts in close proximity on the same surface properly accounts for the lateral configuration of S/D in a MOSFET. Finally, as tunneling effects can significantly enhance current injection when lateral transport takes place, the extracted barrier height should be considered as an effective parameter whose significance goes beyond the pure thermionic view. This article investigates the extraction of low Schottky barrier heights in the perspective of SB-MOSFET integration. After a brief description of the SB-MOSFET architecture in Sec. II, a critical discussion of conventional experimental techniques used for Schottky barrier extraction is presented in Sec. III. An original test structure composed of two back-to-back Schottky junctions is described in Sec. IV in order to alleviate problems associated with other experimental setups. Because the barrier extraction is tightly connected to the physics of current injection, Sec. V summarizes the main features of a transport model that accounts for thermionic (TE) and field emission (FE). In Sec. VI, a validation of the measurement strategy and transport model is proposed with a particular emphasis on the contributions of both injection mechanisms. Finally, results obtained on the PtSi test structures are consolidated by the electrical characterizations and simulations of a long channel *p*-type SB-MOSFET (Sec. VII).

II. BACKGROUND

A schematic representation of a Schottky S/D MOSFET on a silicon-on-insulator (SOI) substrate is given in Fig. 1. As in a conventional MOSFET with implanted source/drain (S/D), one junction operates in forward mode (drain) while the other is biased in reverse mode (source). The principle of operation is illustrated in Fig. 2: the top graph corresponds to an off-state condition for which the additional body barrier

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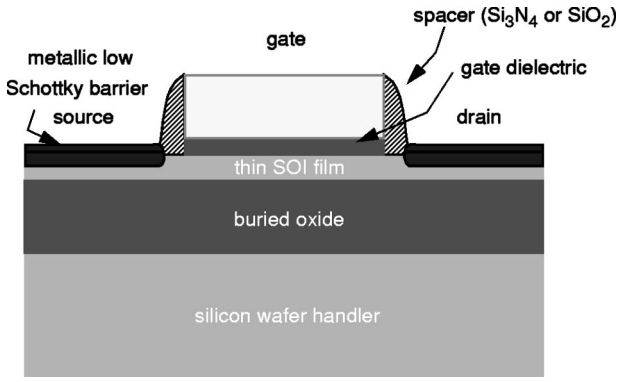

FIG. 1. Schematic representation of a MOSFET that integrates a low Schottky barrier source/drain.

created by the field effect developed by the gate prevents any current from flowing between source and drain. In the bottom graph (on-state), the body barrier disappears and the remaining Schottky barrier is thinned due to the strong band bending at the top silicon/oxide interface. In the latter case, both thermionic and field emission contribute to current injection in the channel. It is worth noting that the ideal operating mode of the Schottky-barrier (SB) MOSFET is based on the unique modulation of the source to channel potential barrier by the field effect developed by the gate voltage. If a zero Schottky barrier height really can be achieved, the MOSFET current will ultimately be controlled by the body barrier generated by the gate terminal. If a nonzero Schottky barrier exists, the current can be controlled by the S/D contact resistance when the channel is pushed in strong accumulation. This explains why Schottky contacts with a very low barrier are necessary to preserve a high current drive in this type of device architecture.

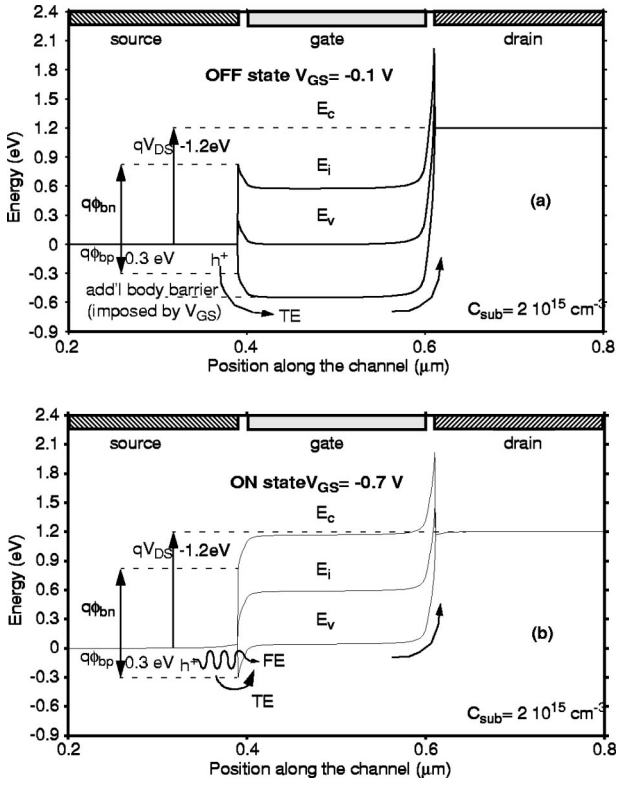

FIG. 2. Band bending along the interface in a *p*-type SB-MOSFET. The Schottky barrier to holes $\phi_{bp}=0.3$ eV is intentionally chosen large to clearly show the band deformation at the vicinity of the Schottky barrier on the source side. (a) The top graph shows band bending in the off state: only a negligible thermally activated current can flow due to a large and deep barrier (ϕ_{bp}+body barrier). (b) A negative bias applied to the gate induces a strong band bending when the transistor is in the on state: both thermionic and field emission contribute to carrier injection in the channel.

III. LIMITATIONS OF MEASUREMENT METHODS OF LOW SCHOTTKY BARRIERS

Four major techniques are widely used for the characterization of Schottky barrier heights: the capacitance voltage, the current voltage, the activation energy, and the photoelectric methods.[4,15,16] However, when a low barrier Schottky contact is associated with a weakly doped substrate as it is the case in SB-MOSFETs, the accurate determination of the barrier height becomes a challenging problem. In this specific case, four major limitations are associated with the aforementioned experimental techniques.

(i) As illustrated in Fig. 3(a), a moderately low Schottky barrier to holes (here, $\phi_{bp}=0.3$ eV) leads to a flat band configuration at equilibrium for which depletion is not observed. It is worth noting that an even lower Schottky barrier (e.g., <0.2 eV), useful for SB-MOSFET applications, would lead to an accumulation regime at the vicinity of the Schottky contact. This operating mode precludes the use of the capacitance-voltage method because the depletion regime is not valid at low reverse bias.

(ii) A significant thermionic current is emitted over the low Schottky barrier under reverse bias. Figure 3(b) shows that holes with energy E_F in the metal have to overcome a low barrier (ϕ_{bp}) to contribute to the reverse current. Under this condition, forward and reverse currents have comparable orders of magnitude [Fig. 3(c)] while several decades of difference are generally observed for midgap barriers ($\phi_{bp}\sim 0.6$ eV). A significant conduction current is therefore superimposed on the displacement current related to the capacitive effect. This current combination often precludes a correct, useful, and accurate determination of the Schottky capacitance that, in turn, makes the capacitance-voltage method questionable for low Schottky barrier measurements. The high level of reverse current is also an issue when internal photoemission measurements (IPE) are considered. Moreover, the square root of photocurrent yield established by Fowler theory becomes superlinear for low values of the Schottky barrier.[4]

(iii) A major obstacle to the accurate determination of a low Schottky barrier lies in the series combination of the silicon resistance of the weakly doped substrate with the Schottky junction. In a first-order estimation, the equivalent Schottky resistance under low bias condition is given by

$$R_{\text{Schottky}}=\left(\frac{\partial I}{\partial V}\right)^{-1}=\frac{k}{SqA^{*}T}\exp\left(\frac{q\phi_b}{kT}\right), \tag{1}$$

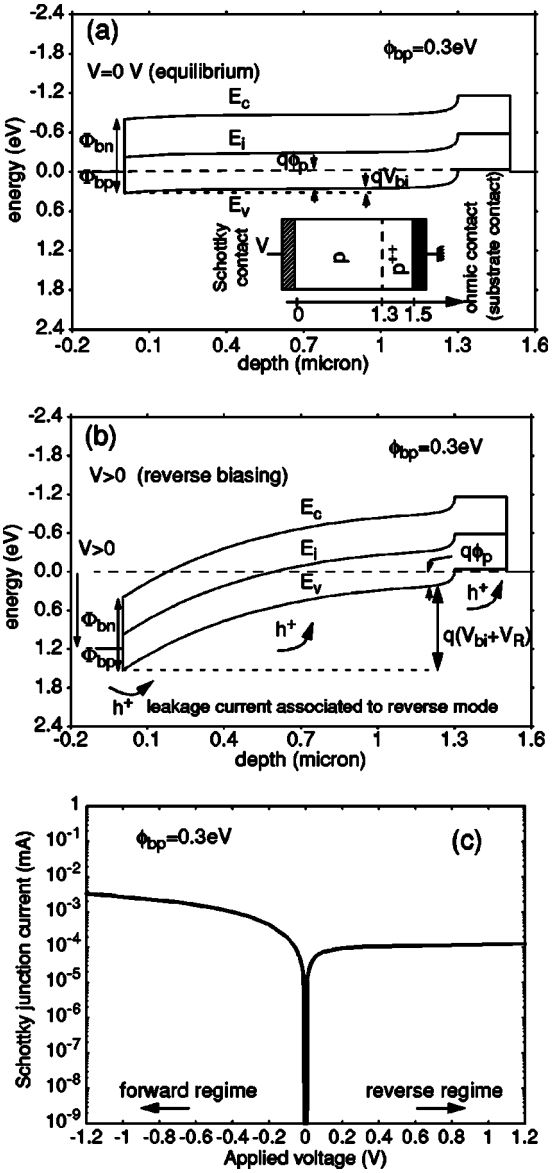

FIG. 3. Calculated band bending for a Schottky barrier on a *p*-doped substrate. The Schottky barrier to holes $\phi_{bp}=0.3$ eV remains representative of a relatively low barrier (a) at equilibrium, the depletion condition is not fulfilled; (b) under reverse bias, the low Schottky barrier to holes enables a large reverse current; (c) current-voltage characteristic.

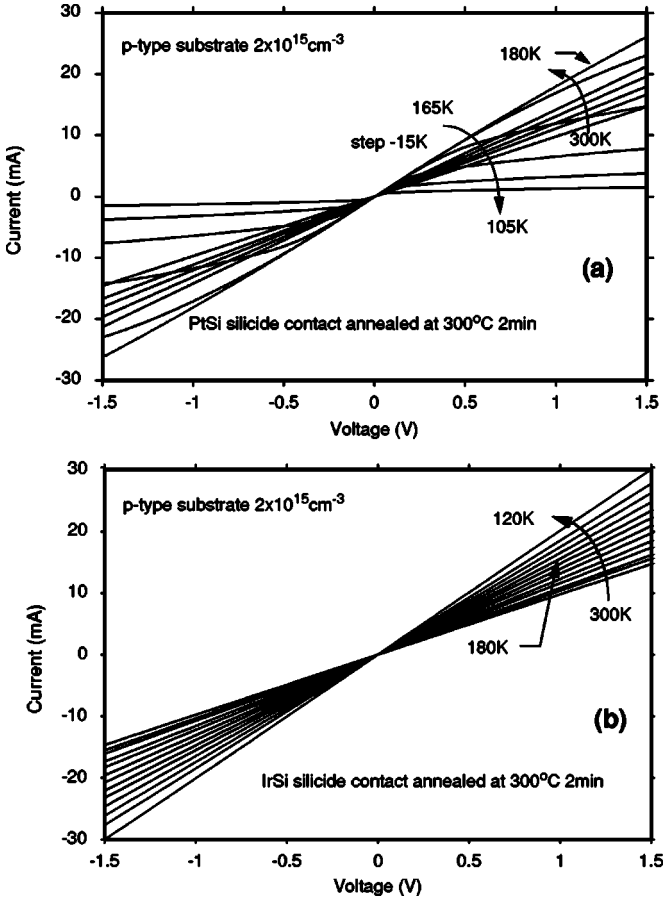

FIG. 4. Current-voltage characteristics of two silicide systems for a varying temperature: (a) PtSi silicide; (b) IrSi silicide.

where ϕ_b is the Schottky barrier, A^* the effective Richardson constant, and S the surface of the junction. This relationship clearly shows that the equivalent Schottky resistance exponentially decays for a decreasing ϕ_b and an increasing temperature T. When the silicon series resistance is orders of magnitude greater than R_{Schottky}, the extraction of the Schottky barrier becomes difficult and inaccurate. This issue mainly affects methods based on current-voltage and activation energy techniques. Figure 4 gives an excellent illustration of this effect. For a moderately low Schottky barrier that characterizes PtSi silicide, the current-voltage characteristics are linear from 300 to 180 K when the silicon series resistance limits the current drive. In this temperature range, the current increases with decreasing temperature consistently with the temperature dependence of the silicon series resistance. Below 165 K, the rectification effect is clearly observed together with an exponential decay of the current with decreasing temperatures consistent with the Schottky law. In contrast, for a very low Schottky barrier height, IrSi silicide in this case, the rectifying effect is never observed down to a temperature of 120 K, indicating that the current-voltage characteristic is always governed by the series resistance. It is also pointed out that the current-voltage characteristics of both silicide systems are the same in the high temperature range above 200 K. This consolidates the interpretation according to which the silicon series resistance R_{Si} governs the observed Ohmic behavior at high temperature. In the present case, $R_{\text{Si}}(T)$ is accurately described by the following expression with $R_{\text{Si}}(300)=98\Omega$ and $\alpha=1.5$:

$$R_{\text{Si}}(T)=R_{\text{Si}}(300)\cdot(T/300)^{\alpha}. \tag{2}$$

(iv) Finally, the last issue is related to the nature of the current transport mechanisms that involve a complex combination of thermionic emission and field emission.[17–20] As a direct consequence, the slope of the $\ln(J_R/T^2)-1/T$ Arrhenius plot does not necessarily reflect the barrier height associated with a pure thermionic current. In order to illustrate this particular

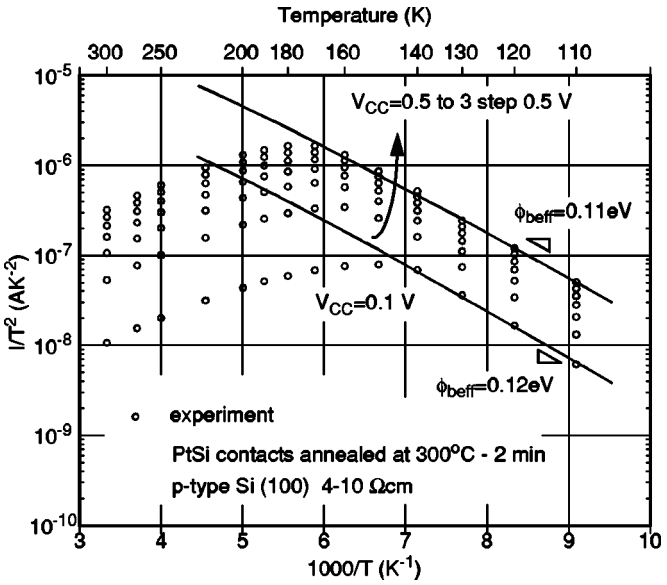

FIG. 5. Arrhenius plot of two back-to-back Schottky junctions. The activation energy extracted from the low temperature section of the graph is representative of the effective Schottky barrier height. The upward shift of the curves with increasing bias indicates that a tunneling current contribution adds to the thermionic one.

point, Fig. 5 shows the Arrhenius plot of PtSi silicide Schottky junctions on a weakly doped *p*-type substrate (4–10 Ωcm) annealed at 300 °C.[21] The effective Schottky barrier to hole extracted from the low temperature portion of the graph typically lies between 0.11 and 0.12 eV depending on the applied reverse bias. This range significantly differs from the commonly accepted values around 0.22–0.25 eV.[4–14] Also, the separation of the curves with the applied bias indicates that an additional current contribution is superimposed to the thermionic one. Because the related current excess is found to be weakly dependent on temperature, tunneling is invoked as the responsible mechanism.

IV. STRATEGY OF SCHOTTKY BARRIER MEASUREMENT AND CHOICE OF A TEST STRUCTURE

As outlined in Sec. II, the characterization method of the Schottky barrier should account for the final application that is targeted, i.e., a Schottky contact MOSFET. This implies important characteristic features for the metal–semiconductor system.

(i) the silicon substrate should be weakly doped;
(ii) the Schottky barrier height should be as small as possible to approach a specific contact resistance close to that of an Ohmic contact; and
(iii) current transport takes place between two identical Schottky contacts corresponding to the source and drain terminals.

In order to meet the above prescriptions as closely as possible, the following experimental conditions have been used:

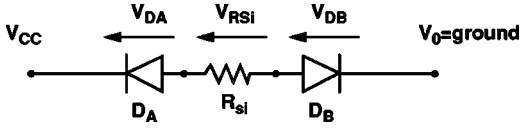

FIG. 6. Equivalent lumped circuit corresponding to two back-to-back Schottky diodes (D_A and D_B) separated by the silicon series resistance R_{Si}.

(i) measurements are conducted on a lowly doped silicon substrate (2×10^{15} cm^{-3});
(ii) Schottky contacts are based on platinum silicide (PtSi); and
(iii) in order to reproduce the lateral configuration of the source/drain contacts of a MOSFET, measurements are performed between two Schottky contacts. This configuration has the advantage to eliminate any contribution of parasitic resistances associated with another type of metal–semiconductor interface (e.g., Ohmic contact at the back side of the sample). The lumped equivalent circuit corresponds to two back-to-back Schottky diodes separated by the series resistance of silicon (Fig. 6). When an external voltage source is applied on one circuit terminal (the other terminal contact being grounded), one Schottky junction is forward biased and the second one operates in reverse mode. Because the forward current increases exponentially with the (forward) applied voltage, this configuration ensures that the measured current is representative of the reverse biased junction provided that the silicon series resistance is negligible.

The most suitable measurement method associated with the proposed test structure remains the activation energy technique because it does not necessitate any assumption on the electrically active area. This last feature is very attractive for the study of metal–semiconductor interfaces because the geometric area is not necessarily representative of the electrical surface of injection. In order to reduce the voltage drop through the silicon series resistance, reverse mode operation is directly obtained from the electrical setup displayed in Fig. 6. Under this condition, the reverse current I_R flowing in one of the junctions can be expressed in a form suitable for extracting the barrier from an Arrhenius plot

$$\ln\left(\frac{I_R}{T^2}\right)=\ln(SA^*)-\frac{q(\phi_{b\,\mathrm{eff}})}{kT}, \tag{3}$$

where $\phi_{b\,\mathrm{eff}}$ stands for the effective Schottky barrier height that may include contributions due to tunneling and barrier reduction related to image charge induction.[4] Figure 7 represents the temperature dependence of the voltage drop across each element of the circuit for different applied voltages. For a low temperature, the total applied voltage matches the voltage drop across the reverse biased junction D_A, indicating that the current flowing through the circuit is limited by this Schottky contact. As the temperature increases, the voltage drop across the silicon series resistance increases up to a point corresponding to the transition temperature for which the external bias is equally distributed across D_A and R_{Si}. From the above discussion, the extraction procedure is there-

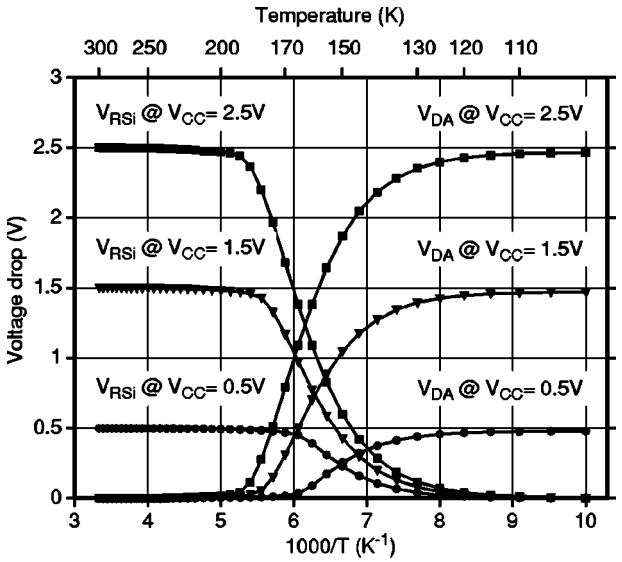

FIG. 7. Calculated voltage drop across the reverse biased Schottky junction D_A and across the silicon series resistance R_{Si} for different applied voltage V_{CC}.

fore based on low temperature and reverse mode for which the silicon sheet resistance is negligible and the current amplitude is much lower than in forward mode. Figure 8 shows the barrier height of Pt–Si Schottky junctions on a weakly doped *p*-type substrate (4–10 Ωcm) submitted to various thermal treatments that determine the formation of different silicides. The Schottky barrier height to holes depends on the annealing conditions as expected from the successive formation of Pt_xSi, Pt_2Si, and PtSi compounds.[21] However, the measured effective barriers ranging from 0.11 to 0.18 eV suggest that the usual thermionic emission prescription as given by Eq. (3) also sustains current contributions due to tunneling.

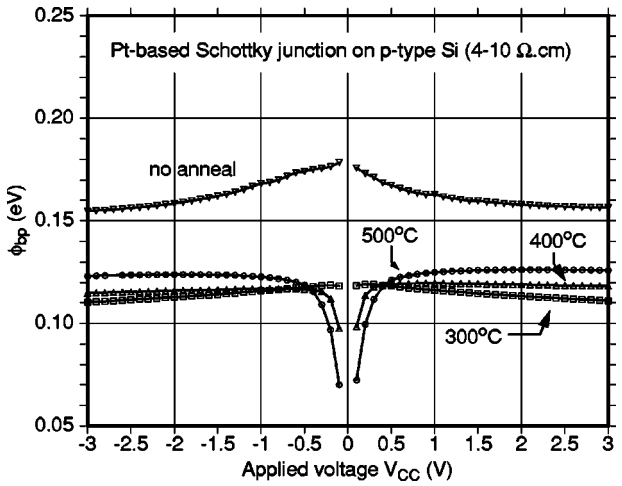

FIG. 8. Voltage dependence of the effective Schottky barrier to holes measured on Pt–Si Schottky junctions. The extraction of ϕ_{bp0} is based on an activation energy method performed at low temperature and in reverse mode.

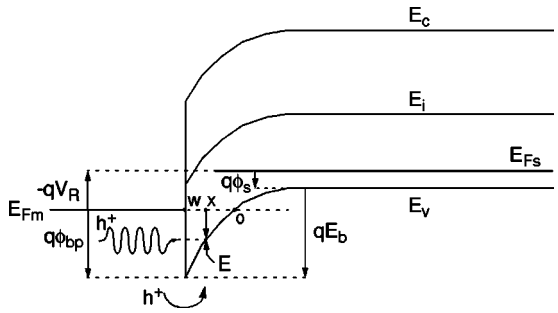

FIG. 9. Band bending at Schottky interface for a reverse bias. This diagram is representative of hole tunneling with energy E crossing the barrier at location x. When $E>E_b=q(\phi_b-\phi_s+V_R)$ thermionic emission is enabled.

V. CURRENT TRANSPORT MODEL

In an attempt to accurately describe the current-voltage characteristics of Schottky junctions for varying temperatures, it is widely recognized that tunneling of carriers at energies lower than the full barrier height can lead to current that is comparable to or even exceeds thermally activated transport over the barrier.[22] While the original papers by Padovani, Stratton, and Summer[18–20] are referenced in most publications that deal with thermionic field emission, the Crowell and Rideout's approach hold the advantage to provide a smooth and continuous transition from a pure field emission to a pure thermionic emission transport mechanism.[17] Following their approach, the total thermionic-field emission (TFE) reverse current density J_R calculated under the WKB approximation can be expressed as

$$J_R=J_{R0}\left[1+\frac{E_b}{kT}\int_0^1 \exp\left\{\frac{-E_b}{kT}\left[\alpha-1+\frac{kT}{E_{00}}y(\alpha)\right]\right\}d\alpha\right], \tag{4}$$

where $E_b=q(\phi_{bp}-\phi_s+V_R)$ is the band bending in the semiconductor region as shown in Fig. 9. The model is presently described for a *p*-type silicon and essentially considers transport of holes. Therefore, ϕ_{bp} represents the Schottky barrier to holes, $q\phi_s$ is the separation between the Fermi level and the valence band, and V_R the reverse voltage applied to the junction. In the last expression, J_{R0} corresponds to the reverse saturation current of pure thermionic emission (TE)

$$J_{R0}=A^*T^2\exp\left\{\frac{-q\phi_{bp}}{kT}\right\}. \tag{5}$$

Of particular significance is the parameter E_{00}, which is a property of the semiconductor through its dielectric constant ε_s, the effective mass of holes m_h^*, and the doping level N. The ratio kT/E_{00} for a given temperature gives a measure of the dominant current flow mechanism: for $kT/E_{00}\sim 1$, field emission dominates, while for $kT/E_{00}\gg 1$ thermionic emission is the most significant mode of current transport

$$E_{00}=\frac{qh}{4\pi}\left[\frac{N}{m_h^*\varepsilon_s}\right]. \tag{6}$$

Finally, the function $y(\alpha)$ results from the transformation of the integration of thermionic/tunneling integral over distance into one over energy.[17] It is defined by

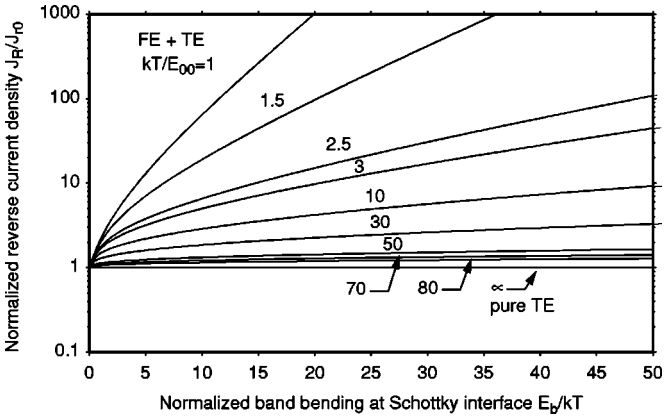

FIG. 10. Normalized reverse current as a function of the normalized band bending. A large ratio kT/E_{00} indicates that current is governed by TE, while a small value of the same ratio indicates that tunneling dominates (FE).

$$y(\alpha)=(1-\alpha)^{1/2}-\alpha\ln\left[\frac{1+(1-\alpha)^{1/2}}{\alpha^{1/2}}\right]. \tag{7}$$

Figure 10 presents the variations of the reverse current J_R normalized by J_{R0} as a function of the normalized band bending at the Schottky interface E_b/kT. This graph consolidates the fact that the ratio kT/E_{00} is the parameter that determines whether field emission is involved in current transport through the barrier. It is worth noting that the reverse current is a fast-growing function with a decreasing kT/E_{00} ratio, leading to a current enhancement of several, decades.

In the above expressions of the current equations, the Schottky barrier to holes should be corrected to account for the image charge induction:[4]

$$\phi_{bp}=\phi_{bp0}-\Delta\phi_{bp}=\phi_{bp0}-\left(\frac{q^2}{8\pi^2\varepsilon_s^3}NE_b\right)^{1/4}. \tag{8}$$

For the sake of completeness, the net current density J due to the tails of thermally excited distributions of carriers in the semiconductor and in the metal is given by the difference between the forward J_F (silicon to metal) and the reverse current J_R (metal to silicon) flows

$$J=J_F-J_R=J_R\left(\exp\left(\frac{-qV_R}{kT}\right)-1\right). \tag{9}$$

VI. APPLICATION TO PtSi SCHOTTKY JUNCTIONS

In order to evaluate the accuracy of the transport model for a Schottky junction as described by Eqs. (4) to (9), the equivalent circuit of Fig. 6 must be solved to determine the current dependence as a function of temperature and applied bias V_{CC}. In that way, it becomes possible to simulate the complete experimental setup composed by the two back-to-back Schottky junctions separated by the silicon series resistance which was defined in Sec. IV. The calculation is performed by solving the set of equations issued from the expression of the Kirchhoff law at each node of the lumped circuit. The resulting 4×4 numerical system is highly nonlinear and is resolved using a conventional Newton–Raphson procedure. Electrical measurements have been conducted on

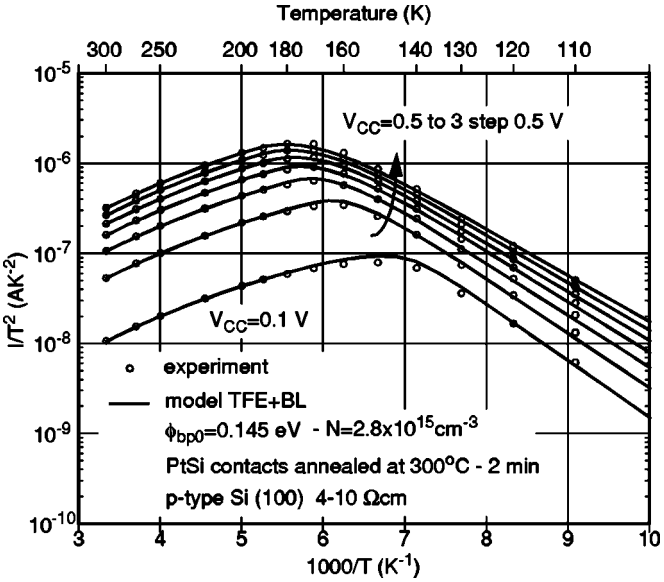

FIG. 11. Experimental and calculated Arrhenius plot using the thermionic field emission (TFE) transport model including barrier lowering (BL) due to image charge induction. Optimum model parameters are $\phi_{bp0}=0.145$ eV, $N=2.8\times10^{15}$ cm^{-3}, $R_{\mathrm{Si}}=98\ \Omega$, and $\alpha=1.5$.

platinum silicide (PtSi) Schottky contacts separated by a micrometer gap to reproduce the lateral source/drain configuration of SB-MOSFET as prescribed in Sec. IV. PtSi was obtained by a 2 min anneal performed at 300 °C in forming gas (97% N_2–3% H_2). Details on sample preparation, XPS, and TEM characterizations of the obtained silicide contacts can be found in Ref. 21. Figure 11 presents a comparison between the simulated Arrhenius plot with optimal parameters and the experimental reference presented in Fig. 5. The complete model (TFE+BL) provides a remarkable agreement with experimental data over the whole interval of temperature and bias ranging from 300 to 110 K and 0.1 to 3 V, respectively. It is worth noting that a very limited number of parameters is needed to reproduce the physics transport in the proposed experimental setup. First, the silicon series resistance $R_{\mathrm{Si}}(300)=98\ \Omega$ and the power coefficient $\alpha=1.5$ of Eq. (2) are easily extracted from current voltage curves in the high temperature section of the graph. The other two parameters to adjust are the zero-field Schottky barrier to holes ϕ_{bp0} and the exact doping concentration N at the silicide/silicon interface that can differ slightly from the corresponding wafer specification (4–10 Ωcm) due, for instance, to segregation and outdiffusion effects. The optimization of these two parameters has been performed using a nonlinear least-squares technique under the constraint of Ref. 23. The minimum and maximum bounds of ϕ_{bp0} and N were reasonably set to 0.1–0.30 eV and 5×10^{14}–10^{16} cm^{-3}, respectively. The resulting calculated optimum parameters are $\phi_{bp0}=0.145$ V and $N=2.8\ 10^{15}$ cm^{-3}. In order to quantify the impact of the field emission and barrier lowering mechanisms, Fig. 12 shows the simulated Arrhenius plots when the transport model is incomplete and hierarchically incorporates (a) thermionic emission only without any barrier lowering effect (TE only); (b) thermionic field emission without barrier lowering, due to image charge (TFE only); and (c) ther-

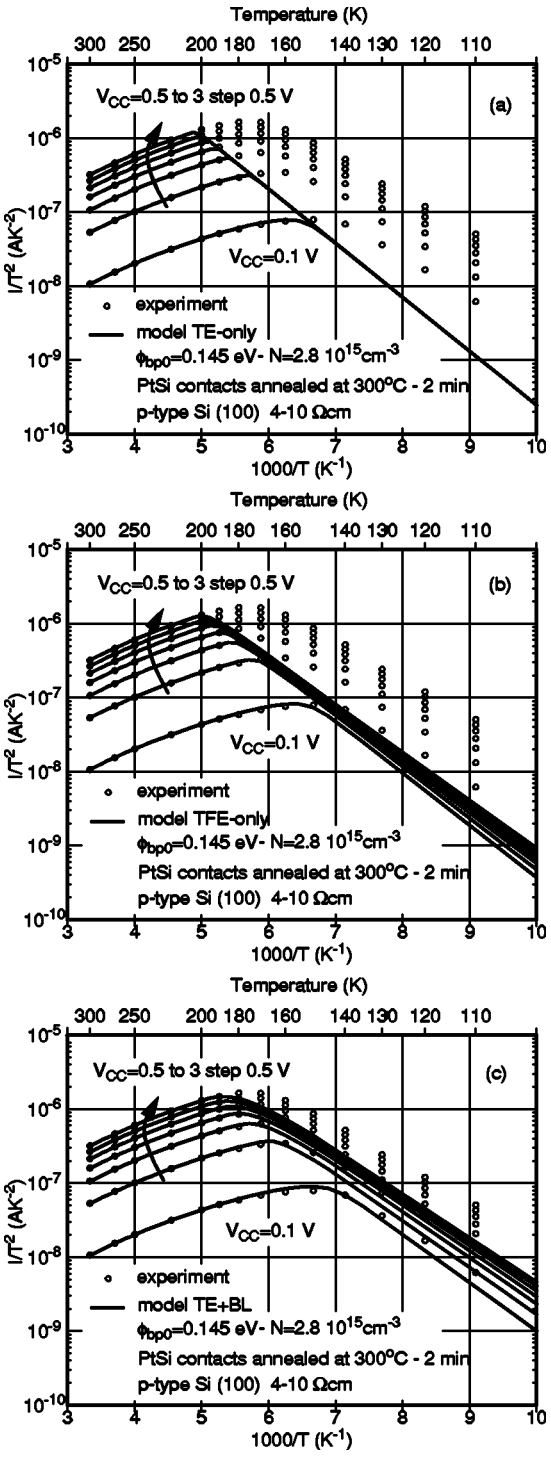

FIG. 12. Experimental and calculated Arrhenius plot using hierarchically the following transport models: (a) thermionic emission (TE only); (b) thermionic field emission (TFE only); (c) thermionic emission with barrier lowering due to image charge (TE+BL). Model parameters are $\phi_{bp0}=0.145$ eV, $N=2.8\times10^{15}$ cm^{-3}, $R_{\mathrm{Si}}=98\ \Omega$, and $\alpha=1.5$.

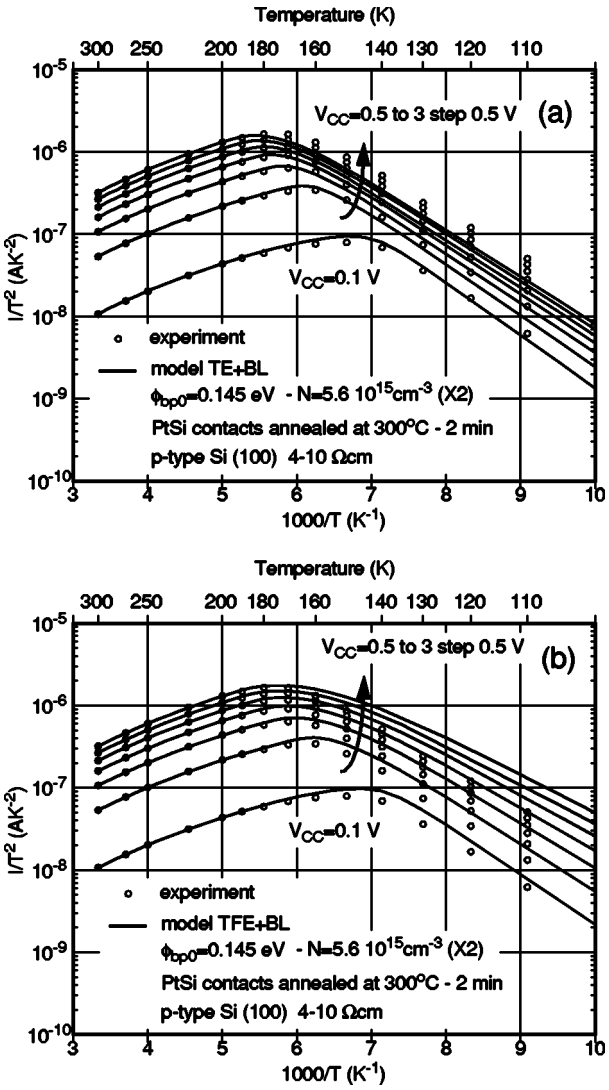

FIG. 13. Impact of a 2X increase of the silicon doping level. Experimental and calculated Arrhenius plot: (a) thermionic emission with barrier lowering due to image charge (TE+BL); (b) thermionic field emission with barrier lowering due to image charge (TFE+BL). Model parameters are $\phi_{bp0}=0.145$ eV, $N=5.6\times10^{15}$ cm^{-3}, $R_{\mathrm{Si}}=98\ \Omega$, and $\alpha=1.5$.

mionic emission with barrier lowering (TE+BL). Because the high temperature section of the Arrhenius plots is governed by the Ohmic behavior of the series resistance R_{Si}, an excellent agreement is again obtained with high temperature experimental data. In the low temperature range, the TE-only model leads to a convergent set of curves that does not exhibit any dependence on the applied bias. The extracted activation energy consistently corresponds to the barrier ϕ_{bp0} that was set to the optimized value of 0.145 eV. The TFE-only version of the model includes tunneling and therefore exhibit a moderate increase of current with bias. The low doping concentration only moderately impacts the tunneling probability. For instance, at 110 K and for $N=2\times10^{15}$ cm^{-3}, the ratio kT/E_{00} is of the order of 30, which leads to a current increase by a factor 2–3 consistently with Fig. 10. Finally, the TE+BL version of the model qualitatively improves the situation through the effect of the barrier lowering mechanism that increases with the effective band bending according to a 1/4 power law. The calculated slope also better matches the experimental one, but the bias dependence of the current remains poorly described. To summarize, beyond the introduction of barrier lowering by image charge, it clearly appears that field emission is also essential to correctly describe the mechanism of current injection in a Schottky junction. To consolidate this view, Fig. 13 indicates

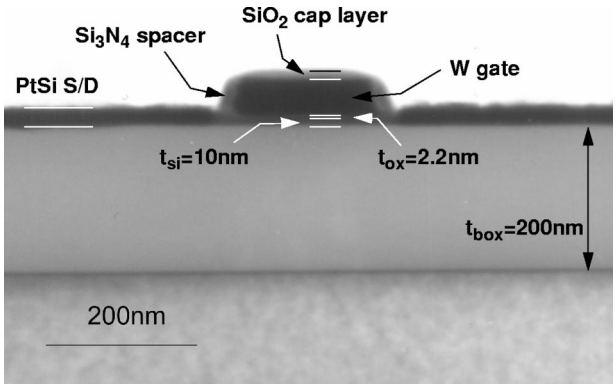

FIG. 14. TEM cross section of *p*-type SB-MOSFET with PtSi S/D. This device architecture features a thin, 10 nm thick SOI channel, a 2.2 nm SiO_2 gate oxide, a 40 nm thick tungsten gate encapsulated by 15 nm wide Si_3N_4 spacers at each side wall, and a deposited SiO_2 capping layer on the top.

the impact of a 2X increase in doping level (5.6×10^{15} cm^{-3}) with ϕ_{bp0} fixed to 0.145 V as previously. According (a) to the TE+BL version of the model, the I/T^2 curve simulated at a low V_{CC} voltage of 0.1 V closely matches the experimental one, indicating that BL coupled to TE could be a sufficient ingredient to properly account for the physics of transport in a low barrier Schottky junction. However, the spacing between curves at higher voltage is not correctly reproduced. In the second case (b), the full model TFE+BL exhibits a clear overestimation of both the current level and curve separation with applied bias when the doping concentration is not finely tuned. Thus, in this last case, the excess of current with respect to the measured one essentially comes from an augmented contribution of field emission which exponentially depends on doping through the tunneling probability.[24]

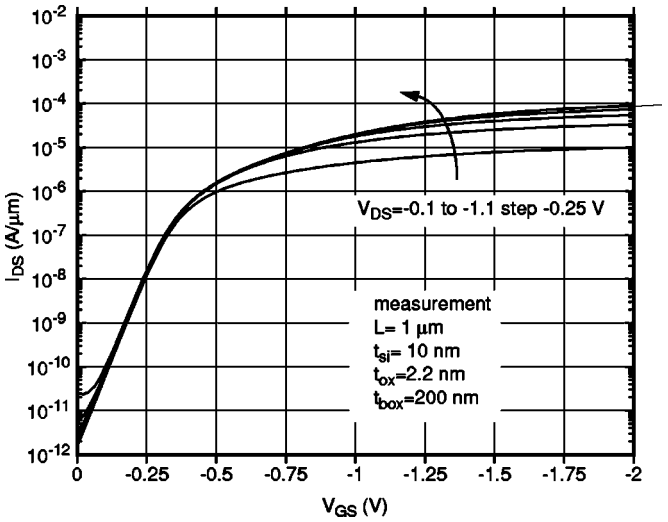

FIG. 15. Measured I_{DS}-V_{GS} characteristics of a long channel *p*-type SB-MOSFET with PtSi S/D. The gate length L and width W are 1 and 10 μm, respectively. A near-ideal subthreshold swing of 62 mV/dec is obtained. The midgap work function provided by the tungsten gate gives a threshold voltage of 0.37 V.

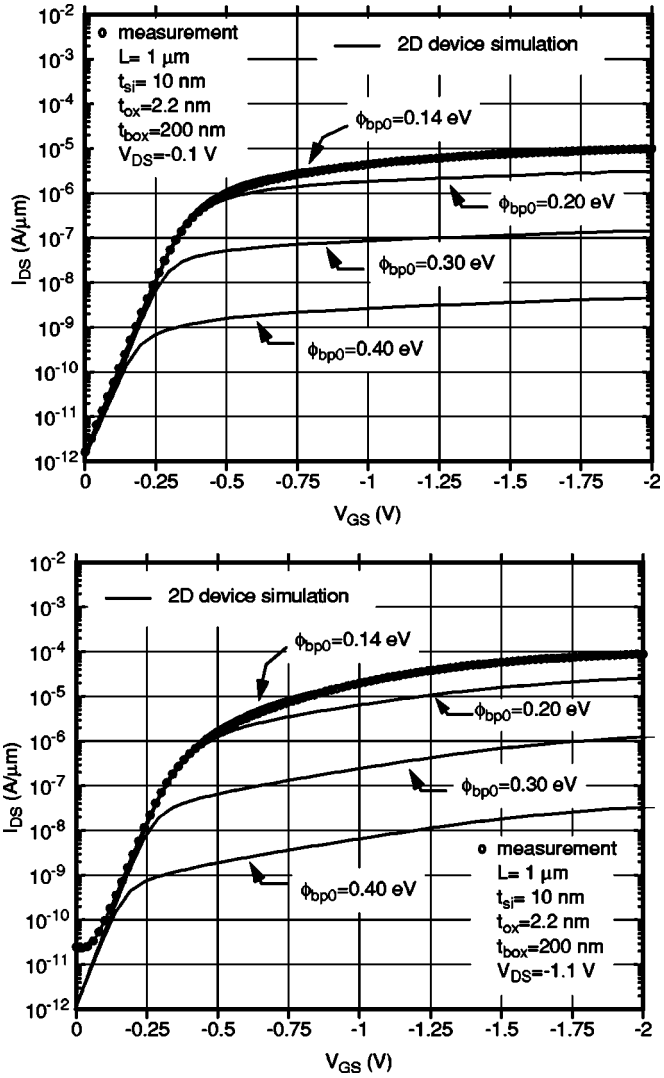

FIG. 16. Comparison between measured and simulated I_{DS}-V_{GS} characteristics of a long channel *p*-type SB-MOSFET with PtSi S/D: (a) $V_{DS} = -0.1$ V; (b) $V_{DS} = -1.1$ V. Simulations account for a variable zero-field Schottky barrier ϕ_{bp0} (0.14, 0.2, 0.3 0.4 eV). A correct current performance is achieved for the lowest barrier (0.14 eV), which consistently corresponds to the value (0.145 eV) that best fits the Arrhenius plot measured on test structures.

VII. MODEL VALIDATION ON A *p*-TYPE SB-MOSFET

As outlined in Refs. 2 and 3, the full potential of SB-MOSFETs can be obtained providing that the Schottky barrier can be reduced to 0.1 eV and below. Considering that the electric field distribution at the source/channel junction is considerably influenced by the band bending developed by the gate potential (Fig. 2), field emission is expected to significantly promote carrier injection to render the SB-MOSFET as competitive as its silicon junction counterpart. In that perspective, the measured effective barriers presented in Fig. 8 indicate that the 0.1 eV target is almost reached with a PtSi silicide system. Moreover, the modeling work exposed in the previous section also supports this assertion through the excellent quantitative agreement between experimental and calculated Arrhenius plots. However, the optimized ϕ_{bp0} equal to 0.145 eV and the even lower voltage-dependent effective barrier in the 0.11–0.12 eV range

significantly differ from commonly accepted numbers.[4–14] This discrepancy is attributed to our experimental setup coupled to an appropriate transport model that inherently accounts for lateral transport and tunneling effects. In order to further consolidate this interpretation, *p*-type SB-MOSFETs with PtSi S/D have been fabricated and measured. The proposed device architecture features a thin, 10 nm thick SOI channel, a 2.2 nm SiO_2 gate oxide, a tungsten gate encapsulated by Si_3N_4 spacers at each side, and a deposited SiO_2 capping layer on the top. As the SOI wafer is originally *p*-type (13–22 Ωcm), the on state is obtained by the accumulation of majority carriers (holes) as exemplified in Fig. 2. A TEM cross section of the PtSi S/D SB-MOSFET is given in Fig. 14. Full details on the process description will be published later.[25] In order to definitely decouple electrical effects related to the Schottky contacts from potential short channel effects, the following discussion is restricted to a long and wide channel ($L=1\ \mu\text{m}, W=10\ \mu\text{m}$). Figure 15 shows well-behaved I_{DS}-V_{GS} measured curves with a near-ideal subthreshold slope of 62 mV/decade. These current-voltage characteristics have been analyzed using the two-dimensional device simulator, IMPACT3. This code was recently enhanced with boundary conditions at Schottky contacts that reproduce TFE carrier injection and include barrier lowering in a way similar to the model revealed in Sec. V. A particular emphasis is put on the sensitivity of the current drive with the zero-field Schottky barrier ϕ_{bp0}. For that purpose, Fig. 16 compares I_{DS}-V_{GS} characteristics measured at $V_{DS}=-0.1$ V and $V_{DS}=-1.1$ V with their simulated counterparts for which ϕ_{bp0} is successively set to 0.14, 0.2, 0.3, and 0.4 eV. A correct current performance is achieved for the lowest barrier (0.14 eV) which consistently corresponds to the value (0.145 eV) that best fits the Arrhenius plot measured on test structures. It can also be clearly observed that barriers above 0.14 eV strongly degrade the current drive and give rise to a sharp down-bending of the I_{DS}-V_{GS} curves at the transition between weak and strong accumulation.

VIII. CONCLUSION

In summary, a test structure composed of two back-to-back junctions has been proposed to characterize materials with a low Schottky barrier. When coupled to a transport model that accounts for thermionic-field emission and barrier lowering due to image charge, it is shown that Arrhenius plots can be accurately reproduced over a wide range of temperature and applied bias. A particular emphasis has been put on PtSi contacts, for which a low zero-field barrier height of 0.145 eV was obtained through numerical optimization. A final consolidation of the measurement strategy and of the associated transport model has been performed through measurements and simulations on a long channel *p*-type SB-SOI-MOSFET with PtSi S/D. An excellent agreement between simulated and experimental I_{DS}-V_{GS} characteristics is obtained for a barrier height of 0.14 eV, consistent with the value (0.145 eV) that best fits the Arrhenius plot measured on test structures. According to these results, the measured PtSi effective barrier in the 0.11–0.12 eV range closely approaches the 0.1 eV bound below which the Schottky S/D architecture favorably compares with the conventional one.[3]

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