# Transient temperature measurements and modeling of IGBT's under short circuit

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# Transient Temperature Measurements and Modeling of IGBT's Under Short Circuit

Anis Ammous, Bruno Allard, *Member IEEE*, and Hervé Morel

***Abstract*—This paper discusses the estimation of possible device destructions inside converters in order to predict failures by mean of simulation. The study of insulated gate bipolar transistor (IGBT) thermal destruction under short circuit is investigated. An easy experimental method is presented to estimate the temperature decay in the device from the saturation current response at low gate-to-source voltage during cooling phase. A comparison with other classical experimental methods is given. Three one-dimensional (1-D) thermal models are also studied. The first one is a thermal equivalent circuit represented by series of resistance–capacitance (*RC*) cells, the second model treats the discretized heat-diffusion equation (HDE), and the third model is an analytical model developed by building an internal approximation (IA) of the heat-diffusion problem. It is shown that the critical temperature of the device just before destruction is larger than the intrinsic temperature, which is the temperature at which the semiconductor becomes intrinsic. The estimated critical temperature is above 1050 K, so it is much higher than the intrinsic temperature (∼550 K). The latter value is underestimated when multidimensional phenomena are not taken into account. The study is completed by results showing the threshold voltage $V_{\rm th}$ and the saturation current $I_{\rm sat}$ degradation when the IGBT is submitted to a stress (repetitive short circuit).**

***Index Terms*—Failure, IGBT, short circuit, temperature measurement, thermal modeling.**

## NOMENCLATURE

| | |
|---|---|
| $L, S$ | Effective length and area of insulated gate bipolar transistor (IGBT) chip. |
| $\mu_{ns}$ | Surface mobility of electrons. |
| $C_{\rm ox}$ | Oxide capacitance per-unit area. |
| $Z_c, L_c$ | Width and length of the channel. |
| $\beta_{\rm PNP}$ | Current gain of internal PNP bipolar transistor in IGBT. |
| $V_{FB}$ | Flat-band voltage. |
| $\psi_B$ | Substrate Fermi potential. |
| $\varepsilon_s$ | Silicon permittivity. |
| $q$ | Electron charge. |
| $N_A$ | Acceptor impurity density. |
| $n_i$ | Intrinsic carrier concentration. |
| $k$ | Boltzmann constant. |
| $i_A$ | Anode current. |
| $V_{AK}$ | Anode-cathode voltage. |
| $c$ | Silicon-specific heat. |
| $\rho$ | Silicon mass density. |
| $K(T)$ | Silicon thermal conductivity. |
| $K_0$ | Silicon thermal conductivity at 300 K (1.5486 W cm$^{-1}$ K$^{-1}$), |
| $T_a$ | Room temperature. |
| $T_{\rm ch}$ | Temperature in the end region of the channel. |
| $\hat{T}_{\rm ch0}$ | Estimated temperature in the middle region of the channel. |
| $T_{\rm ch0}$ | Temperature in the middle region of the channel. |
| $T_{\rm PNP}$ | Temperature in the bipolar transistor base region. |
| $T$ | Absolute temperature. |

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## I. INTRODUCTION

DESIGN IN power electronics is still based on breadboarding as computer-aided engineering (CAE) is yet unable to give simulation results about critical phases of a given converter. For example, it may not be estimated the possibility of device destruction inside a given converter.

The present paper covers a study about the short-circuit operation of insulated gate bipolar transistors (IGBT's). An IGBT may sustain a short-circuit operation, and it is interesting to study if it is possible to predict the device failure by means of simulation at the circuit level. Regarding the IGBT behavior under short-circuit operation conditions, literature shows that a destruction is always induced by a thermal phenomenon at the end of the device channel [1]–[4]. It is defined as a critical temperature when the device becomes uncontrollable (may not be turned off by the gate). It is the temperature of the channel end. Different values of critical temperature are given among literature. However, the physical phenomena that occur at the end of the device controllability phase is not clearly explained. Some authors [5] state that destruction occurs when intrinsic temperature is reached, i.e., the temperature at which the intrinsic carrier concentration becomes larger than the doping concentration of the hottest area. Unfortunately, the latter statement does not explain the device loss of controllability, as derived by the results of [4], where the authors give a destruction temperature value above 690 K, larger than the intrinsic temperature (above 500 K).

The present paper covers an experimental analysis of the IGBT short-circuit operation based on measurement of thermal-dependent parameters (Section II). Three one-dimensional (1-D) thermal models are described (Sections IV–VI) in order to discuss the thermal behavior of the system and to estimate the device peak temperature. The choice of the 1-D approximation is justified by the power semiconductor device geometry as the wafer thickness is very small with respect to other dimensions. In addition, the electrical power

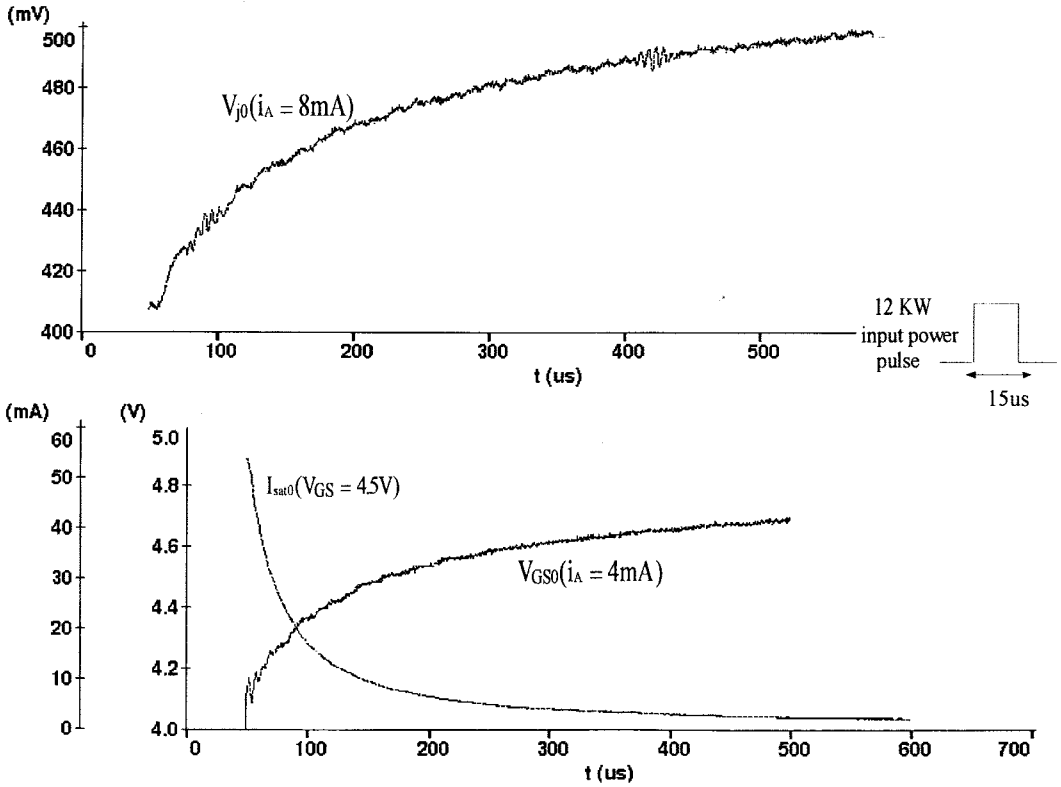


Fig. 1. Saturation current, PN junction voltage, and threshold voltage evolution during a cooling phase of the device.

is converted into heat at the top of silicon surface. So, heat flows essentially perpendicularly to the silicon surface. Section III presents the identification method of the parameters used for all the studied models.

## II. Experimental Estimation of the Device Temperature

### A. State of the Art

The experimental estimation of the hottest area temperature inside an IGBT is based on suitable and measurable parameters. The hottest area that leads to the device destruction is located at the end of the channel region, where the current density is high.

Literature proposes the threshold voltage $V_{\rm th}$ as a parameter depending on the channel temperature [6], [7]. The measurement of the latter parameter is performed after a self-heating phase (by power losses inside the device) due to a nondestructive short circuit. One main problem is the small dependence on temperature, i.e., a small range of variation (Fig. 1). Moreover, the measurement of $V_{\rm th}$ implies a fine control of the voltage $V_{GS}$ in order to insure a low current density inside the device during the cooling phase.

Another method for the estimation of the channel temperature during a device self-heating phase relies on the measurement of the saturation current for a high gate-to-source voltage $V_{GS}$ [8]. The results are not unique since they depend on circuit parameters (wiring inductors and power supply), and the temperature calibration of the saturation current may not be performed without power losses that participate to the device self-heating.

The temperature in the forward-biased PN junction of the internal PNP bipolar transistor of the IGBT can be classically estimated by the PN junction voltage $V_j$ [7]. After a self-heating phase, the IGBT under test is biased with a constant current (some milliamperes). Hence, $V_j$ can be measured (almost equal to drain-to-source voltage) and leads to the junction temperature (Fig. 1).

### B. A New Method

It is considered to measure the saturation current during a cooling phase of the device, but for a low voltage $V_{GS}$ (slightly larger than $V_{\rm th}$ at room temperature). The IGBT saturation current is given by [9]

$$I_{\rm sat} = (1+\beta_{\rm PNP}(T_{\rm PNP})\,\frac{\mu_{\rm ns}(T_{\rm ch0})C_{\rm ox}Z_c}{2L_c} \cdot (V_{GS} - V_{\rm th}(T_{\rm ch0}))^2. \quad (1)$$

In (1), the different temperature dependence has been explicitly specified. The surface mobility of electron $\mu_{\rm ns}$ depends mainly on temperature in the middle region of the channel $T_{\rm ch0}$ (Fig. 2). Notice that the latter temperature is different from the temperature in the end region of the channel $T_{\rm ch}$.

Moreover, the threshold voltage $V_{\rm th}$, of the $n$-channel MOS transistor in the saturation region depends on $T_{\rm ch0}$ temperature [6]

$$V_{\rm th} = V_{FB} + 2\psi_B + \frac{\sqrt{4q\varepsilon_s N_A \psi_B}}{C_{\rm ox}} \quad (2)$$

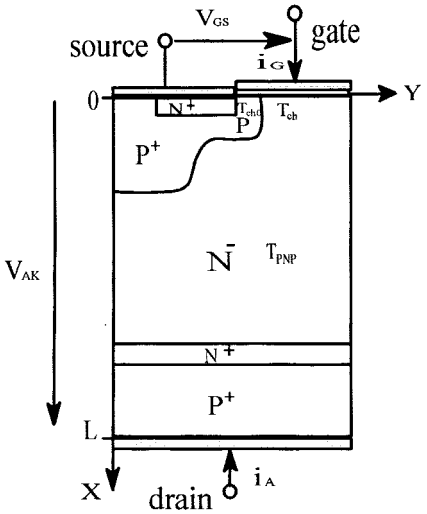


Fig. 2. Schematic diagram of IGBT under test.

where $\psi_B$ is the most temperature-dependent parameter

$$\psi_B = \frac{kT_{\rm ch0}}{q}\,\mathrm{Ln}\left(\frac{N_A}{n_{\rm i}}\right). \tag{3}$$

The variation of the threshold voltage is negative with respect to temperature (Fig. 3). The effective carrier mobility in the channel varies similarly with temperature because of various scattering mechanisms [10].

However, the PNP transistor current gain $\beta_{\rm PNP}$ depends on the temperature in the bipolar transistor base ($T_{\rm PNP}$). This temperature is different from $T_{\rm ch}$ and $T_{\rm ch0}$ during cooling phases because of the difference between spatial bipolar transistor base position and channel position (Fig. 2). This temperature dependence is a source of errors in both $V_{\rm th}$ and $I_{\rm sat}$ measurement.

Indeed, both measurement methods are based on temperature calibration of $V_{\rm th}$ and $I_{\rm sat}$ parameters without including self-heating in the device. So, in these conditions, $T_{\rm ch} = T_{\rm ch0} = T_{\rm PNP} = T_a$.

### C. Experimental Setup and Results

Fig. 4 shows the measurement setup for thermosensitive parameters. The device temperature is controlled by a heated air flow generated by a furnace unit. Fig. 3 shows the experimental temperature calibration curves for

$$V_{j0} = V_{AK}(V_{GS} = 15\ \mathrm{V},\ i_A = 8\ \mathrm{mA})$$
$$V_{GS0} = V_{GS}(V_{AK} = 30\ \mathrm{V},\ i_A = 4\ \mathrm{mA})$$
$$I_{\rm sat0} = i_A(E = 30\ \mathrm{V},\ V_{GS} = 4.5\ \mathrm{V}).$$

$V_{j0}$ is an estimation of $V_j$ voltage, $V_{GS0}$ is an estimation of $V_{\rm th}$ voltage, and $I_{\rm sat0}$ is the saturation current at low $V_{GS}$ voltage.

### D. Estimation of Transient Response of the Channel Temperature

The device under test $T1$ is submitted to a nondestructive short circuit in order to induce an important channel-temperature variation during a short time without inducing an elevation of the case temperature.

$V_{GS0}$, $I_{\rm sat0}$, and $V_{j0}$ parameters are measured during the cooling phase that corresponds to the same heat generation.

Figs. 5 and 6 shows the experimental circuit used for the measurement of $I_{\rm sat0}$ and $V_{GS0}$ responses, respectively. $V_e$ and $V_{\rm in}$ (Fig. 7) are the transistors $T1$ and $T2$ driving signals, respectively. Until time $t1$, the IGBT under test $(T1)$ is short circuited to the 250-V power supply. Thus, it is the place of a high saturation current in $T1$. Transistor $T2$ works in the linear region and is calibrated larger than $T1$. For the $I_{\rm sat0}$ measurement at $t = t_2$, $T1$ is biased in the saturation region with a low $V_{GS}$ ($V_{GS} = 4.5$ V). It is then a cooling phase for $T1$, and the saturation current measurement is performed. For the $V_{GS0}$ measurement at $t = t_2$, the transistor $T1$ gate is connected to the regulation system in order to impose a 4-mA saturation current in the IGBT under test $(T1)$.

The tested IGBT is an IR GPC 20U (13-A/600-V) device. Fig. 1 shows the evolution of the three thermosensitive parameters versus time.

The calibration curves conditions (Fig. 3) do not correspond exactly to the cooling phase condition because of the difference between $T_{\rm ch0}$ and TPNP temperature in the device.

### E. Error Evaluation and Discussion

In (1), the $(1 + \beta_{\rm PNP}(T_{\rm PNP}))$ quantity does not vary significantly in the studied range of temperature (300–420 K during cooling phase).

In the same temperature condition of the cooling phase, the current gain evaluation from the Hefner model [11], [12], corresponding to the IR GPC 20U IGBT, shows that the variation of the quantity is lower than 5%. So, errors due to the use of the calibration curve are not very important. Nevertheless, such errors occur in both the $V_{\rm th}$ and $I_{\rm sat0}$ measurement methods. Threshold voltage $V_{\rm th}$ (real value) is not measured directly, but deduced from the $V_{GS0}$ curve that corresponds to a 4-mA saturation current. So, in the $V_{GS0}$ measurement, the dependencies of $\beta_{\rm PNP}$ with respect to $T_{\rm PNP}$ introduce an error.

The contribution of $\beta_{\rm PNP}$ variation in the introduced error in both the $V_{GS0}$ and $I_{\rm sat0}$ measurement may be estimated. In fact, assuming variation to 5% and channel temperature around 400 K, the introduced error on the $V_{GS0}$ measurement (for $I_{\rm sat} = 4$ mA) using (1) is given by

$$\Delta V_{\rm GS0} = -\frac{\Delta\beta_{\rm PNP}}{2(1+\beta_{\rm PNP})}\,(V_{GS0} - V_{\rm th}).$$

For the $V_{GS0}$ response (Fig. 1), $\Delta V_{GS0} \approx 0.012$ V. Using the $V_{GS0}$ calibration curve in Fig. 3, this variation induces a channel-temperature error value around 1.3 K.

The introduced error on the $I_{\rm sat0}$ measurement (for $V_{GS} = 4.5$ V) is given by

$$\Delta I_{\rm sat} = \frac{\Delta\beta_{\rm PNP}}{1+\beta_{\rm PNP}}\,I_{\rm sat0}.$$

For the $I_{\rm sat0}$ response (Fig. 1), $\Delta I_{\rm sat} \approx -0.7$ mA. Using the $I_{\rm sat0}$ calibration curve in Fig. 3, this variation induces a channel-temperature error value around 0.7 K.

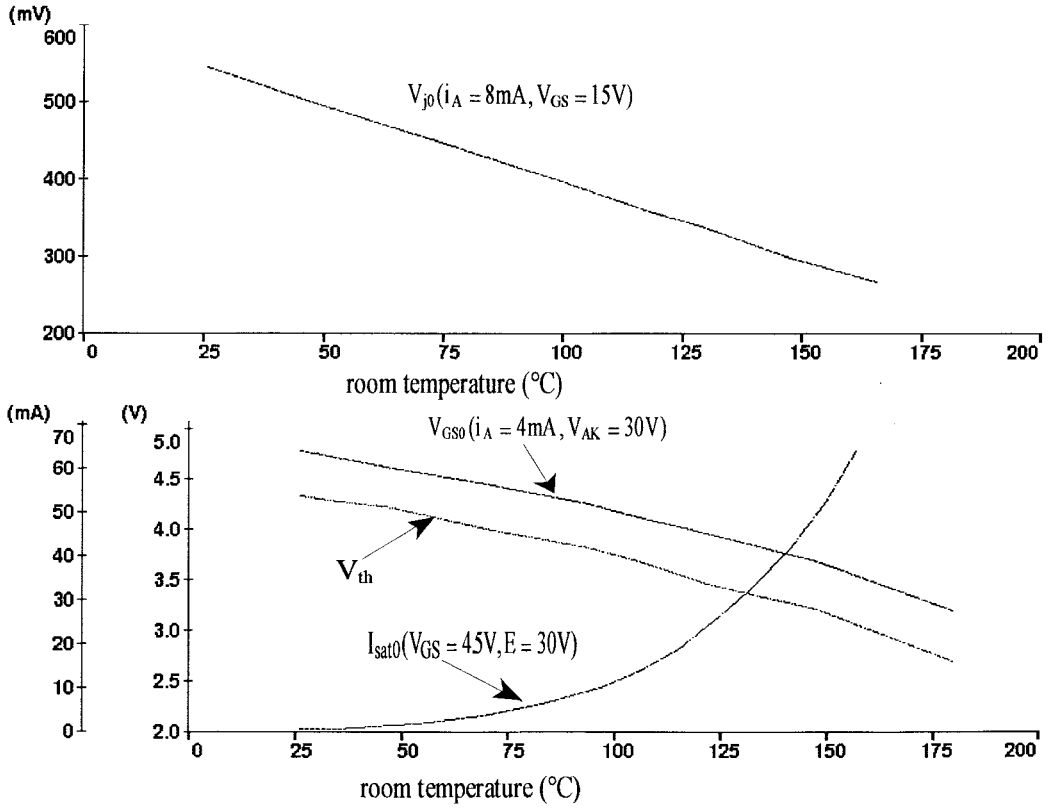


Fig. 3. Experimental calibration curves of estimated PN junction voltage $(V_{j0})$, estimated gate-to-source voltage $(V_{GS0})$, calculated threshold voltage $(V_{\rm th})$, and saturation current $(I_{\rm sat0})$.

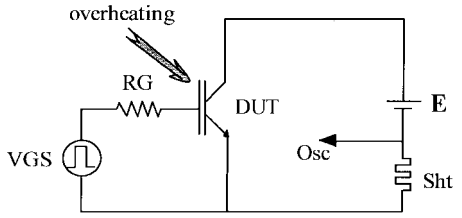


Fig. 4. Experimental circuit used for thermosensitive parameters calibration.

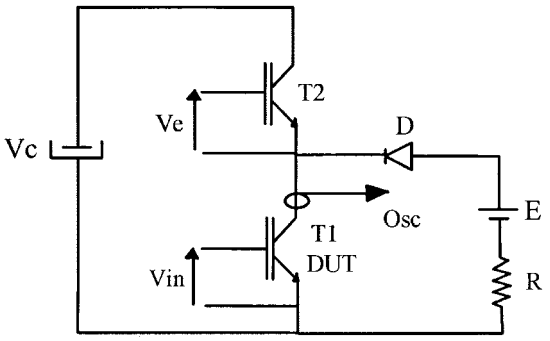


Fig. 5. Experimental circuit used for the measurement of the saturation current response during cooling phases.

It is clear that the introduced error on the $T_{\rm ch}^{I_{\rm sat}}$ estimation curve due to $\beta_{\rm PNP}$ variation is lower than the error introduced on the $T_{\rm ch}^{V_{GS0}}$ estimation curve, particularly at a high temperature.

Another error source in the $T_{\rm ch}^{I_{\rm sat}}$ estimated curve can be provoked by the IGBT $(T1)$ current regulation loop.

In fact, the $V_{GS}$ measurement during cooling phases is delicate and consists of imposing a fixed small current (4 mA) on the IGBT under test $(T1)$ (Fig. 6). The saturation current regulation is not ideal, particularly at high temperature, where the temperature dynamic is important and the saturation current flowing the IGBT is very high compared to the input current reference (around 4 mA). This can explain the difference between the two responses curves ($T_{\rm ch}^{I_{\rm sat}}$ and $T_{\rm ch}^{V_{GS0}}$) (Fig. 8).

Moreover, the $T_{\rm ch}^{V_{GS0}}$ measurement has a bad signal-to-noise ratio, and noise is induced by the measurement of the $V_{GS}$ voltage (high impedance).

We conclude that $T_{\rm ch}^{I_{\rm sat}}$ measurements are more accurate, and their implementations are easier than the $T_{\rm ch}^{V_{GS0}}$ measurement. Thus, $T_{\rm ch}^{I_{\rm sat}}$ measurements are retained to be compared later with simulation results. The $T_{j0}$ response gives the temperature evolution in the PN junction region that is deeper in the structure than the channel end. This explains the time delay in comparison with the other responses.

## III. Identification Method

The present section covers the identification method used with various 1-D models as presented in the following sections. The identification method goal is the research of an optimal parameter set $(p)$ for a given model by minimization of a

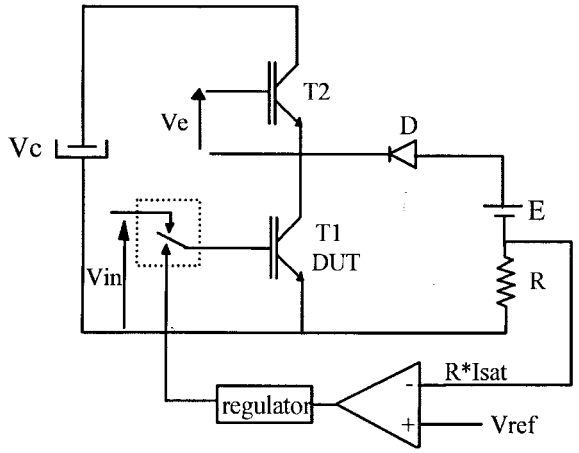


Fig. 6. Experimental circuit used for the measurement of the threshold voltage response during cooling phases.

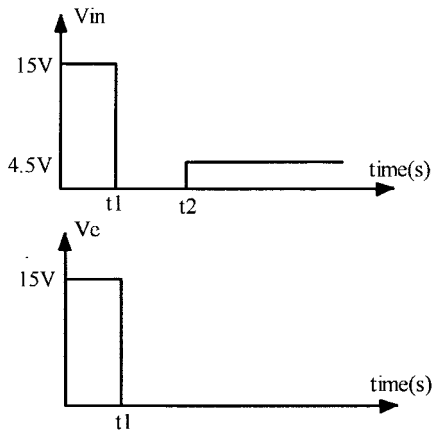


Fig. 7. Input waveforms for $T1$ and $T2$ switches used in the experimental circuit of Figs. 5 and 6.

quadratic error criterion $J$. The latter value is obtained by comparing the experimental results $\tilde{T}_{\text{ch0}}$ and the simulation results yielded by a given model of the system $T_{\text{ch0}}(p)$ for the parameter set $(p)$

$$J(p) = \left[\frac{1}{t_3 - t_2} \int_{t_2}^{t_3} (T_{\text{ch0}}(p) - \tilde{T}_{\text{ch0}})^2 \, dt\right]^{1/2} \tag{4}$$

where $t_2$ and $t_3$ are the boundary times of the experimental estimated temperature curve ($t_2 = 47$ $\mu$s and $t_3 = 2.1$ ms). The relaxation strategy with inequality constraints has been applied for model parameter identifications. All the simulations have been performed with the simulator PACTE [13].

## IV. Modeling with an Equivalent Thermal Circuit

A classical thermal model of silicon wafer is an infinite series of elementary resistance–capacitance (*RC*) cells (Fig. 9), where $R$ is a thermal resistance and $C$ is a thermal capacitance. This representation is the fruit of an analogy with electrical parameters. Strickland [14] has shown that the equivalent thermal circuit leads to the results yielded by the 1-D heat-diffusion equation (HDE). The approximation by a finite series is justified when it is sufficient to determine the temperature at only one geometrical position.

The circuit in Fig. 10 is considered. $P$ is a power source (defining the device power losses), and $n$ is the number of $RC$ cell pairs considered in the thermal model.

The system response (Fig. 8) admits at least two dominant poles—meaning that it cannot be represented by a first-order circuit. Hence, $n \geq 2$. The responses of various equivalent circuits are shown in Fig. 11 for $n = 2$, 3, and 4. The model parameters have been identified using the method described in Section III.

A second-order circuit only gives a rough approximation of the channel-temperature evolution. At least a third-order system is necessary.

It may be noticed that the peak temperature varies between 500 K for a second-order system and 455 K for a fourth-order system. Thus arises the question of whether this peak-temperature value is correct. The answer to this question is discussed later in the paper. Table I collects the values of the different components of the thermal network for various-order systems.

When the system order becomes large, $R_n$ has a tendency to be equal to $R_{\text{th}}$, which is the equivalent thermal resistance between channel and drain. It depends on the semiconductor thermal properties (thermal conductivity and specific heat) and device geometry.

## V. Discretization of the HDE

An accurate model is needed as a reference to predict the peak temperature in the device. Indeed, the HDE is discretized using a 1-D component geometry (Fig. 2). The 1-D equation for an isotropic material may be written as

$$\frac{\partial}{\partial x}\left[K(T)\,\frac{\partial T}{\partial x}\right] = \rho c\,\frac{\partial T}{\partial t}\,(t,x) \tag{5a}$$

subject to the boundary conditions

$$T(L) = T_a \tag{5b}$$

and

$$\left.\frac{\partial T}{\partial x}\right]_{x=0} = -\frac{1}{K(T(t,0))S}\,P(t) = -\frac{1}{f_s}\,P(t) \tag{5c}$$

where $P(t)$ is the input power and $f_s$ is the entropy flow.

The silicon thermal conductivity is given by [15]

$$K(T) = K_0\left(\frac{300}{T}\right)^{4/3}. \tag{6}$$

Fig. 12(a) gives responses of model (5) including either (6) or a constant silicon thermal conductivity $(K_0)$. These results have been obtained considering 400 nodes uniformly distributed. The system parameters are the equivalent length $L$ and the area $S$ of the device, which have been identified using the method of Section III. Using the thermal conductivity expression, the peak temperature is above 780 K. It is larger than what is obtained when considering a constant thermal conductivity (650 K) for the same input stimulus. The best value of the error criterion obtained with the HDE model is around 0.9 K.

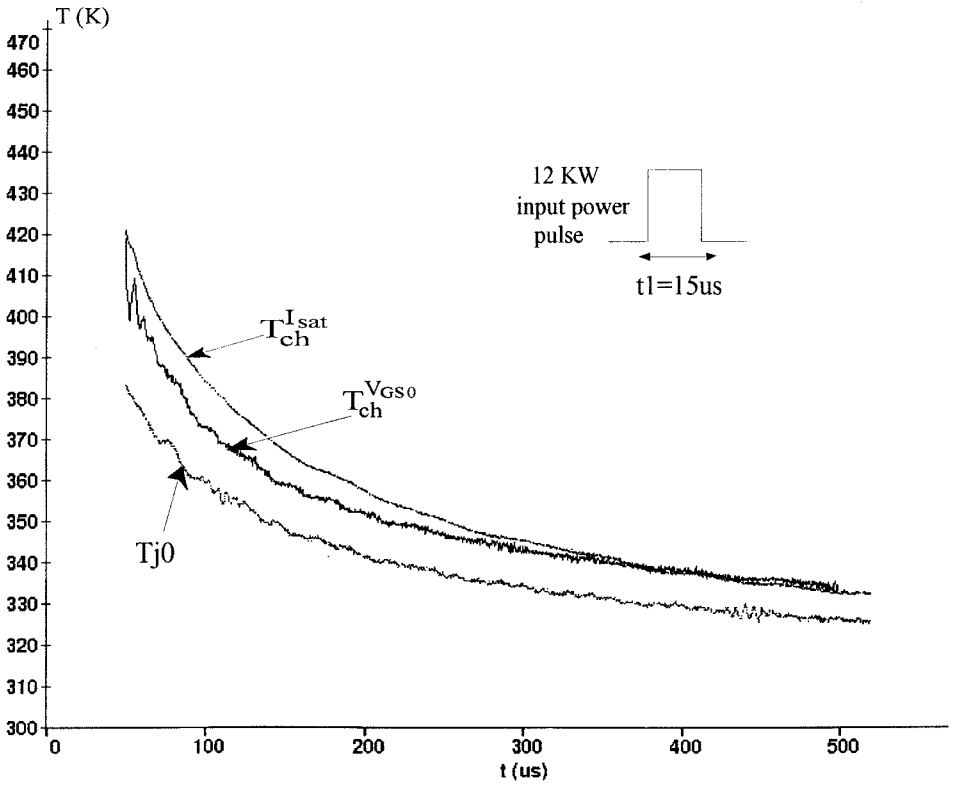


Fig. 8. Estimated temperatures during cooling phase.

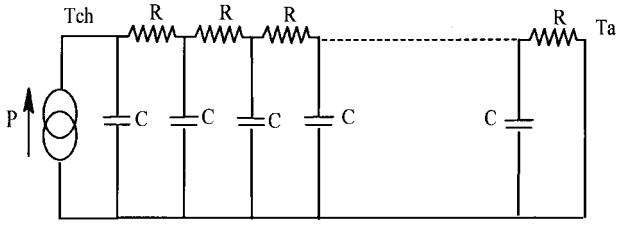


Fig. 9. Equivalent thermal circuit.

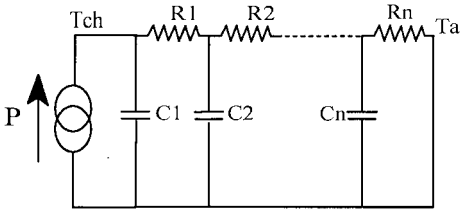


Fig. 10. Simulated model circuit.

Fig. 13 shows the temperature distribution along the geometric abscissa $x$ and for different times in the case of nonconstant thermal conductivity. It may be noticed that the peak temperature does not depend on the device thickness before tens of microseconds. It is due to the heat transit time to a given abscissa.

It may be noticed that the experimental junction temperature evolution $T_j$ does not agree with the temperature evolution at any abscissa $x$ in the device [Fig 12(b)]. This is due to the dependence of the PN junction voltage $V_j$ on temperature in several places in the device. So, methods for the estimation of $T_j$ based on the $V_j$ measurement do not suit with transient thermal conditions.

This numerical study shows that $RC$ thermal models are sufficient to predict long-term thermal responses, but they are insufficient to predict peak temperature.

## VI. Analytical Model and Internal Approximation

The heat-equation discretization model gives an accurate solution, but the simulation time is larger (about 90 times for 400 nodes) than with the equivalent thermal circuit. Thus, we have developed a model that is a good tradeoff between accuracy and simulation cost. A 1-D thermal model of the silicon chip may be obtained using the internal approximation (IA) [16], [17]. The finite-element method is based on the IA. However, the latter method is suitable for deriving analytical models. The method yields the best coefficients of a model that gives the nearest results with respect to the solution of problem (5). Unfortunately, IA is not easily applicable to nonlinear equations. Thus, a constant silicon thermal conductivity must be considered.

The normalized abscissa $y = x/L$ is introduced in (5). A so-called trial function $S(y)$ is considered. Using (5c), the integration of (5a) multiplied by a function $S(y)$ over [0, 1] with respect to $y$, yields

$$\frac{d}{dt}\int_0^1 T(t,y)S(y)\,dy + \frac{1}{\tau}\int_0^1 \frac{\partial T}{\partial y}(t,y)\,\frac{dS}{dy}(y)\,dy - \frac{1}{\tau}\frac{\partial T}{\partial y}(t,1)S(1) = \frac{P(t)S(0)}{\tau f_s} \tag{7}$$

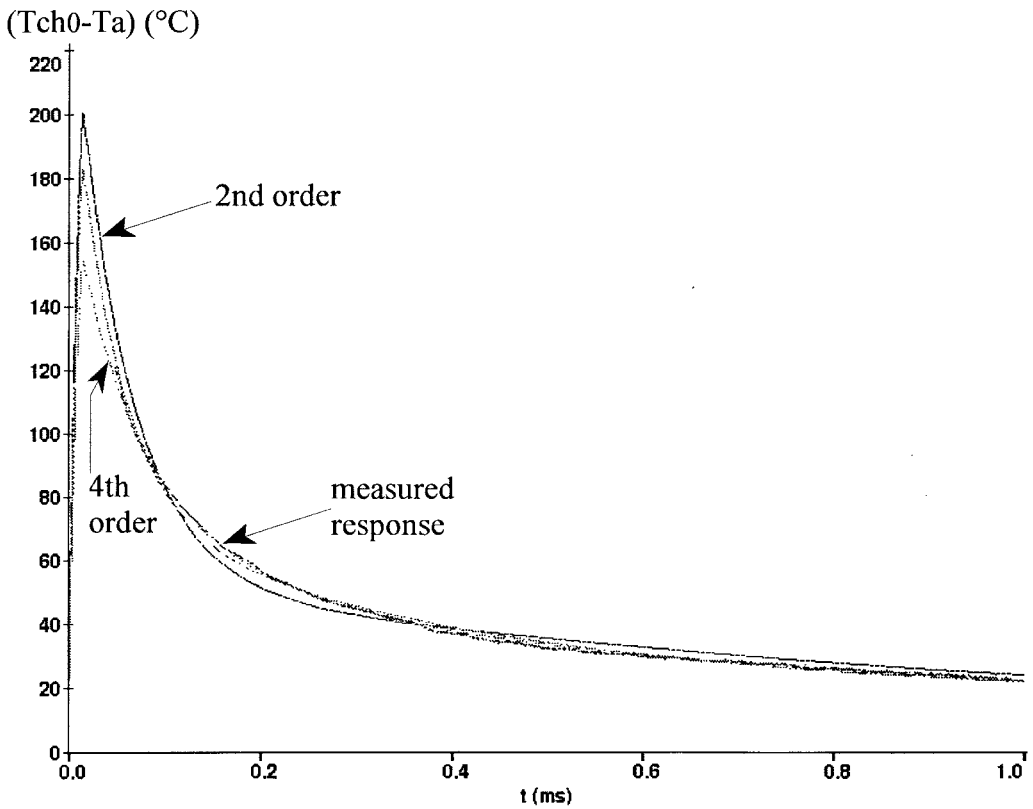


Fig. 11. Equivalent thermal circuit responses (for $n = 2,\ 3,$ and $4$).

where

$$\tau = \frac{\rho c L^2}{K}.$$

Equation (7) is a variational equation of the boundary value problem (5).

It must be now searched for a function $T_{ia}$ in a space $V_n$ as

$$T_{ia}(t,y) = T(L) + \sum_{j=1}^{n} \xi_j(t) W_j(y). \tag{8}$$

Suitable decomposition functions $W_j(y)$ enable a good approximation of the problem solution. Then, the distance between the solution $T$ of (7) and the space $V_n, d(T, V^n)$ has to be minimum. Practically, it is necessary to verify that any (numerical) solution may be well approximated by the decomposition functions.

Equation (7) applied for $n$ trial functions $S_i(y)$ and may be written in a matrix form

$$\frac{dX}{dt} = AX + Bu \tag{9}$$

where $X = M\xi,\ A = -RM^{-1},\ u = P(t)$, and

$$M_{ij} = \int_0^1 W_j(y) S_i(y)\, dy$$

$$R_{ij} = \frac{1}{\tau} \int_0^1 \frac{dW_j}{dy} \frac{dS_i}{dy}\, dy - \frac{1}{\tau} \frac{dW_j(1)}{dy} S_i(1)$$

$$B_i = \frac{S_i(0)}{\tau f_s}.$$

The chosen decomposition functions are

$$W_1(y) = 1 - y$$

$$W_i(y) = -y^{i-1} \exp(-y(i-1)) + \exp(-(i-1)) \quad (i = 2 \to 5)$$

$$W_i(y) = \alpha_i + \frac{\beta_i}{1 + \gamma_i y} \qquad (i > 5)$$

satisfying $W_i(1) = 0$ because $T(L) = T_a$.

The trial functions are chosen like

$$S_i(y) = y^{i-1}.$$

Fig. 14 gives simulation results obtained with models of order 2, 4, and 6.

Fig. 15 shows the error criterion $J$ and the peak temperature versus the model order. It may be noticed that the estimated peak channel temperature reaches a stable value (660 K) for models of at least order four. The temperature value is larger than what may be obtained with the $RC$ cell model.

On the other hand, the IA gives a model in which the behavior is near the behavior of the finite-difference model of the HDE assuming a constant silicon thermal conductivity. Nevertheless, the simulation time needed with the IA model is ten times less than with HDE model.

Fig. 16 shows the temperature distribution inside the device as obtained with the IA and HDE models, both assuming a constant silicon thermal conductivity. These distributions are nearly the same, and it is clearly shown the good agreement between the two models.

TABLE I
VALUES OF DIFFERENT THERMAL PARAMETERS OF THE MODEL ($t_1 = 15\ \mu$s, $t_2 = 47\ \mu$s, AND $t_3 = 2.1\ \mu$s)

| model parameters / model order | $R_j(10^{-3}$°C / W) for j= 1 → n | | | | | | $C_j(10^{-3}$W.s/°C) for j= 1 → n | | | | | | criterion J(K) | $R_n = \sum_{j=1}^{n} R_j$ | Tch peak (K) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| n=2 | 97.89 | 340.98 | | | | | 0.783 | 2.865 | | | | | 2.5 | 0.439 °C/W | 500 |
| n=3 | 86.031 | 185.37 | 348.37 | | | | 0.582 | 1.945 | 5.97 | | | | 1.01 | 0.62 °C/W | 483 |
| n=4 | 102.97 | 147.11 | 131.85 | 355 | | | 1.04 | 2.06 | 3.49 | 4.5 | | | 0.557 | 0.737 °C/W | 455 |
| n=5 | 103 | 149.9 | 228.3 | 64 | 83 | | 1.03 | 2.05 | 3.87 | 13.39 | 52.06 | | 0.553 | 0.63 °C/W | 456 |
| n=6 | 103.6 | 151.9 | 224.7 | 99.4 | 82.9 | 83.1 | 1.05 | 2.05 | 4.17 | 8.27 | 42.7 | 91.5 | 0.57 | 0.745 °C/W | 456 |

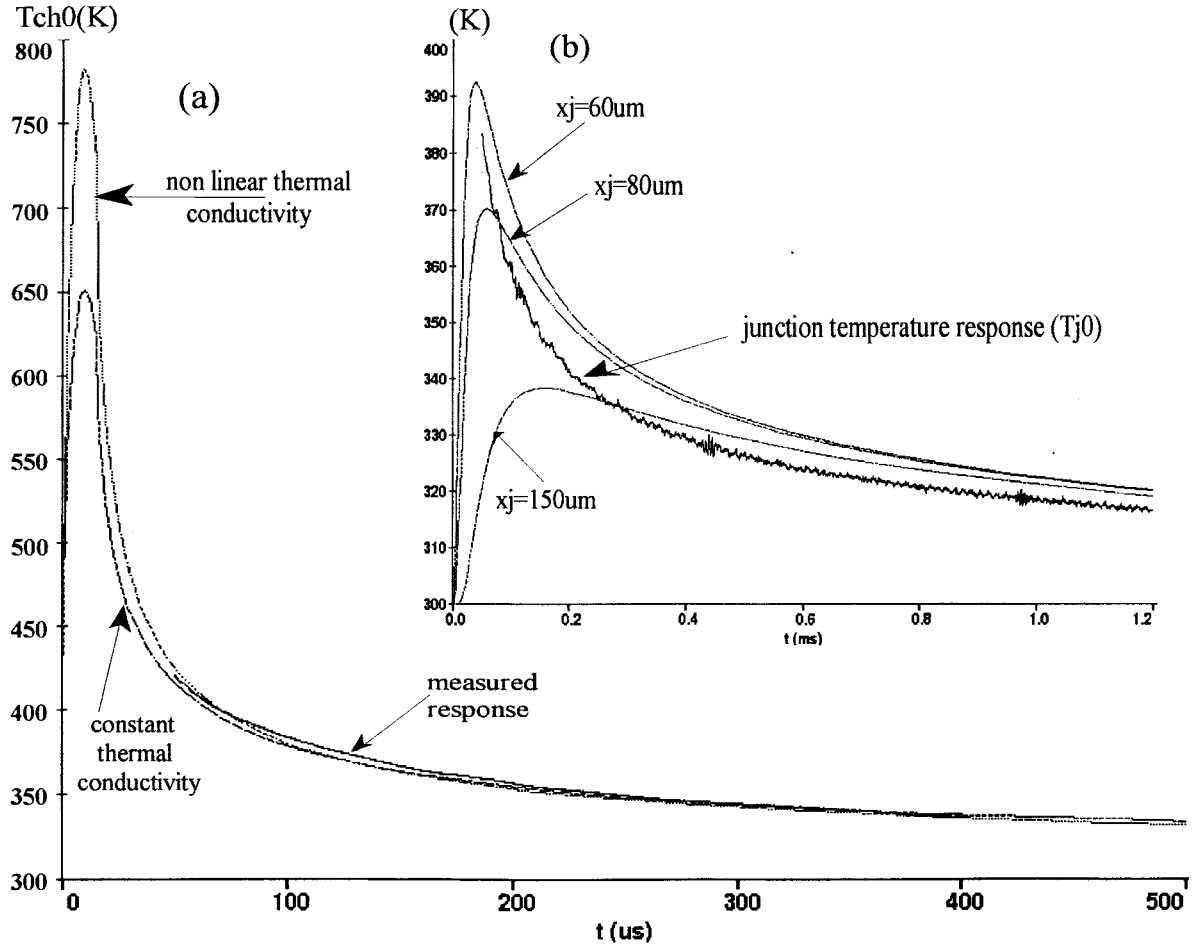


Fig. 12. (a) Heat-diffusion equation model responses with a nonlinear ($L = 668\ \mu$m and $S = 9.5$ mm$^2$) and constant thermal conductivity ($L = 597\ \mu$m and $S = 8$ mm$^2$). (b) HDE model responses at different abscissa $x$ with a nonlinear thermal conductivity.

## VII. BREAKDOWN TEMPERATURE ESTIMATED BY ALL THREE MODELS

The critical temperature in the device at destruction time instant is estimated using the three latter models.

The IGBT under test is submitted to a destructive short circuit as represented in Fig. 17.

The component is initially off, and a 15-V gate voltage initiates the short circuit. Fig. 18 shows the current and voltage waveforms during the short-circuit phase until the component destruction induced by very high instantaneous power losses and consequently increasing device temperature. Fig. 19 shows the destruction phase of the device that seems to have a fuse behavior. The dissipated power is very important, revealed by the explosion of the device case. Fig. 20 shows the time evolution of power losses until the device destruction. The channel peak temperature is then estimated using the three thermal models.

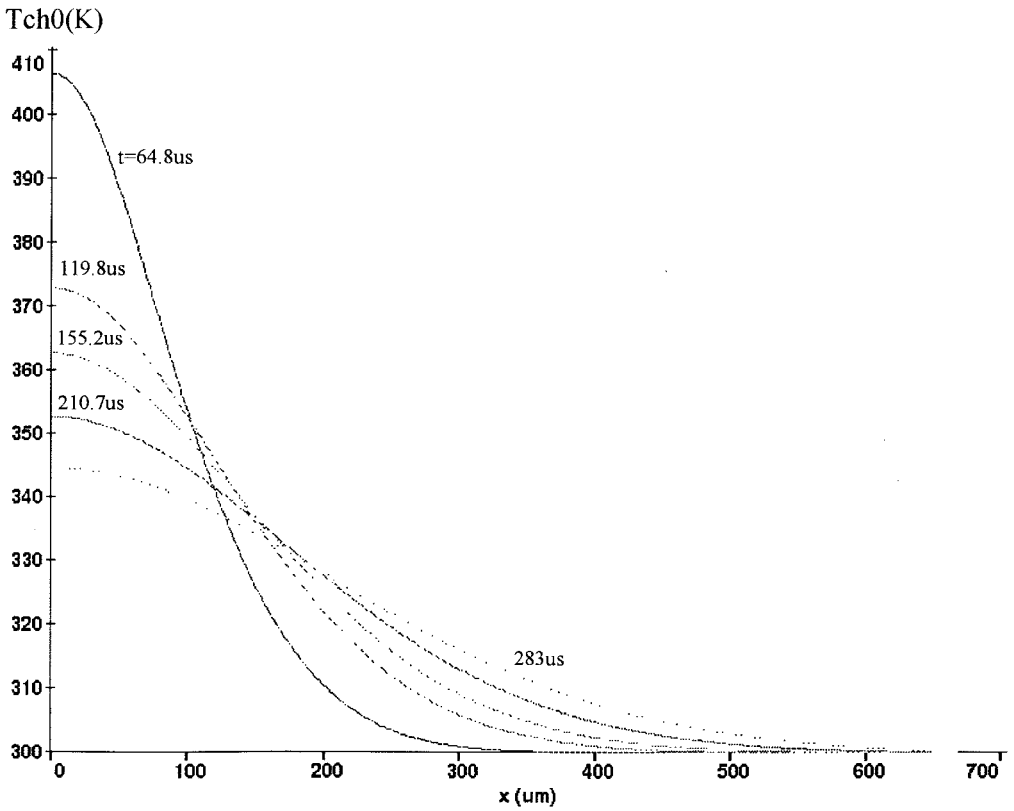


Fig. 13. Temperature distribution along $x$ abscissa at different times obtained with a nonlinear thermal conductivity ($L = 668$ $\mu$m and $S = 9.5$ mm$^2$).

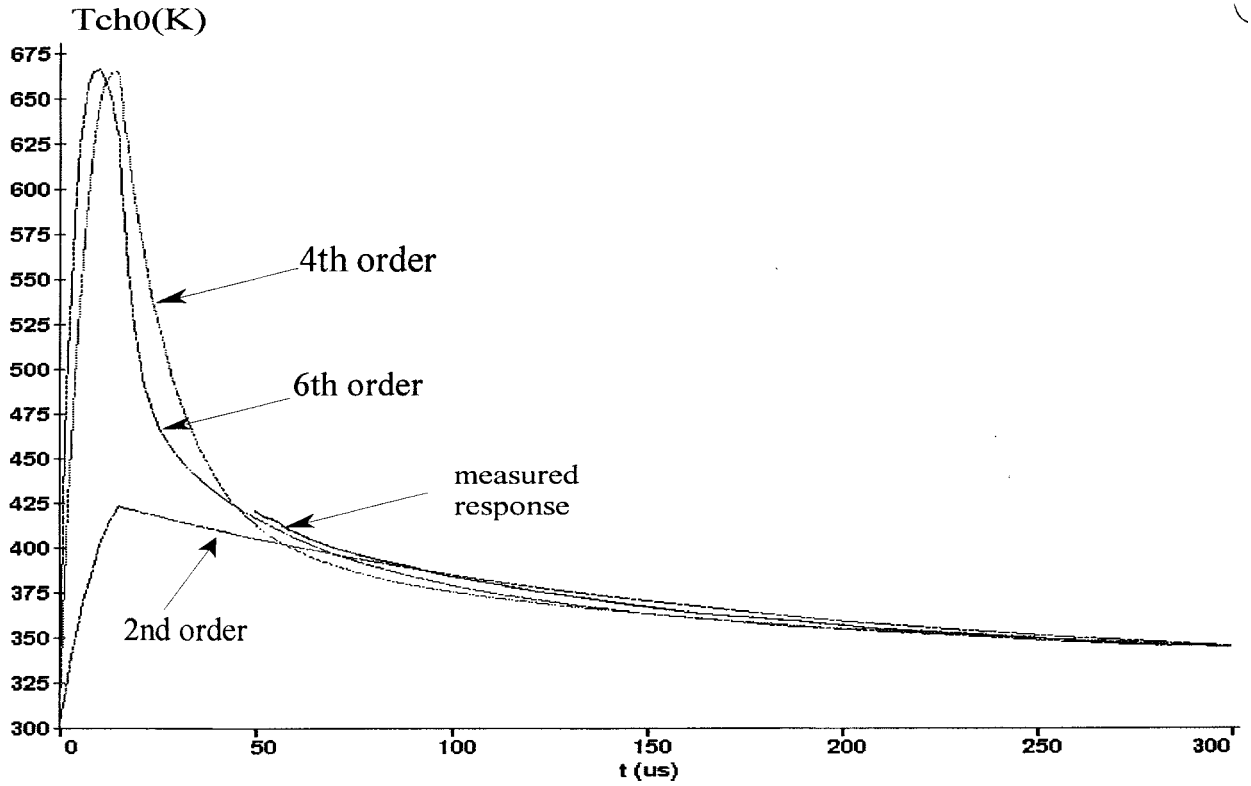


Fig. 14. Responses obtained with IA model for different system orders.

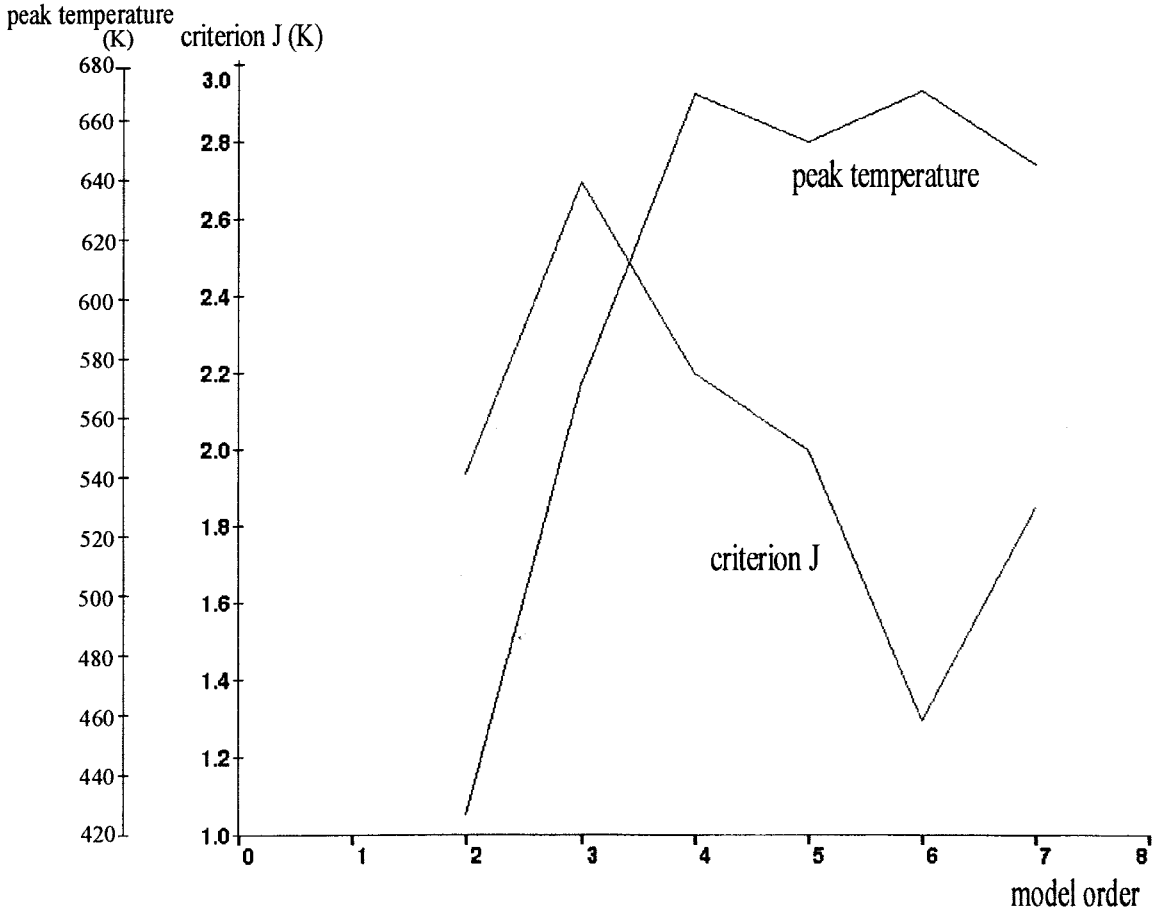


Fig. 15. Evolution of the peak temperature and the criterion $J$ versus model order.

The fourth-order thermal-network model predicts a 460-K temperature at the time of destruction. This temperature value is almost too low to be correct although the model response looks like the real system response. The value of the criterion $J$ during the identification of the thermal-network parameters is small. So, the thermal network is a pertinent model, but cannot predict the temperature in the very initial time of the response.

The IA model predicts a channel peak temperature of 770 K at the time of destruction. Finally, the finite-difference model predicts a peak temperature of 1050 K when considering a nonconstant silicon thermal conductivity.

We have also experienced the stress of IGBT's of the same family by submitting the devices to short-circuit cycles. The short-circuit duration is slightly smaller than the duration leading to the device breakdown (for the same power supply). The short-circuit application is repeated so that the device has cooled to the ambient temperature before a new stress is applied. The experience shows a degradation of the threshold voltage (Fig. 21) and the saturation current values (for $V_{GS} = 15$ V). The component #1 has a saturation current of 54 A before the experience, and the current is degraded by 0.5 A. The component #2 has an initial threshold voltage of 4.16 V, and the voltage varies 50 mV. It is destroyed after $26.10^4$ stress applications.

The latter variation leads us to believe that the peak temperature reached inside the chip is very high during the stress application. Such a temperature may provoke the diffusion of $N^+$ doping atoms in the emitter layer causing the change of the peak $P$-base doping concentration that controls the threshold voltage of the internal MOSFET. However, such a hypothesis requires a very high temperature at the end of the channel (1400 K). Indeed, the equivalent duration of the stress application (above 1 s) and the impurity diffusion coefficient value about $2.10^{-13}$ cm$^2$/s for Boron imply such a temperature value. In the presented 1-D models, the predicted temperatures in the device are assumed to be uniform in the device area at a given depth. This assumption is not true, and taking into account multidimensional phenomena enables predicting a higher temperature value. Moreover, the temperature estimated by measurement corresponds to the effective temperature in the channel, while the hottest temperature area is at the end of the channel. So, the 1-D thermal models underestimate again the critical temperature. Another classical hypothesis (in microelectronics) can be discussed concerning $V_{\rm th}$ degradation. This hypothesis assumes the change of oxide charge by ionized impurity diffusion in $SiO_2$, but the physical phenomenon is not clear, and data concerning temperature dependence of related diffusion mechanisms are not available.

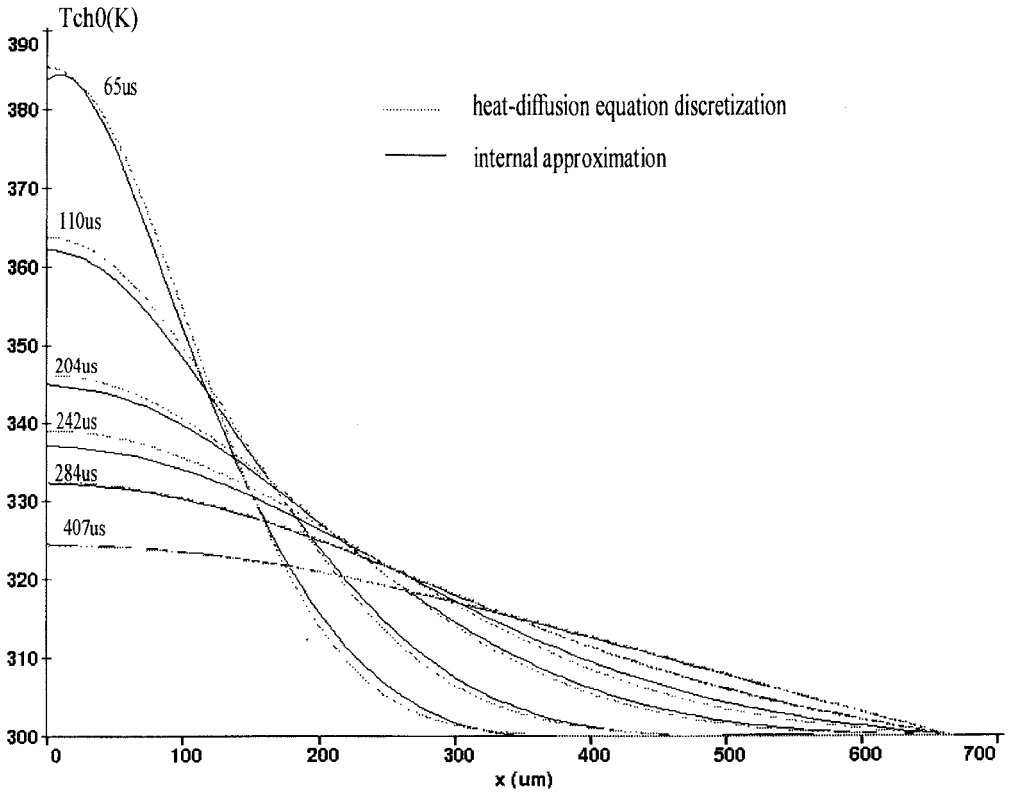


Fig. 16. Temperature distribution along $x$ abscissa at different times obtained with a constant thermal conductivity for the two models (IA and HDE).

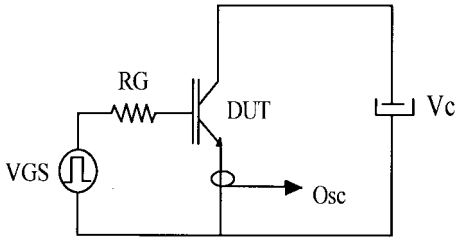


Fig. 17. Experimental circuit used for short-circuit test.

## VIII. Conclusion

A new experimental methodology has been developed for estimating the hottest area in the IGBT during a cooling phase succeeding the self-heating phase of the device. The method is based on saturation current measurement at low $V_{GS}$ value. Contrary to classical measurement methods, the system response has a good signal-to-noise ratio.

Three 1-D thermal models have been developed to estimate the peak temperature in the device, induced by a power pulse input, equivalent $RC$ thermal circuit, numerical model (HDE), and analytic model (AI).

The numerical model is very precise, and it can be used as a reference, and it enables to take into account the nonlinearity expression of the thermal conductivity. The AI model is a compact model with a few degrees of liberty that give a good tradeoff between accuracy and simulation time. It is a useful candidate model for power circuit design when coupling a thermal model to an electrical model.

The simple $RC$ thermal model is an empirical model that is sufficient to predict long-term responses, but it is not sufficient to predict the very fast variation of temperature.

The numerical model (HDE) predicts a destructive temperature above 1050 K. This temperature should be higher if multidimensional phenomena are taken into account. So, it is clear that the critical temperature is higher than the intrinsic temperature $T_i$ as presented in literature. Moreover, numerical studies show clearly that it is necessary to take into account the nonlinearity of the thermal conductivity.

The IA model gives a good tradeoff between accuracy and cost. However, it will be necessary to take into account the nonlinearity of the thermal conductivity in this analytical model to obtain an efficient model. We believe that coupling such a thermal model to an electrical model enables predicting the instantaneous temperature behavior in the device during critical phases and, thus, the reliability of a given converter with respect to the possibility of device destruction.

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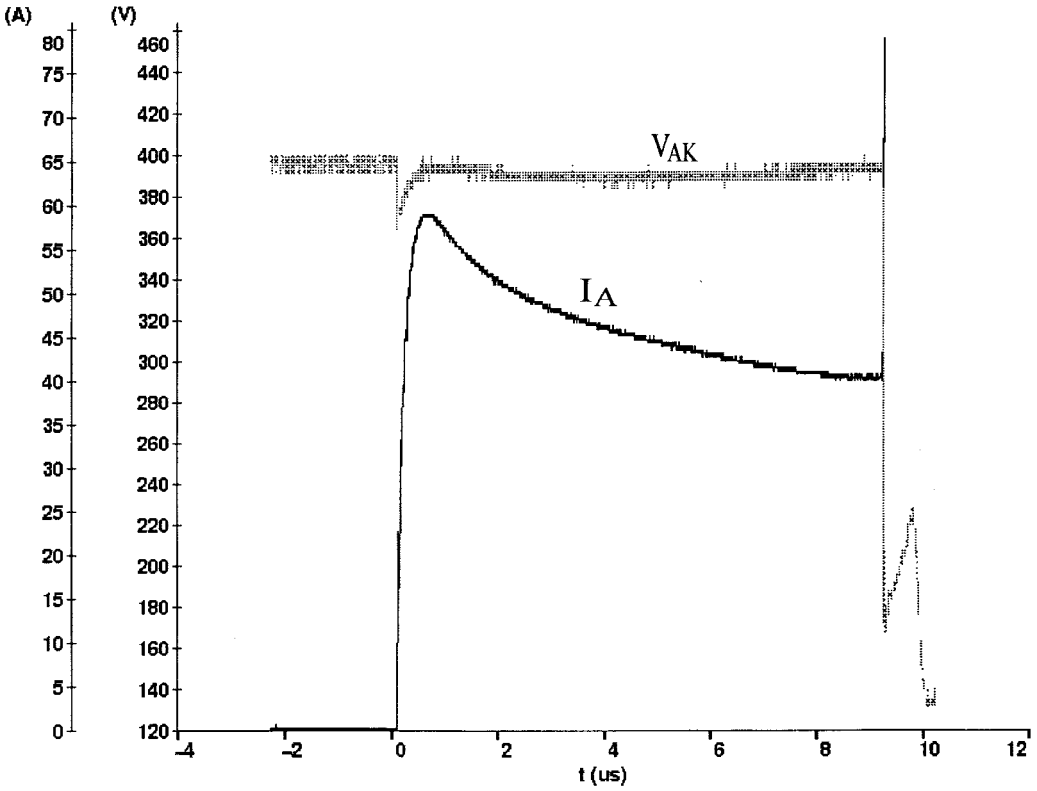


Fig. 18. Drain-to-source voltage and drain-current waveforms during a destructive short-circuit test.

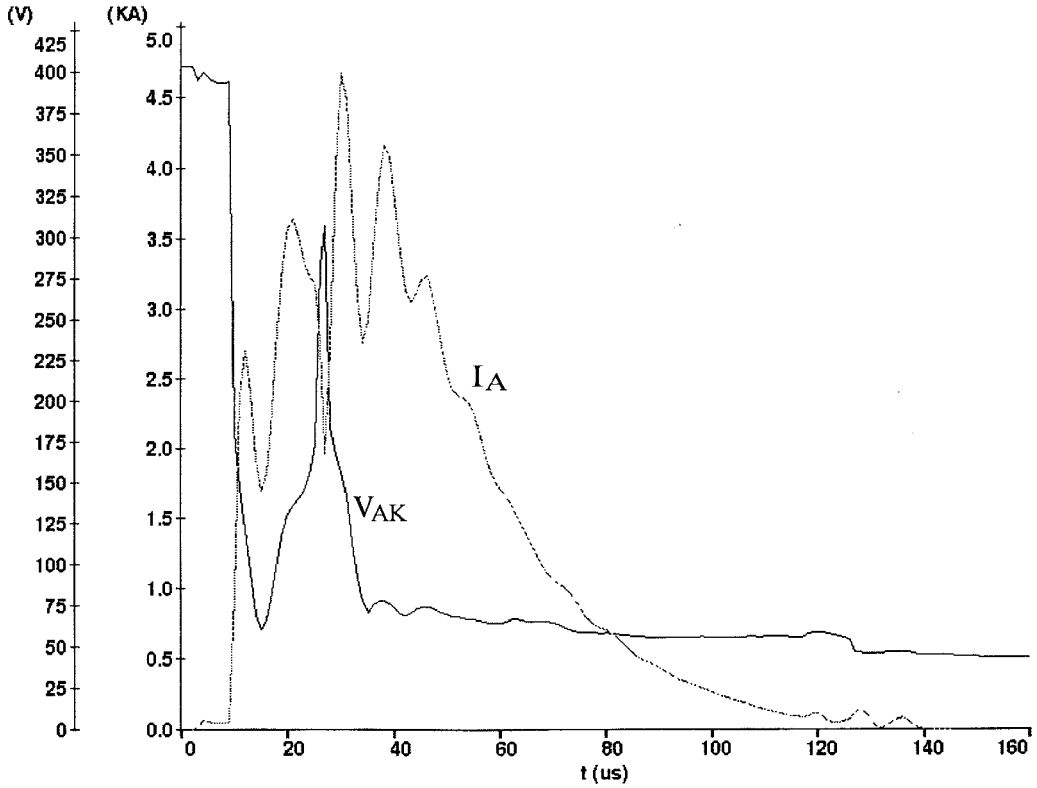


Fig. 19. Drain-to-source voltage and drain-current waveforms during short-circuit and destructive phases.

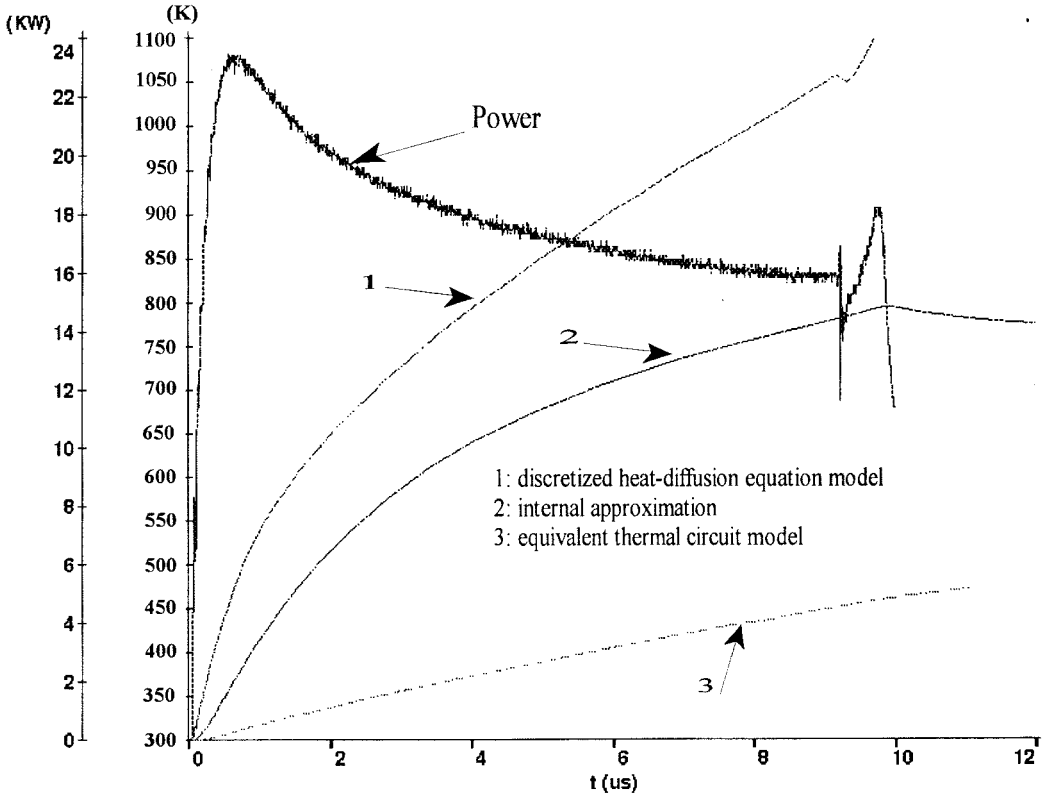


Fig. 20. Power losses in the device under a destructive short-circuit test and the temperature evolution as estimated by the three models.

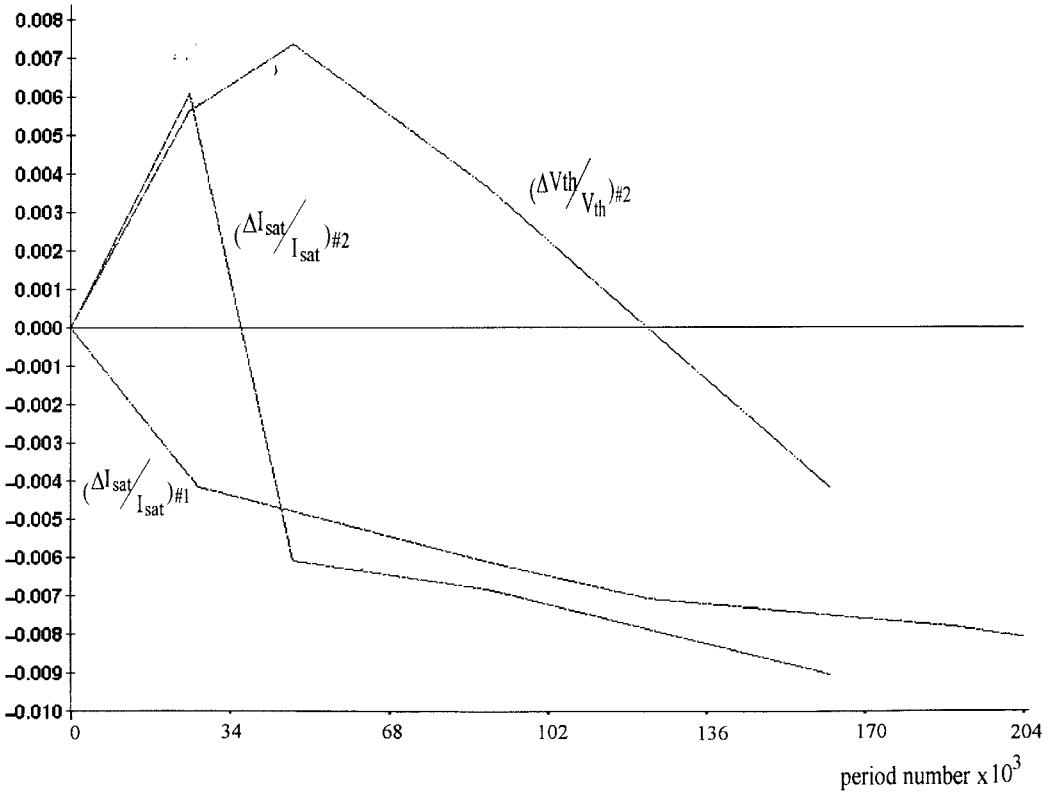


Fig. 21. Threshold voltage and saturation current degradation as a function of the number of stress application.

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