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# Integration of PtSi-Based Schottky-Barrier p-MOSFETs With a Midgap Tungsten Gate

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**Abstract**—This paper demonstrates the successful integration of Schottky barrier (SB) MOSFETs that feature platinum silicide (PtSi) source/drain and a tungsten midgap gate down to a length of 40 nm. SB MOSFETs are shown to steadily progress with respect to conventional highly doped source/drain with a current drive ( $I_{\text{on}}$ ) of 325–425  $\mu\text{A}/\mu\text{m}$ , an off-state current ( $I_{\text{off}}$ ) of 14–368 nA/ $\mu\text{m}$  at  $-2$  V for 100–40 nm physical gate lengths, respectively. Post-silicidation thermal treatments necessary to passivate defects at the silicon/silicon dioxide interface are shown to negatively impact electrical performance of short channel devices due to an increase of the SB to holes. Device simulation corroborates the increased sensitivity of the current drive to the modulation of the SB as the gate length is scaled down.

**Keywords** Deep level defects, metal gate, Schottky barrier (SB) MOSFET, silicon-on-insulator (SOI).

## I. INTRODUCTION

SEVERAL new architecture options are invoked in the International Technology Roadmap for Semiconductors [1] as technology performance boosters necessary to pursue down-scaling of CMOS technology, e.g., metal gate, high- $\kappa$  dielectric, multiple gate and source/drain (S/D) engineering. Among the main difficulties to overcome toward the ultimate technology node, many challenges are associated to the last booster that concentrates on S/D regions. For instance, junctions doped at levels above solid solubility, extremely steep lateral profiling, low resistivity silicides, and extremely low specific contact resistance at the silicide/silicon interface constitute many challenges for which no technological solutions are currently available or well established. One promising approach is to replace ohmic contacts on highly doped junctions by metallic junctions. From that standpoint, the Schottky barrier (SB) MOSFET architecture has received a renewed interest [2]–[18] for the potential it offers to provide atomically abrupt junction and reduced capacitive coupling with the advantage of process simplification. Furthermore, the reduced thermal budget used in the formation of silicided metallic junctions seriously alleviates issues associated with the integration of metal gates or high- $\kappa$  dielectrics. Finally, the SB-MOSFET architecture does not resort to complex doping techniques like solid-phase epitaxial regrowth (SPER) [19] or pre-amorphization and laser annealing [20] that are used

to promote a high level of dopant activation and a tight control of S/D profile abruptness. More recently, a variant of the metallic S/D architecture that takes advantage of dopant segregation at the silicide ( $\text{CoSi}_2$ ) metal interface has been successfully demonstrated [21], [22]. More conventionally, platinum silicide is used in SB p-MOSFETs [2]–[14] because of its very low SB height to holes [5]. For the n-type counterpart, rare earth silicides based on erbium [12], [14], [15] or ytterbium [16] present the lowest SB height for electrons. It is worth noting that most of published fabricated devices are implemented on bulk silicon substrate for which high leakage currents either due to sharp junction edges [3] or due to subsurface punchthrough as the channel length is scaled down are observed [2], [11], [13], [17]. Some groups have successfully introduced a thin silicon-on-insulator (SOI) substrate [5], [6] in order to reduce the off-state current or have implemented Schottky S/D contacts on a silicon-germanium (SiGe) [7] or on germanium-on-insulator (GOI) [10] substrate in order to decrease the barrier to holes as an attempt to improve the current drive of p-MOS devices. However, one common characteristic of many technological realizations is the improper electrical performance of one or several critical figures of merit like the maximum saturated current drive ( $I_{\text{on}}$ ), the off-state current ( $I_{\text{off}}$ ), the maximum transconductance ( $g_{\text{mmax}}$ ), the subthreshold swing or threshold voltage deviation due to drain-induced barrier lowering (DIBL). So far, another major difficulty has been to demonstrate device with  $I_{\text{on}}/I_{\text{off}}$  performance that competes with those of conventional architectures as well as a proper scaling of the threshold voltage. This paper demonstrates the successful integration of p-type SB-MOSFETs that feature a metallic midgap gate and PtSi S/D on an ultrathin SOI body. First, the fabrication process is briefly described in Section II. Results of electrical characterization are subsequently presented in Section III, based on measured  $I_{\text{on}}/I_{\text{off}}$ , subthreshold swing and DIBL for gate lengths of 2  $\mu\text{m}$ , and 100 and 40 nm, respectively. The impact of annealing under forming gas on the electrical performance is discussed and corroborated by device simulations that outline the sensitivity of current injection with potential barrier height variations after post-silicidation thermal treatment.

## II. PROCESS AND DEVICE DESCRIPTION

First, a 100-nm SOI substrate was chemically thinned to 10 nm. The p-type Si doping level is around  $2 \cdot 10^{15} \text{ cm}^{-3}$  corresponding to the initial substrate resistivity of 14–22  $\Omega \cdot \text{cm}$ . The active part of the device is isolated by a classical MESA technique where a trench is etched into the silicon film down to the buried silicon oxide by anisotropic  $\text{SF}_6/\text{N}_2$  reactive ion etching (RIE). A 2- $\mu\text{m}$ -long extrinsic gate finger was used to

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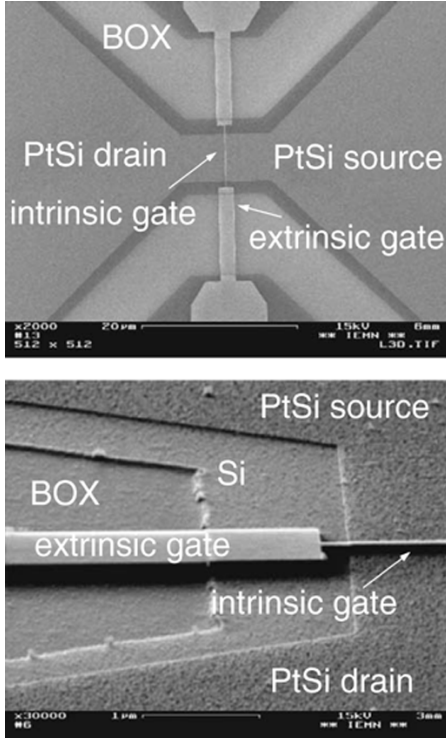


Fig. 1. Aerial scanning electron microscope views of a p-type SB MOSFET on a 10-nm-thick SOI channel with PtSi S/D and a 40-nm-long intrinsic gate. (a) Top view. (b) Perspective view showing the MESA-isolated active region.

step over the MESA before connecting to intrinsic gate (Fig. 1). A schematic view of the active device is proposed in Fig. 2(a). A gate oxide of 2.2 nm was subsequently formed by dry oxidation at 725 °C followed by tungsten deposition by e-beam evaporation. The gate was defined by e-beam lithography using an inorganic negative tone resist, hydrogen silsesquioxane (HSQ). After exposure and hard bake, HSQ holds the remarkable property to evolve from a cage-like monomer to a network-like polymer that approaches the structure of SiO<sub>2</sub> [23]. Therefore, after patterning the gate by RIE using a SF<sub>6</sub>/N<sub>2</sub> chemistry [24], the residual HSQ covering the tungsten gate was not removed but used as a capping layer. A 15-nm-thick nitride layer was then deposited by plasma-enhanced chemical vapor deposition to ensure a conformal coverage over the gate. An anisotropic RIE etching step was subsequently used to define 15-nm-wide spacers. According to this process sequence, the two sidewall nitride spacers and the residual HSQ resist on the top ensure a complete encapsulation of the metal gate. Lastly, S/D metal junctions were realized using a self-aligned silicide process. A 5-nm-thick platinum layer was evaporated after an HF dip used to remove the residual gate oxide. The silicidation reaction was activated by rapid thermal annealing at 300 °C during 2 min under N<sub>2</sub>/H<sub>2</sub> (97%–3%) [25]. The unreacted Pt layer covering the gate perimeter was removed in a diluted hot aqua-regia solution. The final step was a post-silicidation anneal in forming gas. The transmission electron microscope (TEM) cross section shown in Fig. 2(b) presents the fabricated device. The nearly full silicidation of the SOI film corresponds to the optimal configuration to minimize series resistances [18]. It is worth noting that the gate does not overlap the S/D silicided regions.

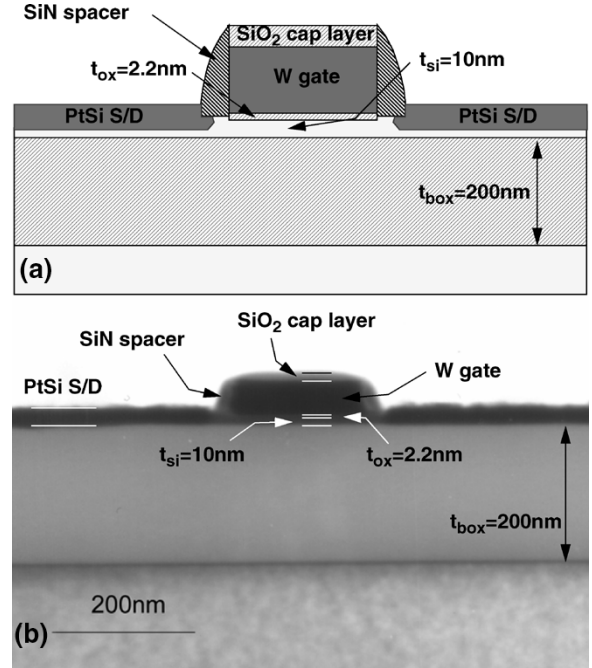


Fig. 2. (a) Schematic representation and (b) TEM cross section of a device architecture of SB p-MOSFET with a thin 10-nm-thick SOI channel, PtSi S/D, a 2.2-nm SiO<sub>2</sub> gate oxide, a 40-nm-thick tungsten gate encapsulated by 15-nm-wide Si<sub>3</sub>N<sub>4</sub> spacers at each sidewall and a deposited HSQ SiO<sub>2</sub>-like capping layer on the top.

As far as the SB is sufficiently low, an underlap of 10 nm is expected to provide an efficient way to control short channel effects without loss of current drive [18]. Finally, the proposed encapsulation scheme authorizes the integration of a large choice of metallic gate materials in PtSi-based SB-MOSFETs.

### III. RESULTS AND DISCUSSION

#### A. Electrical Characteristics

Fig. 3 presents  $I_{ds}-V_{ds}$ ,  $I_{ds}-V_{gs}$  and  $g_m-V_{gs}$  ideal characteristics of a 2- $\mu\text{m}$ -long channel device p-type SB-MOSFET. A subthreshold swing close to the low bound of 60 mV/dec is obtained. The  $I_{on}/I_{off}$  ratio ranges over six decades. The long channel threshold voltage of a midgap gate associated to a lowly doped thin SOI body is ideally determined by the gate workfunction, independent on the depletion charge. The threshold voltage is measured at  $-0.3$  V which corresponds to the expected target [9]. Fig. 4 presents  $I_{ds}-V_{ds}$ ,  $I_{ds}-V_{gs}$  and  $g_m-V_{gs}$  characteristics of a 100-nm-long SB p-MOSFET. An excellent overall performance is obtained with a saturation current of 325  $\mu\text{A}/\mu\text{m}$  at  $V_{ds} = V_{gs} = -2$  V. The subthreshold swing remains below 80 mV/dec, the DIBL is 85 mV/V and the maximum transconductance reaches 250 mS/mm at  $V_{ds} = -1.6$  V. In contrast to the 2  $\mu\text{m}$  MOSFET, a careful inspection of Fig. 4(a) reveals that the  $I_{ds}-V_{gs}$  characteristic of the 100 nm gate long device exhibits a slight but clear flattening at the transition between the subthreshold and the weak accumulation regimes. In order to explain the observed loss of current drive at reduced gate length, the relative weight of the contact resistance with respect to the channel resistance is first clarified. Secondly, it is speculated that the SB is modulated by the presence of platinum-induced deep

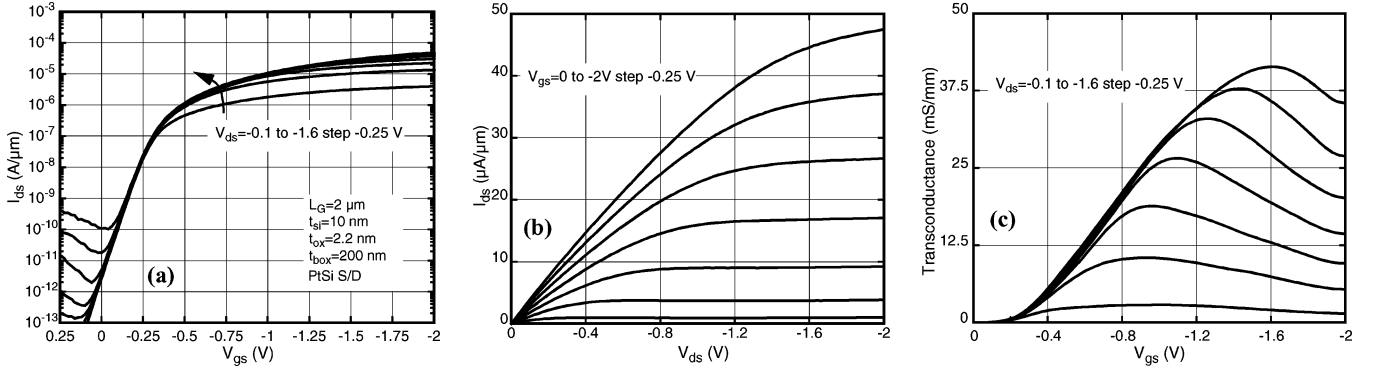


Fig. 3. Measured electrical characteristics of a 2- $\mu\text{m}$ -long channel p-type SB-MOSFET with PtSi S/D. The gatewidth  $W$  is 10  $\mu\text{m}$ . (a)  $I_{\text{ds}}-V_{\text{gs}}$  (b)  $I_{\text{ds}}-V_{\text{ds}}$  and (c)  $g_{\text{m}}-V_{\text{gs}}$ . A near ideal subthreshold swing of 62 mV/dec is obtained with an off-state current of 5 pA/ $\mu\text{m}$  at  $V_{\text{ds}} = -1.1$  V. No sign of sub-linear upward bending of the  $I_{\text{ds}}-V_{\text{ds}}$  curves at low drain voltage is observed.

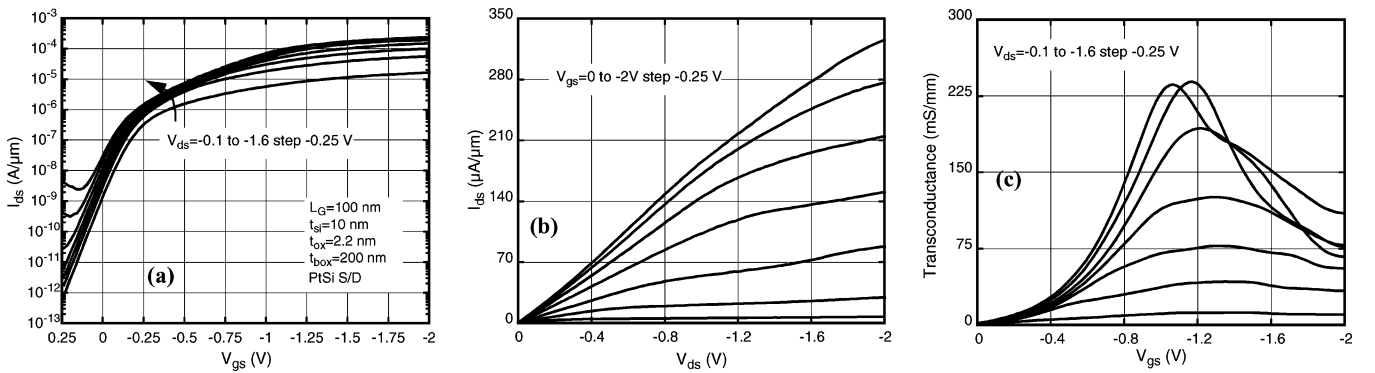


Fig. 4. Measured electrical characteristics of a 100-nm-long channel p-type SB-MOSFET with PtSi S/D. The gatewidth  $W$  is 10  $\mu\text{m}$ . (a)  $I_{\text{ds}}-V_{\text{gs}}$  (b)  $I_{\text{ds}}-V_{\text{ds}}$  and (c)  $g_{\text{m}}-V_{\text{gs}}$ .

level traps and/or by platinum-hydrogen complexes depending on the annealing ambience and temperature. Referring again to Fig. 4(a), the combination of these two physical mechanisms is subsequently proposed as a plausible interpretation of the current flattening for  $0.15 \leq |V_{\text{gs}}| \leq 1$  V.

### B. Contact Versus Channel Resistance

The transition from a body-controlled to a tunneling controlled current has been invoked as a possible mechanism that explains the change of slope when a flatband condition occurs at the source/channel junction [14], [16]. This view is partially correct in the limit of high barrier height. Fig. 5 shows how simulated  $I_{\text{ds}}-V_{\text{gs}}$  curves are affected by the SB height for 1- $\mu\text{m}$ , 100- and 40-nm-long devices. When the SB to holes ( $\phi_{\text{bp}}$ ) is larger than 0.2 eV, current characteristics above threshold are identical irrelevant to the channel length. This observation supports the picture according to which current injection due to both thermoionic and field emission is ultimately limited by the barrier height. However, the situation is slightly more complex depending on the relative weight of the channel resistance with respect to the contact resistance, the latter being nonlinearly dependent on the SB height. For a 1- $\mu\text{m}$ -long device, Fig. 5(a) indicates that lowering the barrier below 0.15 eV does not improve the current level because the channel resistance dominates the source-to-drain resistive path. In contrast, Fig. 5(b) and (c) shows that the current-voltage of 100- and 40-nm-long devices still remain sensitive to an incremental reduction of barrier

below 0.15 eV because the current drive is dominated by the injection level at the source/channel junction. To summarize, the above analysis justifies the ideal experimental characteristics of the 1- $\mu\text{m}$ -long SB-MOSFET reported in Fig. 3 that remain limited by the channel resistance. As expected, it is also confirmed that a proper reduction of S/D barrier height is required to maintain the dominant role of the channel resistance when the gate length is scaled down. Departure from this prescription renders the current level very sensitive to small barrier variations, regardless of their origin. Nevertheless, a mechanism of SB modulation dependent on gate voltage would reasonably explain the current reduction at the transition between subthreshold and weak accumulation regimes observed in Fig. 4(a). In the next section, platinum-induced deep level traps and the formation of additional platinum-hydrogen complexes are identified as the possible mechanism of SB modulation.

### C. Properties of Platinum-Induced Deep Level Traps

In experiments conducted at the elementary device level, Tsaur *et al.* [26] were the first to observe a modulation of the SB to holes in PtSi junctions depending on the annealing atmosphere. Vacuum annealed Schottky junctions at 300  $^{\circ}\text{C}$  for 30 min gave a 0.197-eV barrier while an identical thermal budget in flowing  $\text{H}_2$  at a pressure of  $10^{-7}$  torr decreased the barrier as low as 0.184 eV. Subsequent vacuum annealing showed the effects of  $\text{H}_2$  treatment to be reversible with the SB height recovering the upper bound. The application of a third

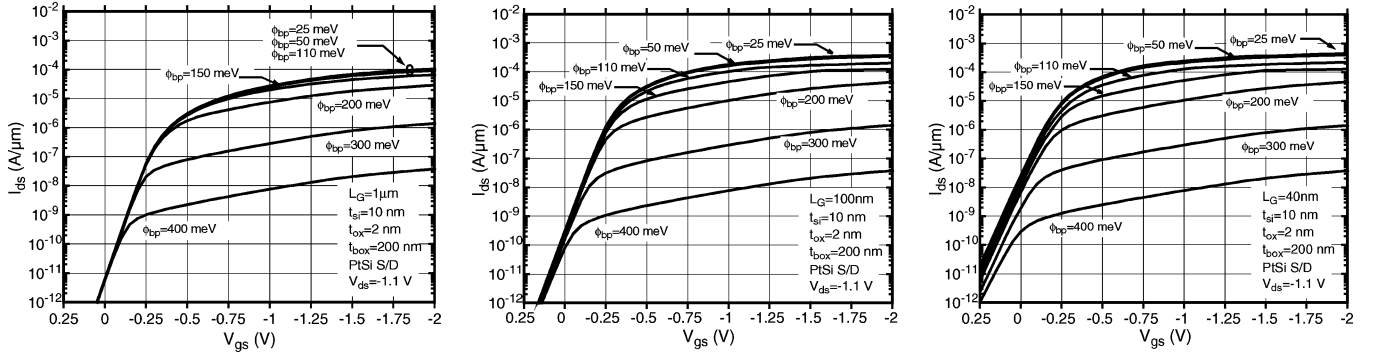


Fig. 5. Simulated  $I_{ds}$ - $V_{gs}$  characteristics of a p-type SB-MOSFET with PtSi S/D at  $V_{ds} = -1.1$  V for gate length of (a)  $1 \mu\text{m}$ , (b)  $100 \text{ nm}$ , and (c)  $40 \text{ nm}$ . Simulations account for a variable SB (25, 50, 110, 150, 200, 300, and 400 meV).

TABLE I  
IDENTIFICATION OF Pt-RELATED DEFECTS AND Pt-H COMPLEXES INDICATING THEIR ENERGY IN BANDGAP RELATIVE TO BAND EDGES, THEIR ASSIGNMENT, CHARGE STATE, AND TYPE [31]–[33]

Defect ID	Energy	assignment	charge state	defect type	
				acceptor	donor
Pt120	Ec-0.23	substitutional Pt	-/0	x	
Pt160	Ev+0.33	substitutional Pt	0/+		x
Pt50	Ev+0.09	substitutional Pt	+ /++		x

Defect ID	Energy	assignment	charge state	defect type	
				acc	don
E90	Ec-0.18	Pt-H <sub>2</sub>	--/-	x	
E250	Ec-0.50	Pt-H	-/0	x	
H210	Ev+0.40	Pt-H <sub>2</sub>	-/0	x	
H150	Ev+0.30	Pt-H <sub>3</sub>	-/0	x	

thermal budget in hydrogen atmosphere for the same duration and temperature conditions revealed again a decrease of the SB to holes accompanied by a coherent increase of the barrier to electron by the same amount. To account for these results, the authors attributed the modulation of the SB height to the presence of electrically active defects in the bandgap situated in silicon close to the silicide-Si interface [26]. One possible concern related to the silicidation reaction is indeed the formation of deep level defects into silicon in the vicinity of the Schottky interface [27]. In the specific case of platinum-based silicides, a conversion to p-type conductivity was even observed under the silicide surface on an initially n-type phosphorus doped substrate [28]. The identification of platinum-induced deep level traps has been a subject of debate for many years [29], [30]. It is now well established that substitutional Pt forms a trivalent defect with a single acceptor level (Pt120) 0.23 eV below the conduction band and a single donor level (Pt160) as well as a double donor level (Pt50) located at 0.33 and 0.09 eV above the valence band, respectively [31]. More recent literature [32] has provided a complete review of the interaction of hydrogen with transition metal impurities in silicon. Using depth profiling of all platinum-related defects by deep level transient spectroscopy, Sachse *et al.* [31], [33] have convincingly demonstrated the creation of four additional acceptor-like levels (E90, E250, H210, H150) in the silicon bandgap attributed Pt-H complexes after sample hydrogenation. The main characteristics of platinum electrical levels and of its complexes are summarized

in Table I. In the following discussion on thermal stability of Pt-H related defects, we essentially concentrate on the lower half of the silicon bandgap which corresponds to the region where band bending determines current injection relevant to p-type MOSFETs. In the absence of thermal treatment, the two donor levels of substitutional platinum  $\text{Pt}^{+/++}$  (Pt50) and  $\text{Pt}^{0/+}$  (Pt160) are the dominant stable defects. Upon annealing at  $100 \text{ }^\circ\text{C}$ , the  $\text{Pt}^{0/+}$  (Pt160) concentration decreases slightly while the acceptor level  $\text{Pt-H}_2^{-/0}$  (H210) increases by the same amount [31]. A higher heat treatment conducted around  $200 \text{ }^\circ\text{C}$  is characterized by a dramatic reduction of the two donor levels  $\text{Pt}^{+/++}$  (Pt50) and  $\text{Pt}^{0/+}$  (Pt160) quantitatively correlated to the appearance of the acceptor level  $\text{Pt-H}_3^{-/0}$  (H150) indicating that the nature of the defects has totally switched from donor-like to acceptor-like [31], [34]. Further annealing above  $350 \text{ }^\circ\text{C}$  for 1 h holds the property to completely anneal out the Pt-H-related complexes and to restore the initial donor levels,  $\text{Pt}^{+/++}$  (Pt50) and  $\text{Pt}^{0/+}$  (Pt160), associated to substitutional Pt [34].

#### D. Impact of Pt and Pt-H Induced Defects on Current-Voltage Characteristics

For the sake of completeness, Fig. 6 schematically illustrates the influence of donor or acceptor-like defects located in the vicinity of a silicide-Si interface. It is assumed that the position of energy bands with respect to the Fermi level at the right-hand side is essentially governed by the voltage applied to the gate of

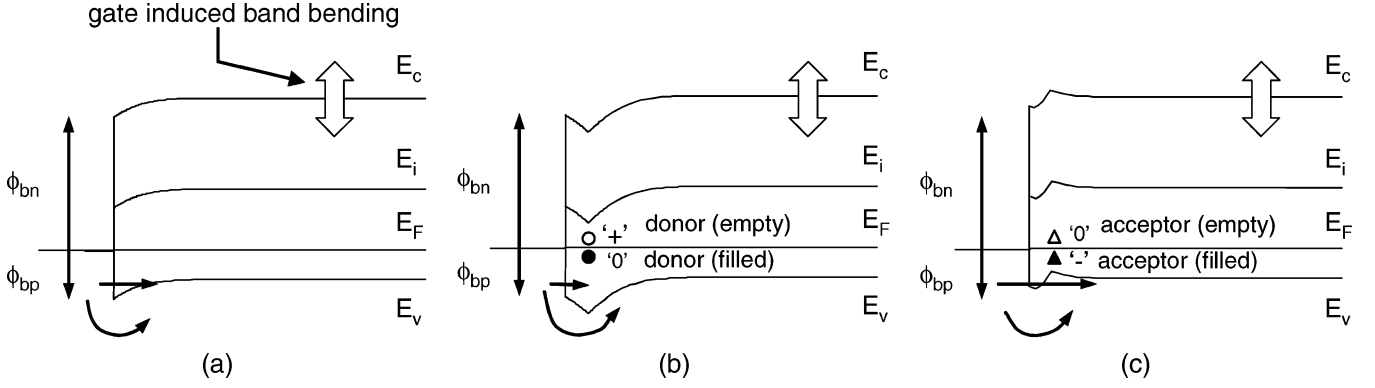


Fig. 6. Schematic representation of band curvature in the vicinity of the source/channel interface. The position of energy bands at the right-hand side is primarily governed by the gate potential of the MOS structure. (a) Reference band configuration in absence of electrically active defects. (b) Band deformation induced by an empty positively charged donor level lying above the Fermi level. The other filled donor defect below Fermi-level remains neutral. (c) Band deformation induced by a negatively charged filled acceptor level lying below Fermi level. The other acceptor level located above Fermi level remains empty and neutral.

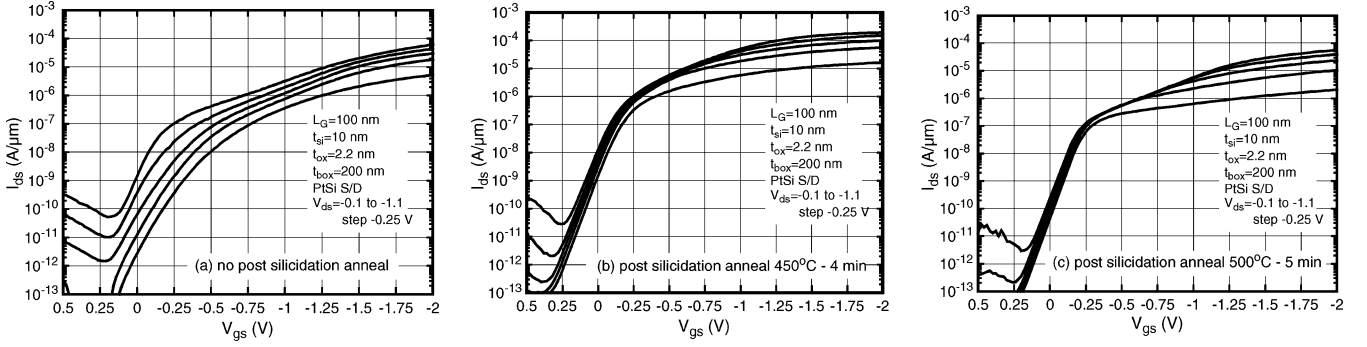


Fig. 7. Comparison between measured  $I_{ds}-V_{gs}$  characteristics of a 100-nm p-type SB-MOSFET (a) without a post silicidation annealing step, with a post silicidation annealing in forming gas  $N_2/H_2$  (97%-3%) performed at (b) 450 °C for 4 min and (c) 500 °C for 5 min.

the MOS structure. Fig. 6(a) gives the reference band configuration in absence of electrically active defects. Fig. 6(b) shows that donor levels become positively charged when gate-induced bending curve bands sufficiently upward to leave these defects unoccupied when located above the Fermi level. This results in the formation of an additional charge dipole that leads a global increase of the total barrier that holes have to overcome before entering the channel. Conversely, Fig. 6(c) shows that occupied acceptor levels are negatively charged when lying under the Fermi level. This charge state induces a band deformation that tends to lower the SB to holes ( $\phi_{bp}$ ). Based on the above considerations, one way to explain the flattening of current characteristics in Fig. 4 is to consider a modulation of the SB by deep level Pt-induced defects. To support this assertion, Fig. 7 shows the experimental  $I_{ds}-V_{gs}$  characteristics of the 100-nm-long device submitted to different post-silicidation annealing steps. In the first case [Fig. 7(a)], no post anneal was conducted leading to poor subthreshold characteristics and to a significant scattering of the current-voltage ( $I-V$ ) curves. This behavior is clearly the signature interface states often attributed to the well-known  $P_{b0}$  center [35] at the gate oxide-silicon channel interface. Depending on the occupation of these interface traps which is subject to band bending at the  $\text{SiO}_2\text{-Si}$  interface, the threshold voltage varies with gate voltage leading to the degradation of the subthreshold slope [36]. Under these conditions, the potential effect of Pt-related defects on the S/D SB is completely hidden by the overwhelming contribution of the interface states. In the

second case [Fig. 7(b)], a silicidation post anneal performed at 450 °C for 4 min significantly decreases the subthreshold swing to 80 mV/dec. This improvement can be attributed to the passivation of  $\text{Si/SiO}_2$  interface states. Concomitantly, current levels are significantly increased over the entire range of gate bias. Finally, a post anneal realized at 500 °C for 5 min [Fig. 7(c)] clearly shows a complete passivation of  $\text{Si/SiO}_2$  interface states with a swing and DIBL that steadily improve to 70 mV/dec and 60 mV/V, respectively. In counterpart, the current flattening at the onset of strong accumulation ( $0.25 \leq |V_{gs}| \leq 1$  V) is markedly enhanced. Referring to the discussion in Section III-C, it is well established that acceptor deep level defects related to Pt-H complexes dissociate at temperature above 350 °C for 1 h [31]. Although, the dissociation may be incomplete in the present case due to the reduced annealing time, it is reasonable to consider that the concentration of Pt-H complexes is reduced at the benefit of donor levels recovery. The expected result is therefore an incremental increase of the SB to holes that is clearly observed in Fig. 7(c) through the reduction of current drive.

#### E. $I_{on}-I_{off}$ Figure of Merit

Although not optimized in terms of passivation treatment, Fig. 8 shows the  $I_{ds}-V_{ds}$ ,  $I_{ds}-V_{gs}$  and  $g_m-V_{gs}$  characteristics of a 40-nm SB MOSFET. An excellent current drive of 425  $\mu\text{A}/\mu\text{m}$  at  $V_{ds} = V_{gs} = -2$  V is associated to an off-state current of 368 nA/ $\mu\text{m}$ . A compilation of  $I_{on}/I_{off}$  data of the

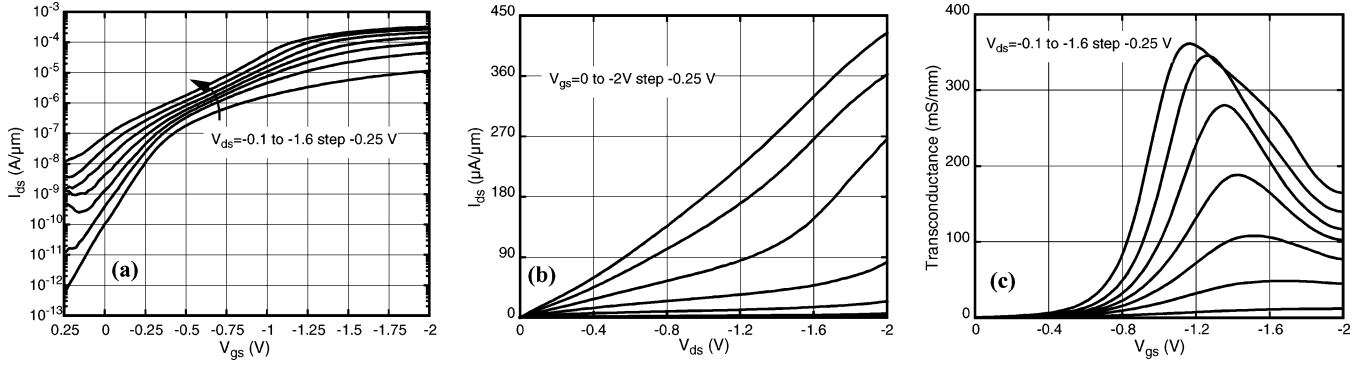


Fig. 8. (a)  $I_{ds}$ - $V_{gs}$ , (b)  $I_{ds}$ - $V_{ds}$ , and (c)  $g_m$ - $V_{gs}$  characteristics of a 40-nm SB p-MOSFET (without post-silicidation annealing).

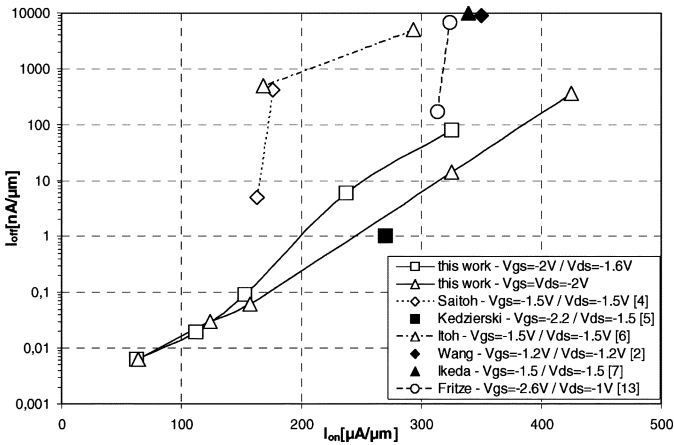


Fig. 9.  $I_{on}$ - $I_{off}$  figure of merit of recently published SB-MOSFETs.

most significant references related to fabricated SB-MOSFETs is presented in Fig. 9 and places the present work favorably with respect to the state-of-the-art. A performance comparison between Pt-based SB and p-type conventional S/D architectures [37]–[39] proves to be a difficult exercise as channel lengths, gate dielectric thickness and supply voltage may significantly differ. Based on MASTAR simulations [40], it can be estimated that on-state current drives of SB-MOSFETs remains 30% behind those of conventional highly doped S/D devices. However, retracing recent work on SB S/D integration, e.g., [4], [6], Fig. 9 shows that  $I_{off}$  has been lowered by almost four decades at a comparable  $I_{on}$  around  $160 \mu A/\mu m$ . Conversely, the on-state current has doubled, keeping the off-state current fixed below  $10 nA/\mu m$ . The striking point is that SB-MOSFETs steadily progress both in terms of device architecture and electrical performance. At the present time, the main limitation to current drive capabilities is the integration of Schottky S/D contacts with a sufficiently low barrier ( $\leq 0.1$  eV), as estimated by Connelly *et al.* [41] in a theoretical study. Material engineering applied to SB reduction is therefore identified as a key activity necessary to assure the competitiveness of the SB-MOSFET architecture that holds the promise of reduced process complexity and high-frequency performance [13].

#### IV. CONCLUSION

A 40-nm SB-MOSFETs that features a midgap tungsten metal gate and PtSi S/D on a thin SOI film has been demon-

strated for the first time. Excellent  $I_{on}/I_{off}$  performance in excess of 6, 4, or 3 decades have been obtained at  $V_{dd} = -2$  V for channel lengths of  $2 \mu m$ ,  $100$  and  $40$  nm, respectively. A post silicidation anneal under forming gas is shown to significantly improve the subthreshold slope by passivating defects located at the Si-SiO<sub>2</sub> interface, as expected. Consistent with the dominant role of donor-like Pt-induced deep level at annealing temperature above  $350$  °C, the loss of current drive observed at the transition between weak and strong accumulation is attributed to a deformation of the energy bands that increases the barrier height to holes in the vicinity of the Schottky interface.

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