Experimental Analysis of Punch-Through Conditions in Power P-I-N Diodes

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***Abstract*—Commercial power diodes are optimized to feature punch–through behavior. However, a tradeoff between the width and the doping level of the diode epitaxial layer leads to various levels of optimization. For a given breakdown voltage, a shorter epitaxial layer width leads to better transient performances. Device datasheets do not cover this issue and a simple experimental setup is presented to assess the optimization conditions inside the diode epitaxial layer. Three commercial devices are tested and experimental results are confronted to device simulations. A good agreement is found.**

***Index Terms*—Avalanche, p-type, intrinsic, n-type (P–I–N) diode, punch-through (PT), reverse-recovery.**

I. Introduction

LOW-VOLTAGE drop and high-breakdown voltage p-type, intrinsic, n-type (P–I–N) diodes play an important role in power electronic applications. These devices are fabricated with complex technologies where many tradeoffs balance physical constraints. In particular the doping concentration, N_D, and the width of the low-doped base region, W_B, define the reverse breakdown voltage of the P–I–N diode and the resistance of the diode epitaxial layer under forward bias. In on-state the diode is mostly used under high-level injection operation. On the one hand a minimal value of the width W_B of the diode base region guarantees a minimum of charge storage and a faster recovery. On the other hand the larger W_B the higher the breakdown voltage, until a critical value of the electric field is reached. For a given voltage rating, device engineers shape the low-doped epitaxial central layer of the diode to obtain a high breakdown voltage but also indirectly the lowest on-state voltage-drop. There is then a tradeoff to settle between W_B and N_D.

The diode transient behavior is related mainly to the shape of the doping profile and the effective lifetime inside the epitaxial layer. These issues do not affect the tradeoff between the doping level and the width of the diode base.

The paper details an experimental and nondestructive method to assess the tradeoff between the width and doping level of the diode epitaxial layer. These latter values are required for accurate system-level simulation of devices. Most published accurate models of P–I–N diode have N_D and W_B as parameters [11], [13], [16], [17]. These models are intended to simulate reverse-recovery for example: it is a critical operation of a power diode inside a converter. System-level simulation should estimate overvoltage, overcurrent, power losses, oscillations, and electromagnetic compatibility among others quantities that a design engineer must control.

The paper focuses on the relation between the N_D/W_B tradeoff and the diode behavior during reverse recovery, and a method to quantify this tradeoff. The experimental method gives access to the tradeoff without the identification of the values for the doping concentration, N_D, and the diode base width, W_B. The values of N_D and W_B are not documented in device datasheets. They are difficult to identify, thus the interest of an experimental method to evaluate the tradeoff between the latter values.

Finally, one more interest of the proposed method is to determine punch-through (PT) or non punch-through (NPT) conditions of new design diodes like emerging devices in Silicone–Carbide, Gallium–Arsenide, or other large-gap materials. Avalanche may not be predicted in these devices as various semiconductor-related parameters are unknown like ionization coefficients or ionization velocities for example.

Fig. 1(a) presents a simplified one-dimensional (1-D) doping profile of a P–I–N-diode. The real doping-profile of commercial diodes is more complicated; particularly the shape at the N^-N^+ junction is critical [1], [2]. On the one hand, the industrial technology is confidential. On the other hand, a 1-D approach is sufficient to develop the experimental method presented here.

Fig. 1 presents the electric field distribution inside the diode under reverse-bias condition at the onset of avalanche phenomenon. The applied reverse-voltage induces a critical field and impact ionization becomes significant. Fig. 1(b) presents a diode with an epitaxial layer larger than necessary with respect to the doping profile (large W_B) (see Table I). The diode profile in Fig. 1(b) is exaggerated (thus not realistic) for the sake of demonstration. The electric field distribution remains triangular even at the beginning of avalanche. The unnecessary epitaxial layer from voltage breakdown point of view creates an additional resistive layer when the diode is forward-biased. Under high-level injection operation the excessive epitaxial layer means additional charge storage. Optimization means to shorten the diode epitaxial layer to reduce the forward voltage-drop even under high-level injection operation. Fig. 1(a) presents the electric field distribution for an optimized

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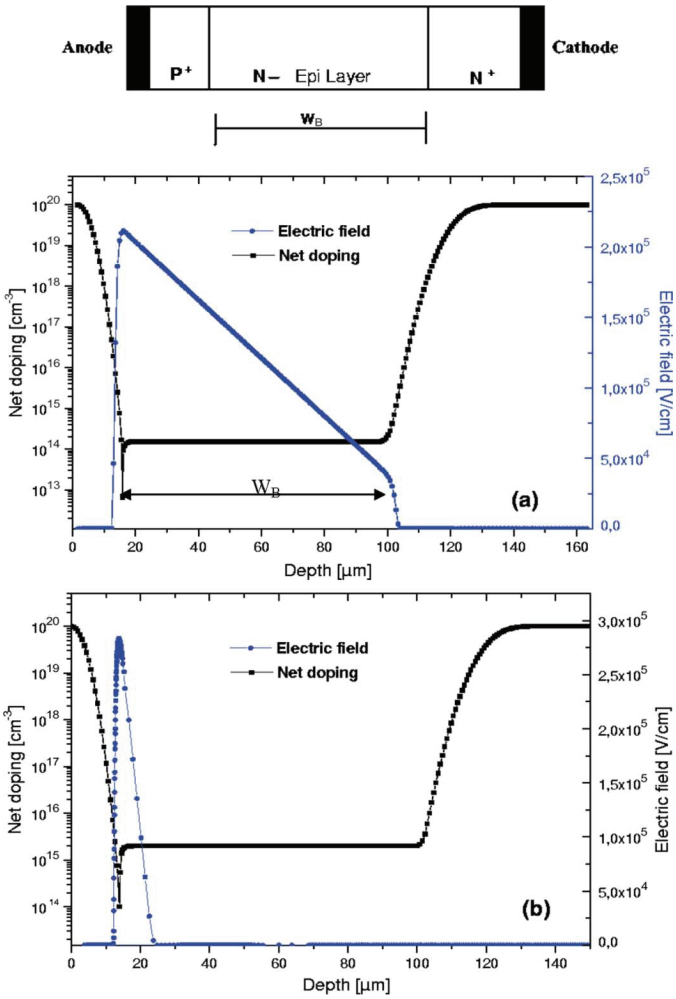

Fig. 1. One-dimensional typical doping-profile of a power P–I–N-diode. Distribution of the electric field inside the diode under reverse-bias conditions at the edge of avalanche. (a) A PT condition and a trapezoidal electric field (V_R ∼1100 V) and (b) a NPT condition and a triangular electric field (V_R ∼220 V).

TABLE I
DESIGN PARAMETER SET FOR PT AND NPT DIODES IN FIG. 1 AND FIG. 2

Technological parameters	N_D(cm^{-3})	W_B(μm)	A(mm^2)
punch-through diode (C)	1,6 . 10^{14}	83	5
non-punch-through diode (A)	2 . 10^{15}	83	5

(N_D, W_B) couple. The electric field is on the edge to change from triangular to trapezoidal when avalanche occurs.

Simulations of the static behavior of the diode are carried out using the device simulator Dessis-ISE [3]. The doping profile is entered as shown in Fig. 1 using the utility ISE-Mdraw [4]. The doping profile represents a typical 25-A/1000-V diode: $N_D = 1{,}6.10^{14}$ cm^{-3}, $W_B = 83$ μm and the effective area is 5 mm^2. The quasistationary mode is selected for the simulator as Poisson's Law mainly governs the diode reverse-bias operation.

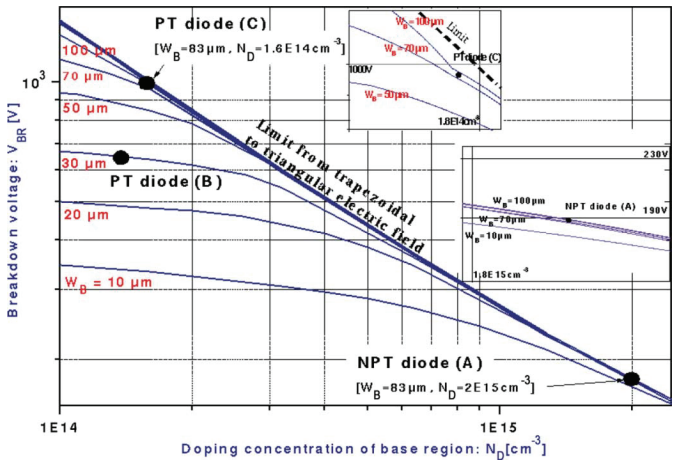

Fig. 2. Variation of the breakdown voltage $V_{\rm BR}$ versus N_D in the epitaxial layer of a P–I–N junction with W_B as a parameter.

The tradeoff between the doping level and the width of the diode epitaxial layer is documented in many textbooks with regard to the breakdown voltage [1], [2]. Fig. 2 pictures the breakdown voltage inside a highly dissymmetrical junction with W_B as a parameter. The result is obtained using a finite-element simulation based on the diode doping profile in Fig. 1(a). The breakdown voltage depends essentially on N_D and W_B. It is not affected by the lifetime inside the epitaxial layer or the diode area. A quasilinear limit appears in Fig. 2. This limit and its neighborhood region is the locus of (W_B, N_D)-couples leading to a triangular electric field at onset of avalanche (NPT diodes). Diode A is an example of NPT diode [Table I and Fig. 1(b)]. Diode B would be designed with PT behavior but with a low doping level in diode base leading to excessive charge storage and voltage drop in onstate. An optimized geometry corresponds to (W_B, N_D)-sets near the knee region but not too close to the limit, like diode C [Table I and Fig. 1(a)].

Basically the experimental method described here enables the design engineer to verify if a given diode is PT or not. Most commercial devices are PT, or they would feature poor transient and on-state performances. The method is useful with regard to new devices such as Silicon–Carbide P–I–N diodes. Due to Silicon–Carbide technology, the PT or NPT conditions inside the diode are unknown and can be verified using the experimental method. The proposed method offers also an additional experimental mean to validate P–I–N diode models.

PT and NPT are now classical definitions. They have been used for IGBT technologies for example. Concerning IGBT, other tradeoffs are experimented [5]. Recently, a study on PT/NPT tradeoff has been presented for light-triggered thyristor [6]. A reduction in thyristor thickness is demonstrated without noticeable detrimental effects on transient behavior. A section in [6] details the effect of the thyristor thickness on the proposed tradeoff. Analytical and experimental results show a decrease in charge storage for a given on-state voltage. Reverse-recovery is then faster and generates less power losses. The same results are of course applicable to the P–I–N diode. The thyristor leakage current is improved with the optimized PT layer compared to conventional structures. Finally [6] indicates

that the tolerance of the PT layer to dv/dt is almost the same as for conventional structures.

The literature related to diode technology is not recent. Papers analysed the diode recovery behavior [7]–[9]. The influence of the PT or NPT tradeoff on the diode recovery behavior is scarcely mentioned. The control of lifetime is the most recent issue to obtain soft or hard recovery behavior. In [8] a complex P^+ profile is experimented to soften the diode recovery. The PT tradeoff of the diode is not affected by the latter complex profile, as the epitaxial layer width and doping concentration remain essentially unchanged.

Many circuit models of the power P–I–N diode are reported in literature [10]–[16], but few are related to the diode technology and circuit models are not able to evaluate PT or NTP conditions.

A recent paper introduces an identification method of the diode main technological parameters with respect to a 1-D doping profile as shown in Fig. 1 [17]. An optimization procedure is used to identify the technological or design parameters based on a comparison between device simulations and experimental results. The identified parameters have been validated.

So far literature does not address the issues related to PT/NPT conditions in diode technology and the effects on the diode behavior. The present paper addresses an experimental method to verify the technological optimization (PT or NPT) of a given device. The next section introduces the physical analysis related to the proposed experimental method. Section III details the experimental method and the application to commercial diodes. The technological parameters of the commercial diodes are then identified to extract the values of the diode epitaxial layer width and doping level. The tradeoff between these latter values is then compared to the results of the proposed experimental method.

II. Analysis of V_{RM} Versus V_R During a Diode Reverse-Recovery

The diode epitaxial layer defines the device breakdown voltage. The paper focuses on the tradeoff necessary to obtain a given breakdown voltage while guaranteeing a minimal resistive layer, and thus the lowest onstate voltage drop. A large electric field appears inside the diode space-charge region during the reverse recovery. Some operating conditions may be reached that lead to a critical electric field initiating avalanche inside the diode epitaxial layer.

Avalanche breakdown voltage is evaluated when the leakage current density attains a threshold value and impact ionization thus becomes significant. A simplified review of avalanche conditions may be given using a 1-D representation of the diode. The doping profile of the drift region is assumed to be uniform while the doping profiles at the boundaries (P^+ and N^+) are assumed to be Gaussian for the sake of simple analytical expressions.

Using the depletion approximation in semiconductor device equations, the distribution of the electric field is computed as shown in Fig. 3, using the device simulator Dessis-ISE and the doping profile pictured in Fig. 1. Increasing the reverse-bias voltage creates an expansion of the space-charge region (SCR) in the N and P^+ regions, with a corresponding increase in the magnitude of the electric field at the P^+–N junction. A critical

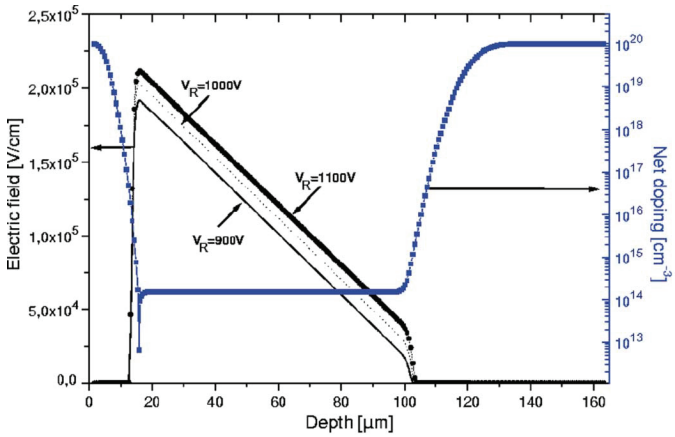

Fig. 3. Electric field distribution in an optimized P–I–N diode in the vicinity of avalanche operation.

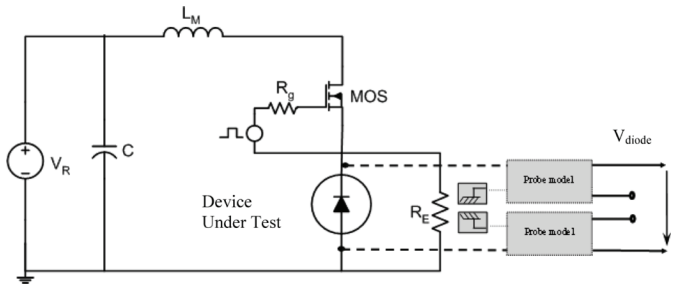

Fig. 4. Mosfet-diode switching cell for the measurement and simulation of the diode reverse-recovery (with null initial forward-current conditions).

value of the electric field may be reached that amplifies impact ionization and then avalanche. If the parameters W_B and N_D are optimized (a PT structure), the length of the N-region is slightly shorter than necessary to allow the SCR to completely expand when avalanche occurs (Fig. 3). The SCR is then said to "punch through," i.e., the SCR extends and finally joins the N^+ neutral region [1], [2]. The electric field decreases from a maximum value at the P^+–N junction to the N–N^+ junction.

A comparable electric field distribution may be obtained during a diode transient as reverse-recovery. Typically, the main switching parameters measured to characterize the diode recovery are the peak reverse voltage V_{RM}, the peak reverse current I_{RM}, the recovery time $t_{\rm rr}$ and the reverse recovery charge $Q_{\rm rr}$ among others. These parameters mainly depend on the internal diode structure and on external factors that are imposed by the circuit, the components and the operating conditions.

The variation of V_{RM} versus V_R in relation with the diode technology is analysed with the diode reverse-recovery from a zero direct current condition ($I_F = 0$ A). The thermodynamic equilibrium is selected as an initial condition. It avoids high-level injection conditions and limit power losses and device self-heating during the reverse recovery transient. An experimental circuit is proposed that is also used in simulation (Fig. 4). The device simulator Dessis-ISE enables mixed-mode simulation and is used to simulate the diode recovery within the switching-cell in Fig. 4. The diode is represented by its technological parameters while other circuit components are described

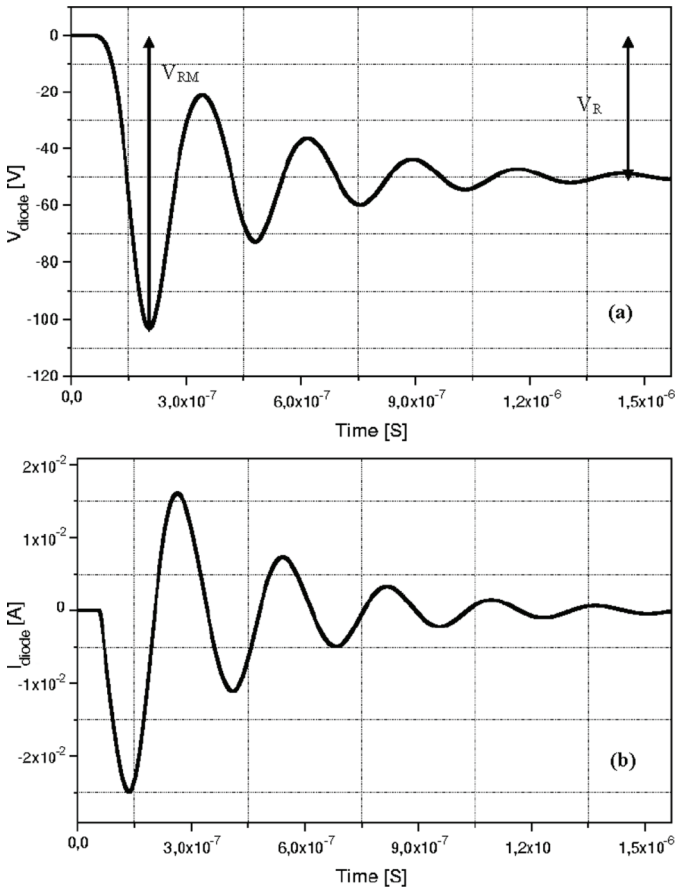

Fig. 5. Typical simulation waveforms of the reverse recovery of a diode in the circuit in Fig. 4. The diode doping profile in Fig. 1(a) is selected and $V_R = 50$ V. (a) Voltage. (b) current.

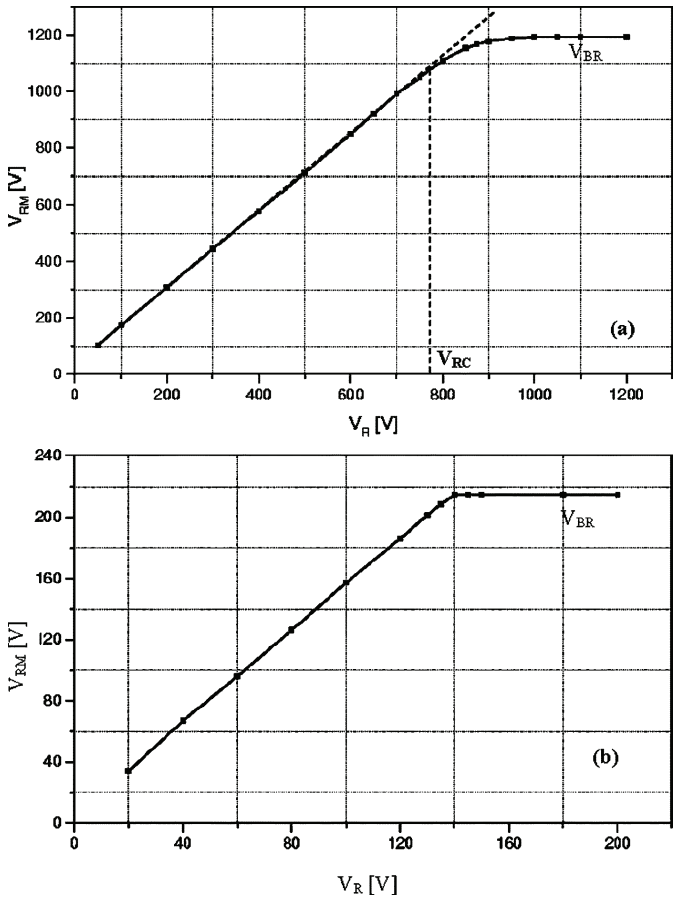

Fig. 6. Simulated variation of V_{RM} versus V_R during the diode reverse-recovery in the circuit in Fig. 4, using DESSIS-ISE: (a) PT diode of Fig. 1(a), $V_{RC} = 750$ V, breakdown voltage $V_{\rm BR} = 1115$ V and (b) NPT diode of Fig. 1(b), $V_{RC} \sim V_{\rm BR} = 225$ V.

using Spice equivalent models. The MOSFET transistor is represented by a Level-3 model and parameters identified from a 2SK1317 device.

The inductance, L_M (22 μH), is inserted to reduce the current-slope during the recovery transient, and to reduce significantly any effect of parasitic components like stray inductances. If L_M is too small, ripples on current waveform are not damped. If L_M is too large then commutation becomes very slow and current waveform features no oscillation but is not informative enough for the experimental method. L_M value is to be set according to the diode junction capacitance.

A resistor, R_E (4.7 kΩ), is inserted in parallel with the diode under test in the experimental circuit, to minimize the effect of the MOSFET leakage current and thus insure an initial thermodynamic equilibrium. The latter resistor is also considered in simulation as it affects slightly the diode behavior during reverse recovery. Voltage probe models are inserted in simulation to take care of the distortion on the experimental diode voltage waveforms. The probe models are detailed in [18].

Various simulations (Fig. 5) are performed to obtain the diode voltage waveform during reverse-recovery in the circuit in Fig. 4. The diode profile is pictured in Fig. 1(a) (Table I).

The variation of V_{RM} versus the applied reverse voltage, V_R, is extracted. Fig. 6 presents the typical variation for a PT and a NPT diode, respectively. Fig. 2 pictures the (N_D, W_B) tradeoff for both diodes. It appears in Fig. 6 that the peak reverse voltage, V_{RM}, varies linearly with the applied reverse voltage, V_R, up to a critical voltage, V_{RC}. Obviously the diode behavior changes for applied reverse voltage larger than V_{RC}.

PT diodes present the following behavior Fig. 6(a).

- If V_R is less then V_{RC}, the curve V_{RM} versus V_R is mostly linear. The electric field is triangular and there is a partial depletion of the epitaxial layer.
- If $V_{RC} < V_R < V_{\rm BR}$, V_{RM} presents a knee waveform. The electric field is trapezoidal and there is a complete depletion of the epitaxial layer.
- If $V_R \geq V_{RC}$, a peak value is obtained for V_{RM}. A constant electric field is established in the P^+–n junction. The device is considered to undergo avalanche breakdown when the role of impact ionization approaches infinity as the device cannot accommodate the additional electric field due to an increase in the applied reverse voltage, V_R.

If the base width and the doping concentration of the low-doped region are not optimized, a NPT structure is obtained, and the diode behavior is as follows Fig. 6(b).

- If V_R is less than V_{RC}, the curve V_{RM} versus V_R is mostly linear. The electric field is triangular and there is a partial depletion of the epitaxial layer.

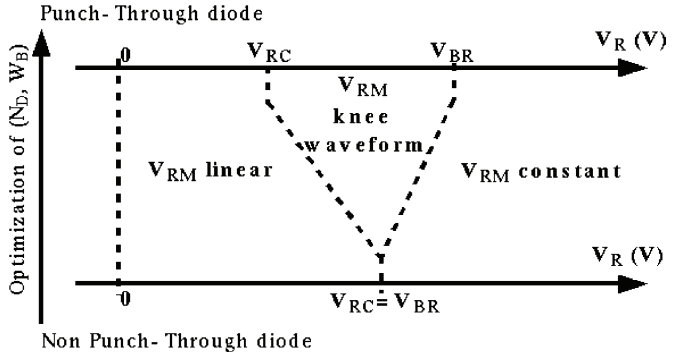

Fig. 7. Diode behavior during reverse recovery in terms of V_{RM} versus V_R with respect to (W_B, N_D) optimization.

- If $V_R \geq V_{RC}$, the electric field remains triangular but avalanche occurs in the epitaxial layer. The reverse recovery voltage is constant and the curve V_{RM} versus V_R represents a clear breakpoint.

In other words, V_{RC} correspond to a voltage limit between triangular and trapezoidal electric field in a PT diode. Increasing the reverse voltage, V_R, leads to an increase in the electric field before avalanche occurs. V_{RC} is less than the practical breakdown voltage. For a NPT diode, V_{RC} has no meaning, as the electric field remains triangular at onset of avalanche.

The here-above observation is used from experimental point-of-view to discriminate PT and NPT devices. Moreover the extension of the knee-region in Fig. 6(a) between partial and full depletion of the diode epitaxial layer may be a qualitative measure of the tradeoff between the width and the doping concentration of the diode base (Fig. 7). The better the optimization the larger the difference between V_{RC} and $V_{\rm BR}$.

III. Experimental Method

A simple experimental setup is proposed to obtain the variation of V_{RM} versus V_R as described in the previous section. The method is then applied to commercial diodes. The technological parameters of the commercial diodes are identified using a published method [17]. The values of W_B and N_D, diode epitaxial layer width and doping level, respectively, are confronted to the conclusion of the experimental measurements with respect to the PT or NPT behavior of the devices.

A. Test Circuit

Reverse recovery switching performances of the P–I–N power diode are evaluated in so-called depletion mode transient voltage and current analysis (DMTVCA). The circuit is pictured in Fig. 4. This circuit uses a 2SK1317 MOSFET transistor as the main switch, which is driven by a fast driver circuit (IR4429 IC). In practice, the resistor R_E is used to divert the leakage current of the MOSFET transistor when it is in off-state to insure the thermodynamic equilibrium of the diode. Otherwise the diode conducts a leakage current and the initial conditions ($I_F = 0$ A, $V_D = 0$ V) are not controlled. Unfortunately the resistor affects slightly the maximum reverse voltage, V_{RM}, of the diode during reverse recovery. Practically as the value of the resistor R_E is decreased, the maximum reverse voltage increases. A tradeoff between the leakage current and the effect on V_{RM} leads to a practical resistor value of 4.7 kΩ. The resistor power losses remain acceptable slowly repetitive operation. Moreover, the resistor doest not influence the variation of V_{RM} versus V_R as detailed in the previous section.

TABLE II
Design Parameters Identified From Three Commercial Diodes Using the Procedure Detailed in [17]

Diodes	BYW81P200	BYT08P400	STTB506
W_B(μm)	10	27	50
N_D(cm^{-3})	1.41×10^{15}	4.7×10^{14}	3×10^{14}
A(mm^2)	6.9	3.2	3.65

The current measurement is carried out using a 1 $\Omega/2$ GHz TMS-Research noninductive shunt [19], [20]. The diode current during reverse recovery is necessary for the identification method of the device technological parameters. Two voltage probes Tektronix P6139A [21], [22] are connected differentially to measure the diode voltage. The differential setup features a 400-MHz bandwidth.

B. Switching Waveforms

The diode technological parameters are identified from experimental measurements about the device reverse recovery as detailed in [17]. The 1-D diode technological description is considered as pictured in Fig. 1. The identification method comes as a four-step procedure to extract the value of the device effective area, A, the epitaxial width, W_B, the epitaxial layer doping level, N_D and the epitaxial layer ambipolar lifetime, τ. Results are listed in Table II.

Diode current and voltage waveforms are considered to validate the diode technological parameters. The diode reverse recovery is observed experimentally and by mean of simulation of the circuit in Fig. 4. Fig. 8 pictures the typical diode current and voltage waveforms. A 200-V commercial diode BYW81P200 is considered. The applied reverse voltage, V_R, is 100 V. There is no forward current ($I_F = 0$ A) when the MOSFET transistor is turned-on as explained previously. The current slope depends mainly on the applied reverse voltage V_R, the circuit parasitic inductance and the inductance, L_M. With no initial forward current, the diode behaves as a nonlinear capacitance. The discharge of the internal capacitance of the diode through the total circuit inductance and the resistance causes a resonating response. The damping effects in the current and voltage waveforms depend on the circuit total resistance. Simulation and experimental results are in good agreement, except for the RLC damping transient at the end of turnoff. So far the agreement between simulation and experiment validates the diode design-parameter values for the simulation objectives detailed in the paper.

The inductance, L_M, effectively masks the effect of the circuit parasitic wiring inductances. The resistor, R_E, is the major damping factor with the $R_{\rm DSON}$ of the MOSFET transistor. The presented method is based on the measurement of V_{RM}, maximum reverse voltage during reverse-recovery. Hence, it is not

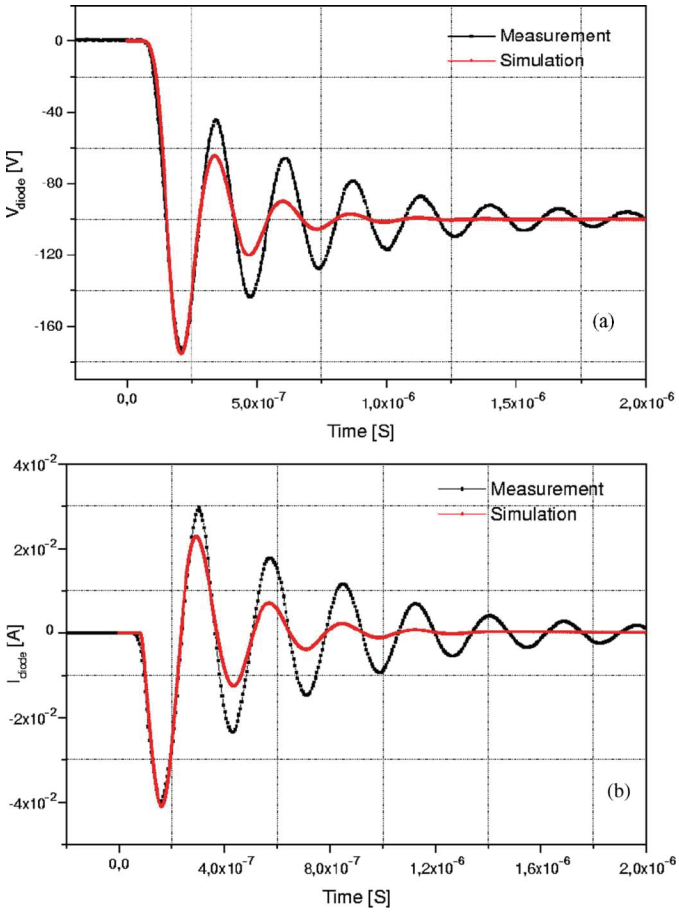

Fig. 8. Measured and simulated waveforms (DESSIS-ISE) during a BYW81P200 diode turnoff. (a) Voltage waveforms. (b) Current waveforms.

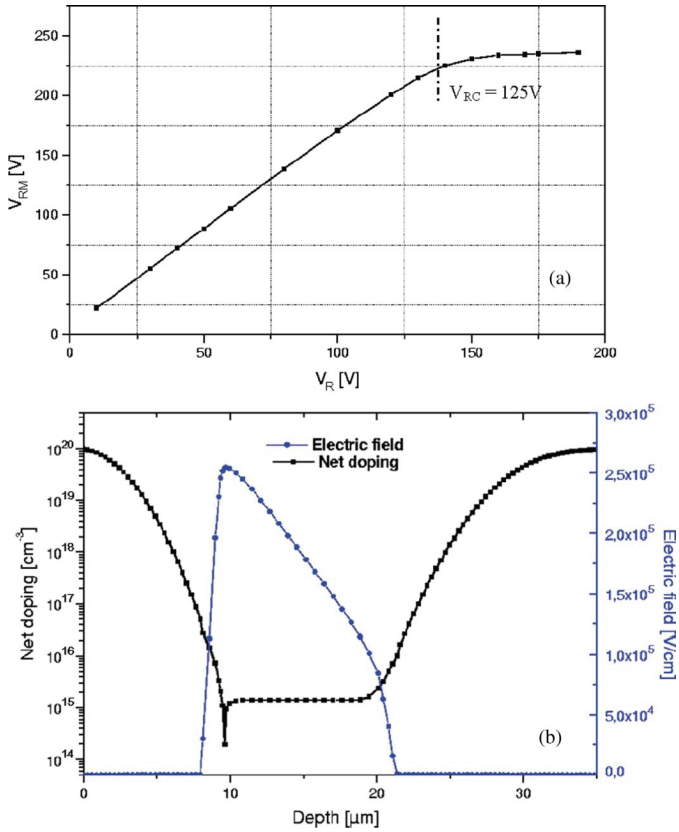

Fig. 9. Results for the device BYW81P200. (a) Experimental V_{RM} versus V_R, $V_{\rm BR} = 230$ V and $V_{RC} = 125$ V ($V_{\rm BR} = 200$ V in datasheet). (b) Simulated electric field distribution at onset of avalanche ($V_R = 200$ V).

necessary to refine the simulation to obtain a significant agreement at the end of reverse-recovery. Such an accurate simulation implies to evaluate any parasitic components and phenomena, and particularly the nonlinear capacitive behavior of the P–I–N diode. The latter behavior may be related to 2-D phenomena for example.

C. Measurement Results

Three commercial diodes have been tested: BYW81P200, BYT08P400, and STTB506. These diodes are optimized and thus feature a PT behavior. To be sure to test a NPT diode, it has been considered the emitter-base junction of a transistor like 2N1711 and 2N2219a devices for example. The transistor base doping level is high compared to the doping level of a P–I–N-diode epitaxial layer.

Fig. 9 pictures the electric field distribution at onset of avalanche and the curve V_{RM} versus V_R for device BYW81P200. The electric field distribution is simulated using Dessis-ISE in static-mode, and the diode design parameters in Table II. The two other commercial devices feature similar waveforms. Main experimental results are listed in Table III.

Fig. 10 presents the V_{RM} versus V_R curve obtained for the emitter-base diode of 2N1711 transistor. Avalanche occurs at $V_R = 9.2$ V. Transistor 2N2219a presents similar waveforms

TABLE III
MAIN PARAMETERS OF THE V_{RM} VERSUS V_R CURVES

Diodes	V_{BR}	V_{RC}	$(V_{BR}$-$V_{RC})/V_{BR}$
BYW81P200	200	130	0.3
BYT08P400	400	350	0.11
STTB506	600	500	0.16

and avalanche occurs at $V_R = 9.1$ V. The emitter-base diodes are not power diodes but the PT or NPT conditions remain the same. Obviously, emitter-base diodes present a NPT behavior. It is expected that avalanche occurs before PT in the base of a bipolar transistor because of the relatively high-doping level. Fig. 10 confirms the expectation. This also validates the proposed experimental method.

Obviously the identified diode technological parameters (Table II) and the V_{RM} versus V_R curves show a good agreement. The (N_D, W_B)-sets appear in the knee-region of the curves (Fig. 11), demonstrating a technological optimization of the devices for a PT behavior.

The tested commercial diodes feature a PT behavior. The emitter-base junction of the tested transistors features a NPT behavior as expected. The V_{RM} versus V_R curve shows the characteristic breakpoint as explained in the previous section.

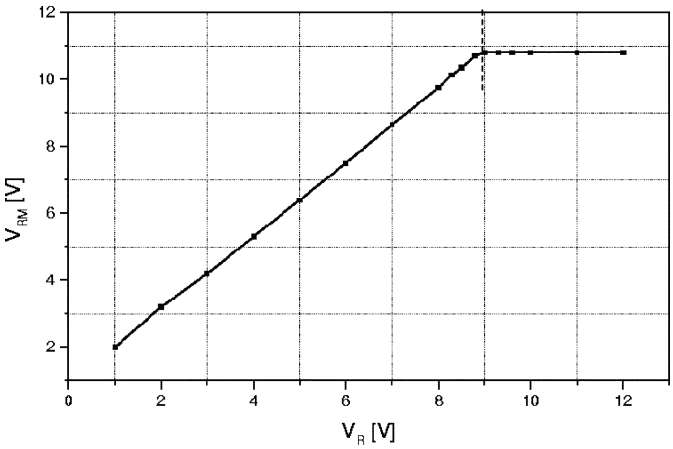

Fig. 10. Experimental V_{RM} versus V_R for the emitter-base junction of the transistor 2N1711.

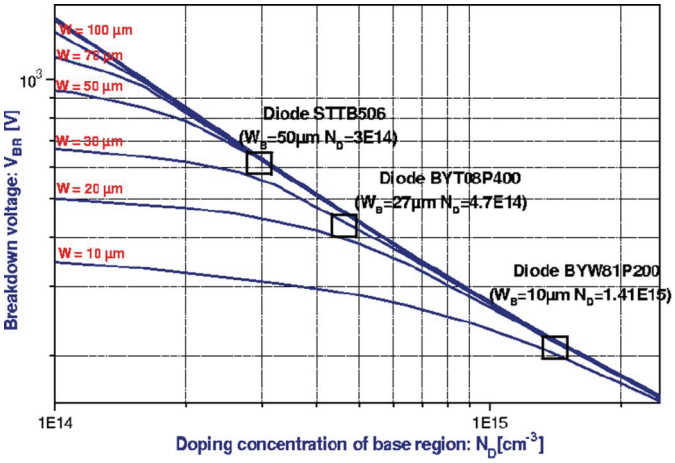

Fig. 11. Identified (N_D, W_B)-sets for three tested commercial diodes.

The main difference between the three commercial diodes lies within the expansion of the logarithmic region in the V_{RM} versus V_R curves. A larger region means an advanced and specific optimization of a given device for a PT behavior (Fig. 7 and Table III). Obviously the device STTB506 is more optimized than the BYT08P400 device but less than the BYW81P200. The measurement allows assessing this result and it shows that the technology of the BYW81P200 device enables the shortest possible W_B to guarantee the targeted breakdown voltage. Less charge-storage may be expected and improved performances during reverse-recovery for example. The technology of the BYT08P400 forbids shortening too much the epitaxial layer width to obtain the targeted breakdown-voltage. The device features a PT behavior but it is quite-close to a NPT behavior.

In the doping profile in Fig. 1, Gaussian approximations have been considered for the neutral regions $P+$ and $N+$. The simulation results are not affected when abrupt junction are considered instead of gradual junctions. In fact, the behavior of the diode space-charge region depends scarcely on the $P+$ and $N+$ region doping profile. The experimental method is then scarcely affected by the real doping profile of commercial devices. The V_{RM} versus V_R curves are not affected and the conclusion remains essentially the same for the optimization or not of the tested diode.

IV. Conclusion

An experimental method has been presented to test the PT or NPT behavior of a P-I-N power diode. The test is nondestructive but representative of the diode operating conditions in term of applied reverse voltage. The analysis of the electric field distribution is correlated to identify technological parameters of the devices.

The identification of the diode technological parameters is difficult and requires an assumption about the diode doping profile. A 1-D simple doping profile has been considered here. The identified parameter values are then approximate as commercial device doping profile is more complex. However a good agreement has been found between the (N_D, W_B)-sets and the V_{RM}-versus-V_R curves. The proposed experimental method is thus able to verify the tradeoff in the diode design between the epitaxial layer width and the doping level. A simple circuit is required with simple operating conditions. A zero-value initial current guarantees the lowest self-heating inside the device.

The presented method is validated in the two cases of PT and NPT diodes. It may then be applied to test new devices as Silicon–Carbide power P-I-N diodes for example.

Practically, a converter design engineer is expected to choose only PT-diodes as these devices show the best tradeoff between a high breakdown voltage, the smallest charge storage, and indirectly, the lowest forward voltage drop. Datasheets do not cover this technological issue. It is of course reasonable to assume that a commercial device has been optimized. In case of suspicion due to a surprising behavior of the device during reverse recovery, the proposed experimental method enables one to obtain a clear discrimination between optimized devices, i.e., PT or NPT devices, respectively, and also the level of optimization for PT-devices.

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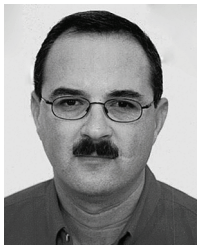

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