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This article reports on a direct method for patterning a tungsten gate in the decananometric range using high-resolution electron-beam lithography and reactive ion etching (RIE). Electron-beam lithography is based on the use of hydrogen silsesquioxane for its remarkable properties as a negative-tone resist, for its high resistance to dry etching and its capability to deliver extremely straight sidewalls. The transfer of the resist pattern into the tungsten gate stack is ensured by RIE based on a chemistry using sulfur hexafluoride and nitrogen. An optimization of the tungsten etching step is performed by investigating the impact of the RIE power, gas flows, and pressure on both the anisotropy and selectivity with respect to silicon dioxide. Finally, the integration of a *p*-type metal-oxide-semiconductor field effect transistor with a tungsten gate and platinum silicide Schottky source/drain was demonstrated and characterized to show that current-voltage characteristics do not exhibit symptoms of plasma-induced damage.
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I. INTRODUCTION

As complementary metal-oxide-semiconductor (CMOS) generations enter into the sub-65 nm technology node regime,[1] the use of polysilicon as gate material faces important issues that ultimately counterbalance benefits associated to the aggressive scaling of the channel length and gate oxide thickness. First, the polysilicon gate depletion reduces the gate capacitance in the inversion regime which in turn degrades the current drive capabilities.[2] Boron penetration from *p*-type poly-Si gate into the channel is another severe limitation to deep downscaling. Finally, in the high-frequency regime, the gate resistance is also recognized as a major source of performance degradation, as far as the maximum oscillation frequency (f_{max}) is concerned.[3,4] In that context, the introduction of a metal gate offers an alternative of choice to the aforementioned problems. The choice of tungsten as a gate electrode demonstrates many advantages, including high thermal stability, low resistivity, and CMOS process compatibility.[5,6] Moreover, tungsten features a work function close to silicon midgap which provides an appropriate low threshold voltage when coupled to a thin low doped silicon-on-insulator body.[7] Nevertheless, the integration of a metal gate remains a difficult task from a technological standpoint. One possible approach is to first define a dummy polysilicon gate structure that is subsequently replaced by a metal gate using gap filling and chemical mechanical polishing according to the damascene fabrication scheme.[8,9] Beyond the increase of the processing effort, this technique also introduces critical steps for the precise mask alignment of the metal line to the dummy gate cavity and holds the drawback of exposing the gate dielectric to reactive ion etching (RIE) that introduces plasma damage. Thus, a more direct patterning method of the metal gate by lithography and dry etching still remains an attractive and technically viable solution. The first challenge lies in the definition of a masking layer with nanometric dimensions compatible with the metal gate etching step. For that purpose, hydrogen silsesQuioxane (HSQ) was selected for its inorganic nature[10] that provides an excellent resistance to dry etching, giving typically a 24 $\times$ improvement over polymethylmethacrylate using for example a SF_6-based RIE chemistry. Primarily used as a flowable low permittivity dielectric,[11] HSQ also demonstrates excellent negative-tone resist properties suitable for electron-beam lithography.[12] In particular, the small size of the HSQ polymer chain gives access to very high-resolution performance when both electron beam exposure and development steps are optimized.[13] The second challenge is to ensure the proper transfer of the hard mask resist pattern into the metal stack using RIE. The etching must be anisotropic to provide vertical gate sidewalls and highly selective to ensure a precise etch stop at the ultrathin gate dielectric. In addition, the exposure to the RIE step must preserve the dielectric and silicon underlying layers from plasma damage and metallic contamination. Most tungsten RIE processes are based on fluorinated gas, such as CF_4, SF_6, CHF_3, and $CBrF_3$.[14–16] The main issue associated with these chemistries is the lack of anisotropy that can be compensated for by combining with an additional process gas, e.g., NF_3, that simultaneously introduces a passivation mechanism through the deposition of a polymer on the sidewall.[14] However, this type of process results, in most cases, in the production of sloped profiles where the base of the feature is wider than the initial mask width.[15] Another method combines a very reactive gas, such as sulphur hexafluoride (SF_6) with a halogenated gas containing silicon or carbon, e.g., CCl_4, CF_4, or SiF_4, $SiCl_4$, that also forms a passivating layer.[16] The main drawback of the last technique is also the production of sloped walls because

it proves difficult to accurately tune the ratio between etching and passivating species.[16] A final procedure associates SF_6 to a neutral gas, such as N_2. During gas dissociation, fluorine initially reacts with tungsten to form the volatile species $WF_{x\leqslant 5}$ and WF_6, and a resulting product composed of nitrogen and sulphur reacts with tungsten also forming a protecting thin film.[17] This article investigates this last approach in detail. After a brief description of the gate stack composition and our experimental procedure in Sec. II, the production of high-resolution HSQ resist patterns acting as a hard mask for dry etching is discussed in Sec. III. Particular attention is drawn in Sec. IV to the optimization of the tungsten etching step as a function of the process parameters: $N_2/(SF_6+N_2)$ ratio, gas flow, pressure, and operating rf power. Finally, Sec. V provides a validation of the gate fabrication process through the characterization of a *p*-type Schottky-barrier (SB) metal-oxide-semiconductor field effect transistor (MOSFET) that does not exhibit any sign of degradation related to plasma-induced damage.

II. EXPERIMENT

The gate stack consists of a (100) Si substrate (*p*-type doped $4-10\ \Omega$ cm) which is thermally oxidized in a dry atmosphere to grow a thin gate oxide layer followed by the deposition of a 40 nm thick tungsten layer acting as the gate material. A first degreasing step applied to the bare substrate was performed in acetone followed by a rinse in isopropyl alcohol. A standard RCA cleaning step was subsequently applied to remove any possible surface contamination. Before being loaded into the oxidation tube, the native oxide was removed by a $HF:H_2O$ (1:100) dip for 30 s, followed by a rinse in deionized water. The thermal oxidation was performed at 725 °C under a flow of 2 l/min of O_2 to obtain a gate oxide of $\sim$2.2 nm. The process includes a preoxidation ramp from 675 °C to 725 °C for 30 min under a reduced oxygen atmosphere (0.2 l/min O_2 and 2 l/min N_2) that generates a smooth and well-controlled interface. The 40 nm thick tungsten film was deposited by electron-beam evaporation with a base vacuum before deposition of 2×10^{-8} Torr. It is worth noting that no additional cleaning, e.g., by Ar sputtering, was applied prior to metal evaporation in order to preserve the gate oxide integrity. Etching experiments have been conducted in a conventional capacitively coupled rf-driven (13.56 MHz) plasma reactor with a stainless steel chamber.

III. DEFINITION OF A HSQ HARD MASK

A solution of HSQ diluted in methyl isobutyl ketone marketed by Dow Corning under the name of FOx-12 was used. The solution of HSQ was spin coated at a speed of 3000 rpm for 60 s yielding a 50-nm-thick resist layer. The HSQ film was prebaked in two steps on a hot plate at 150 °C for 120 s and 220 °C for 120 s. Electron-beam exposure was realized with a LEICA Electron Beam Pattern Generator (EBPG 5000^+) at an acceleration voltage of 50 kV and 800 pA beam current from which the spot size is estimated at 10 nm. Isolated lines with widths ranging between 10 nm to 100 nm were exposed at various doses using a single pass. The HSQ resist was developed by manual immersion in 0.26N tetramethyl hydroxyl ammonium (MF 322 Shipley) for 60 s, rinsed in deionized water, and blown dry with nitrogen. The optimum dose obtained for a simple beam pass exposure is 2000 $\mu C/cm^2$ for a 20 nm gate length [Fig.1(a)]. The resist line sidewalls feature a nearly vertical profile. Using this dose, a 50 nm designed gate length is correctly developed to its nominal value as exemplified in Fig. 1(b).

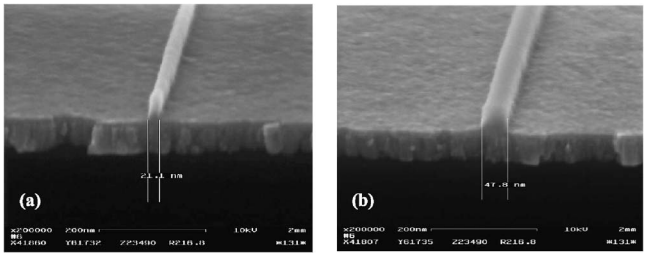

FIG. 1. 50 nm thick HSQ resist lines on top of a 40 nm thick tungsten layer deposited on a 2.2 nm silicon dioxide gate dielectric thermally grown on bulk silicon. HSQ was electron-beam exposed at 50 kV with a dose of 2000 $\mu C/cm^2$ under a beam current of 800 pA. The tungsten grains can be clearly observed. (a) 20 nm designed line measured at 21.1 nm and (b) 50 nm designed line measured at 47.8 nm.

IV. REACTIVE ION ETCHING ETCHING EXPERIMENTS AND RESULTS

After exposure and hard bake, HSQ has the remarkable property of evolving from a cagelike monomer to a network-like polymer that approaches the structure of SiO_2.[12] This property enables the use of HSQ directly as a hard mask with masking properties that approach those obtained by thermal oxide. Figure 2 gives the dependence of the tungsten etching rate on the main operating parameters, namely, the $N_2/(SF_6+N_2)$ gas ratio, the pressure of the chamber, the gas flow, and the rf power. The etching experiments have been conducted on the sample described in Sec. II, composed of 40 nm thick tungsten layer covering a thin SiO_2 gate dielectric of 2.2 nm thermally grown on a silicon substrate. The nominal parameters of the etching step are as follows: SF_6 and N_2 gas flow are both set to 10 sccm, the power is 50 W, and the pressure is tuned to 20 mTorr. Figure 2(a) shows the impact of the $N_2/(SF_6+N_2)$ flow ratio on the etching rates. Lee *et al.*[18] have argued that the presence of nitrogen accelerates the SF_6 dissociation resulting in an increase in atomic fluorine concentration according to the following mechanism $N+SF\rightarrow NS+F$. For a low $N_2/(SF_6+N_2)$ ratio, this effect partially compensates for the loss of reactive species due to SF_6 dilution. This mechanism does not hold for an important SF_6 dilution for which the tungsten etching rate decays rapidly. In contrast, the SiO_2 etching rate is not affected by dilution because physical etching remains the relevant mechanism. The variations of W and SiO_2 etching rates with gas pressure are depicted in Fig. 2(b). This graph mainly points out that the decreasing etch rate of SiO_2 with increasing pressure is the signature of a physical etching mechanism. This assertion is supported by the classical picture ac-

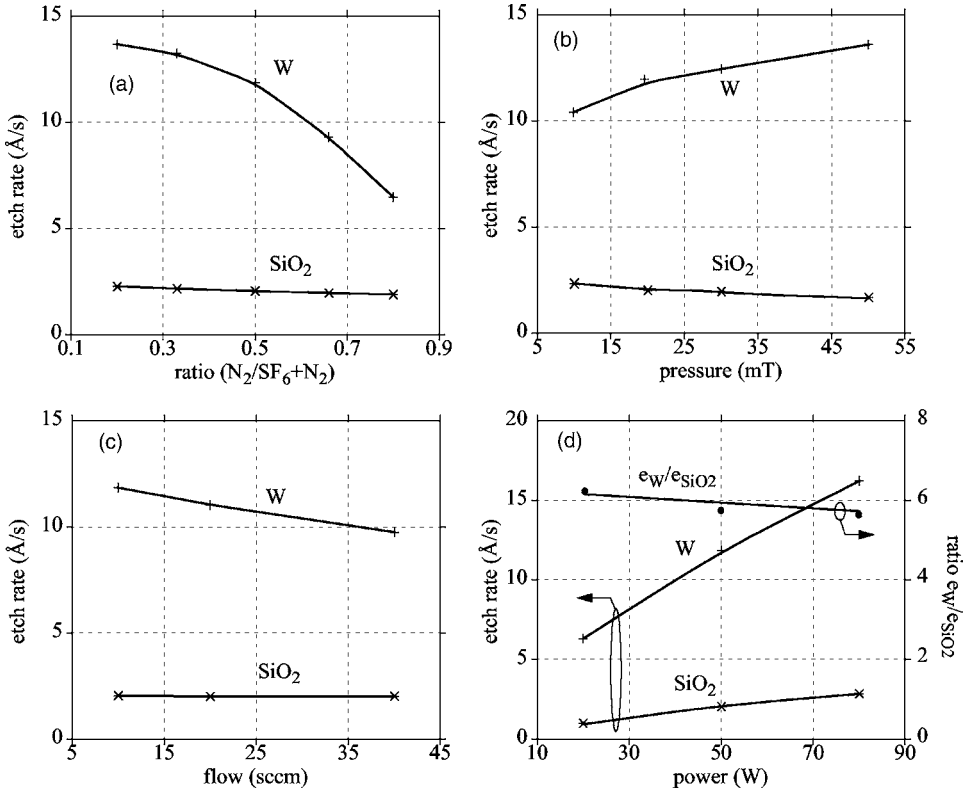

FIG. 2. Effect of RIE operating conditions on the etching rate of tungsten and silicon oxide. Nominal parameters are: SF_6 flow of 10 sccm, N_2 flow of 10 sccm, rf power 50 W, chamber pressure 20 mT. The sensitivity to the following parameters are studied: (a) $N_2/(SF_6+N_2)$ flow ratio, (b) pressure, (c) gas flows, and (d) rf applied power.

cording to which more collisions take place in a plasma under high pressure leading to a randomization of particles motions and, thus, to a loss of sputtering efficiency. The opposite trend is observed for the W etch rate, suggesting that a combination of chemical and physical etching mechanisms is involved. In the latter case, the density of chemically reactive species increases consistently with the observed increase of W etch rate. Figure 2(c) shows that the etching rate of SiO_2 remains constant with the flow of gas, indicating that the etch mechanism remains essentially of physical type because it is not dependent on the amount of reacting species. On the other hand, the W etch rate exhibits a more pronounced dependence on the gas flow that consolidates its chemical activity. Finally, Fig. 2(d) shows that the etch rates of W and SiO_2 both increase linearly with the rf power leading to a nearly constant selectivity er_W/er_{SiO2} equal to $\sim$6. This behavior is inferred by the fact that higher rf power provides increased kinetic bombardment energy to the plasma species, causing proportionally more sputtering of both W and SiO_2. As already observed in Ref. 18, the rf power applied to the substrate does not increase the dissociation of the fluorine, keeping constant the chemical contribution by F radicals. In order to characterize the anisotropy of RIE with operating conditions, characterizations by scanning electron microscopy (SEM) have been conducted on a gate stack protected by an HSQ strip that corresponds to the gate mask. The essential results are summarized in Fig. 3 that presents a series of SEM pictures showing the tungsten sidewall using various etching conditions. Starting from an initial 50 nm thick HSQ layer, it is worth noting that the remaining HSQ thickness after etching typically ranges in the 10–15 nm interval depending on the process conditions. First, it clearly appears that etching in pure SF_6 leads to undercutting as exemplified in the top views of Fig. 3(a). The introduction of nitrogen notably improves the steepness of the gate stack sidewalls [Figs. 3(b)–3(d)] as expected from the passivation mechanism discussed earlier. Also of interest is the presence of tungsten stringers at the base of the gate lines when the pressure of the chamber is set to 20 mTorr [Fig. 3(b)] indicating that an excess of passivation generates nonideal sidewalls. Operating at a lower pressure of 10 mTorr presents the advantage to correct this effect. Finally, a power of 50 W was found as a reasonable compromise that sufficiently promotes anisotropic physical etching to obtain a straight gate profile while keeping the end point detection controllable in a sufficiently long time window. In summary, correct etching of tungsten features is achieved with the following optimized parameters: SF_6 and N_2 flows of 10 sccm, rf power of 50 W, and pressure set to 10 mTorr. This selection is confirmed in Fig. 4 that demonstrates the excellent profile obtained on a 20 nm gate length and a smooth and flat SiO_2 surface state that confirms the selective nature of the etching technique.

V. INTEGRATION OF A TUNGSTEN GATE IN SCHOTTKY-BARRIER *P* METAL-OXIDE-SEMICONDUCTOR FIELD EFFECT TRANSISTORS

Plasma-induced damage is recognized as a source of device performance and reliability degradation. Many types of dry etch-related damage can be invoked, including metallic contamination, UV radiation, electrostatic discharge, and physical damage due to ionic bombardment. Ion-induced

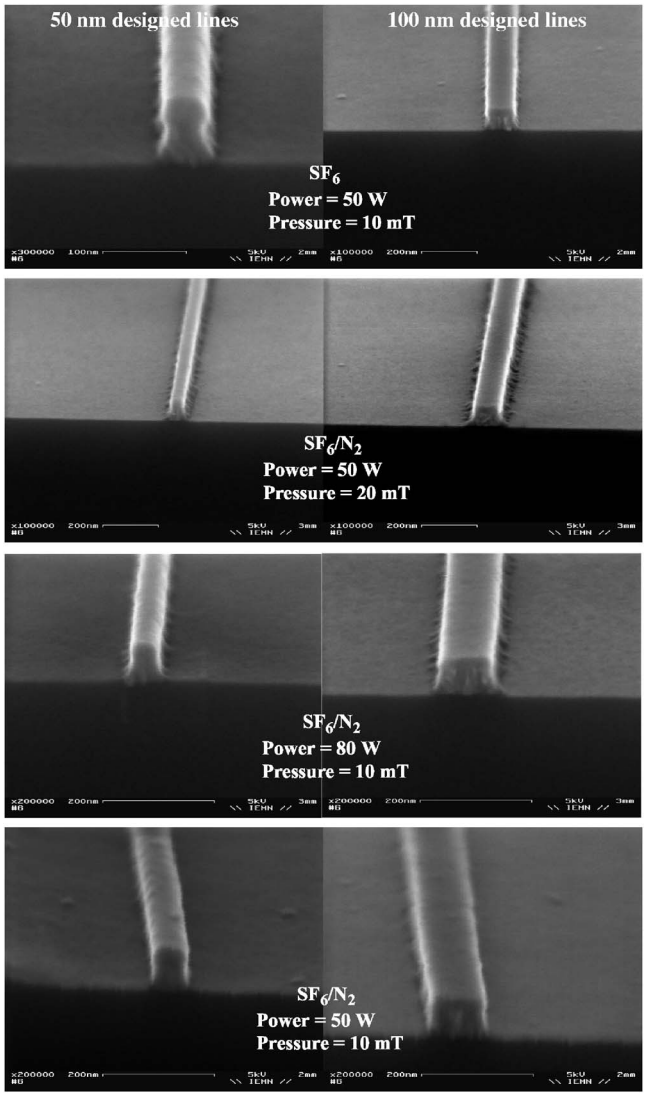

FIG. 3. SEM cross sections of the gate stack after etching. The stack remains covered by the HSQ resist used as a hard mask. Left side: 50 nm designed lines. Right side: 100 nm designed lines. (a) Undercut is observed with a pure SF_6 chemistry (10 sccm). (b) A mixture of SF_6/N_2 (10 sccm/10 sccm) promotes vertical sidewalls [(b)–(d)]. (d) Optimized parameters that eliminate etching residue at the bottom of the gate are: SF_6/N_2 (10 sccm/10 sccm), rf power 50 W, and pressure of 10 mTorr.

point defects and surface or interface nonstoichiometric states resulting from plasma exposure hold a major responsibility in the degradation of, e.g., gate dielectrics, carrier lifetime, and subthreshold metal-oxide-semiconductor characteristics.[19] Recently, SB source/drain (S/D) MOSFETs have prompted a renewed interest for their ability to solve end-of-roadmap roadblocks associated with the S/D architecture.[20] Recent theoretical work outlines the need for extremely low SBs ($\leqslant$0.15 eV) to reach a competitive current drive.[21] Nevertheless, the literature reports little work on the influence of plasma-induced traps on the modulation of SB height.[22–24] In that respect, it is well known that a high density of states at a given energy in the silicon band gap strongly pins the Fermi level and thus determines the SB height. In particular, donor states localized above the valence

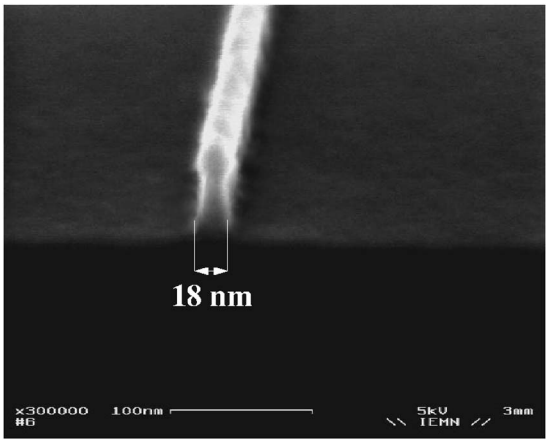

FIG. 4. SEM cross section of a 20 nm designed line etched under optimized RIE conditions with a mixture of SF_6 (10 sccm)/N_2 (10 sccm), rf power of 50 W, and a pressure of 10 mTorr.

band remain filled and therefore inactive (i.e., neutral) when bands are bending down. Conversely, these donor states are positively charged when empty and strongly pin the Fermi level when energy bands are sloping upward. The latter case is representative of the operation mode of a *p*-type SB-MOSFET for which energy bands in the channel are pulled upward by the electric field developed by a negative gate voltage. The aforementioned mechanism of trap emptying can result in a severe current loss at the transition between the subthreshold and the weak inversion regime depending on the density of traps.[24] In order to check the impact of plasma-induced damage during etching, a tungsten gate architecture has been integrated in a SB-MOSFET that features PtSi silicide contacts.[20] The S/D contacts and part of the channel located under the gate spacer are critical regions that have been exposed to the RIE plasma during the tungsten gate etching. From the drain current versus gate voltage electrical characteristic presented in Fig. 5, no sign of subthresh-

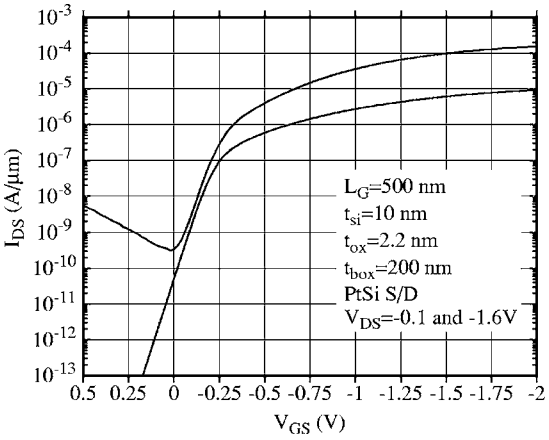

FIG. 5. Measured current-voltage (I_{DS}-V_{GS}) characteristics (log scale) of a long channel (500 nm) *p*-type MOSFET that integrates a tungsten gate and Schottky PtSi S/D. No degradation of the subthreshold slope is observed indicating that plasma-induced damage in the S/D contact and spacer regions remain negligible.

old slope deformation or of current loss is observed, indicating that the gate etching step developed in this work does not produce significant plasma damage.

VI. CONCLUSION

A direct method for patterning a tungsten metal gate down to 20 nm by electron-beam lithography and RIE has been investigated and optimized. HSQ, acting as a negative-tone electron-sensitive resist, was selected as a hard mask and also for its capability to deliver sharply defined high-resolution features after development. A RIE chemistry, based on SF_6 and N_2, was optimized for the anisotropic and selective etching of the tungsten gate stack. The optimization of the process parameters was performed to promote vertical gate sidewalls and high selectivity between tungsten and silicon dioxide. In a final validation step, the integration of a tungsten gate in a *p*-type MOSFET with PtSi SB S/D demonstrated that electrical characteristics do not show any sign of degradation related to plasma-induced damage.

ACKNOWLEDGMENTS

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